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A Multilevel Inverter Based Dual Voltage Source Inverter Design for Improving Power Quality of Grid

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Abstract

A Multi level inverter scheme is developed in Dual voltage source inverter (DVSI) to improve power quality and reliability of Microgrid system. The proposed plan consists of two inverters, power generated by the distributed energy resources (DERs) is injected as a real power by main voltage source inverter, furthermore to compensate the nearby unbalanced and nonlinear burden is done by auxiliary voltage source inverter.In main voltage source inverter, three levwl inverter is replaced with multi level inverter to synthesize a near sinusoidal voltage from several levels of dc voltages, the synthesized output waveform has more steps which provides a staircase waveform that approaches a desired wave form. The harmonic distiton of the output wave decreases, approaching zero as the number of voltage levels increases. Calculations are done for reference current generation of DVSI using ISCT to operate DVSI in grid sharing and grid injected modes . These works make the DVSI scheme a promising alternative for microgrid supplying weak loads. The topology and control calculation are approved through broad recreation and test results by using five level inverter it reduces THD percentage and improves efficiency.

Keywords: Network associated inverter, prompt symmetrical segment hypothesis (ISCT), microgrid, power quality.

I. INTRODUCTION

A Multi-level inverter is a power electronic device built to synthesize a desired ac voltage from several levels of dc voltages such as inverters. The five level inverter consists of standard three leg inverter and an H-bridge inverter in series with each inverter leg which uses a capacitor as a dc source. The regulation of capacitor voltage whie achieving an output voltage wavefom which is 25% higher than that obtained using a standard three leg inverter by itself. In a microgrid, power from various renewable vitality sources, for example power modules, photovoltaic (PV) frameworks, and wind vitality frameworks are interfaced to lattice and burdens utilizing power electronic converters. A lattice intelligent inverter assumes a critical part in trading power from the microgrid to the network and the associated load [2], [3]. Another essential aspect which must be tended to while the microgrid framework is associated with the maingrid is to keep the power quality. The increase in number of electrical burdens with uneven nonlinear streams has corrupted the power quality in the force appropriation net-work. Also, if there is a some amount of feeder Impedance in the circulation frameworks, the engendering of these consonant streams bends the voltage at the purpose of basic coupling. At the same moment, industry robotization has come to an abnormal state of refinement, where plants like car assembling units, compound processing plants, and semiconductor commercial ventures require clean power. For these applications, it is vital to remunerate nonlinear and uneven burden streams [4].

Load remuneration and force infusion utilizing lattice intuitive inverters as a part of microgrid have been exhibited in the prose[5],[6]. A solitary inverter framework with force quality improvement is examined in [7]. The principle center of this work is to acknowledge double functionalities in an inverter that would give the dynamic force infusion from a solar based PV framework furthermore functions. As a dynamic force filter, repaying unbalances and the receptive force required by different burdens associated with the framework. In [8], a voltage direction and force flow control plan for a wind vitality framework is proposed.

An appropriation static compensator (DSTATCOM) is used for voltage control furthermore for dynamic force infusion. The control plan keeps up the force equalization at the network terminal amid the wind varieties utilizing sliding mode control. A multifunctional power electronic converter for the DG power framework is depicted in [9]. This plan has the ability to infuse power produced by WES furthermore to execute as a consonant compensator

This concept presents a dual voltage source inverter (DVSI) plan, which empowers the microgrid to trade power produced by the distributed energy resources (DERs) furthermore to compensate the nearby unbalanced and nonlinear burden. This has favorable position that the evaluated limit of MVSI can simply be utilized to infuse genuine energy to the grid, if sufficient renewable force is accessible at the dc join. Besides, as the principle inverter is supplying genuine force, the inverter needs to track the central positive arrangement of current. This diminishes the data transfer

capacity prerequisite of the fundamental inverter. Since the helper inverter is supplying zero succession of burden current, a three-stage three-leg inverter topology with a solitary dc stockpiling capacitor can be utilized for the fundamental inverter.

II. DUAL VOLTAGE SOURCE INVERTER

A. Framework Topology:

The proposed DVSI topology is appeared in Fig. 1. It comprises of a nonpartisan point clasped (NPC) inverter to acknowledge AVSI and a three-leg inverter for MVSI [18]. These are associated with lattice at the PCC and supplying a nonlinear and lopsided burden. Likewise $i_{g(abc)}, i_{ugm(abc))}$, and $i_{ugx(abc)}$, show network streams, MVSI ebbs and flows, and AVSI ebbs and flows in three stages, individually.

The DER can be a dc source or an alternate source with rectifier coupled to dc join. Generally, renewable vitality sources like energy unit and PV produce power at variable low dc voltage, while the variable rate wind turbines create power at variable ac voltage. In this study, DER is being as a dc source.

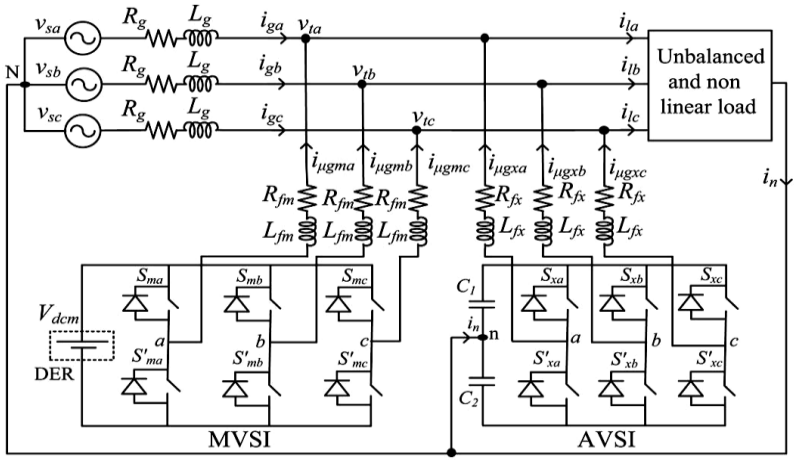


Fig.1: Topology of proposed DVSI scheme.

B. Outline of DVSI Parameters:

1) AVSI: The vital parameters of AVSI like dc connection voltage (V_{dc}), dc stockpiling capacitors (C_1 and C_2), interfacing inductance (L_{fx}), and hysteresis band ($\pm h_x$) are selected based on the configuration strategy for split capacitor DSTATCOM topology. The dc-join voltage over every capacitor is taken as 1.6 times the crest of stage voltage. The aggregate dc-join voltage reference (V_{dcref}) is observed to be 1040 V. Estimations of dc capacitors of AVSI are picked in view of the adjustment in dc-join voltage amid homeless people. Let complete burden rating is S kVA. In the most pessimistic scenario, the heap force may differ from least to greatest, i.e., from 0 to S kVA. Expect that the voltage controller takes n cycles, i.e., nT seconds to act, where T is the framework day and age.

$$\frac{1}{2}C_1(V_{dcr}^2 - V_{dcr}^2) = nST \qquad (1)$$

where V_{dcr} and V_{dc1} are the reference dc voltage and greatest allowable dc voltage crosswise over C_1 amid transient, separately. Here, S =5 kVA, Vdcr =520 V, V_{dc1} $=0.8*V_{dcr}$ or $1.2*V_{dcr}$, n=1, and T =0.02 s. Substituting these qualities in (1), the dclink capacitance (C_1) is figured to be 278000 µF. Same estimation of capacitance is chosen for C_2. The interfacing inductance is given by

$$L_{fx} = \frac{1.6V_m}{4h_x f_{max}} \qquad (2)$$

Expecting a most extreme exchanging recurrence (f_{max}) of 10 kHz and hysteresis band (h_x) as5% of burden current (0.5A),the estimation of Lfx is ascertained to be 26 mH.

2) MVSI: The MVSI utilizes a three-leg inverter topology. Its dc-join voltage is gotten as $1.15*V_{ml}$, where Vml is the crest estimation of line voltage. In this way, zero arrangement exchanging music will be truant in the yield current of MVSI. This lessens the filter necessity for MVSI when contrasted with AVSI. In this investigation, a filter inductance (Lfm) of 5 mH is utilized

III. CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control calculation for reference current era utilizing ISCT requires adjusted sinusoidal PCC voltages. Due to the nearness of feeder impedance, PCC voltages are contorted. Along these lines, the principal positive succession parts of the PCC voltages are removed for the reference current era. To change over the contorted PCC voltages to adjusted.

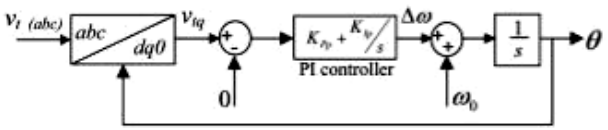


Fig.2: Schematic diagram of PLL.

The PCC voltages in characteristic reference outline (V_{ta}, V_{tb}, and V_{tc}) are first changed into dq0 reference outline With a specific end goal to get θ, a modified synchronous reference frame(SRF) stage bolted circle (PLL) is utilized. The schematic outline of this PLL is appeared in Fig. 2. It basically comprises of a corresponding basic (PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-hub (vtq) is contrasted and 0 V and the mistake voltage along these lines acquired is given to the PI controller.

B. Instantaneous Symmetrical Component Theory

ISCT was created essentially for uneven and nonlinear burden remunerations by dynamic force filters. The framework topology appeared in Fig. 3 is utilized for understanding the reference current for the compensator [15]. The ISCT for burden pay is inferred in view of the accompanying three conditions.

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0 \qquad (3)$$

2) The phase angle between the fundamental positive sequence voltage ($\angle V_{ta}^{+}$) and source current (i_{sa})

$$\angle V_{ta}^{+} = \angle i_{sa} + \varphi \qquad (4)$$

3) The average real power of the load (P_l) should be supplied by the source

$$V_{ta1}^{+}\, i_{sa} + V_{tb1}^{+}\, i_{sb} + V_{tc1}^{+}\, i_{sc} = P_l \qquad (5)$$

C. Control Strategy of DVSI

Control technique of DVSI is produced in a manner that lattice and MVSI together share the dynamic burden force, and AVSI supplies rest of the force segments requested by the heap.

1) Reference Current Generation for Auxiliary Inverter:

The dc-join voltage of the AVSI ought to be kept up steady for appropriate operation of the helper inverter. DC-join voltage variety happens in helper inverter because of its exchanging and ohmic misfortunes. These misfortunes termed as Ploss ought to likewise be supplied by the lattice. An expression for Ploss is inferred on the condition that normal dc capacitor current is zero to keep up a steady capacitor voltage [15]. A PI controller is utilized to produce Ploss term as given by

$$P_{loss} = K_{pv}\, e_{vdc} + K_{iv} \int e_{Vdc}\, dt \qquad (6)$$

where $e_{vdc} = V_{dcref} - V_{dc}$, V_{dc} represents the actual voltage sensed and updated once in a cycle .In the above equation, K_{pv} and K_{pv} represent the proportional and integral gains of dc-link PI controller, respectively.

2) Reference Current Generation for Main Inverter:

The MVSI supplies adjusted sinusoidal streams in view of the accessible renewable force at DER. In the event that MVSI misfortunes are ignored, the influence infused to network will be equivalent to that accessible at DER ($P_{\mu g}$).The taking after condition, which is gotten from ISCT can be utilized to produce MVSI reference streams for three stages (a, b, and c).

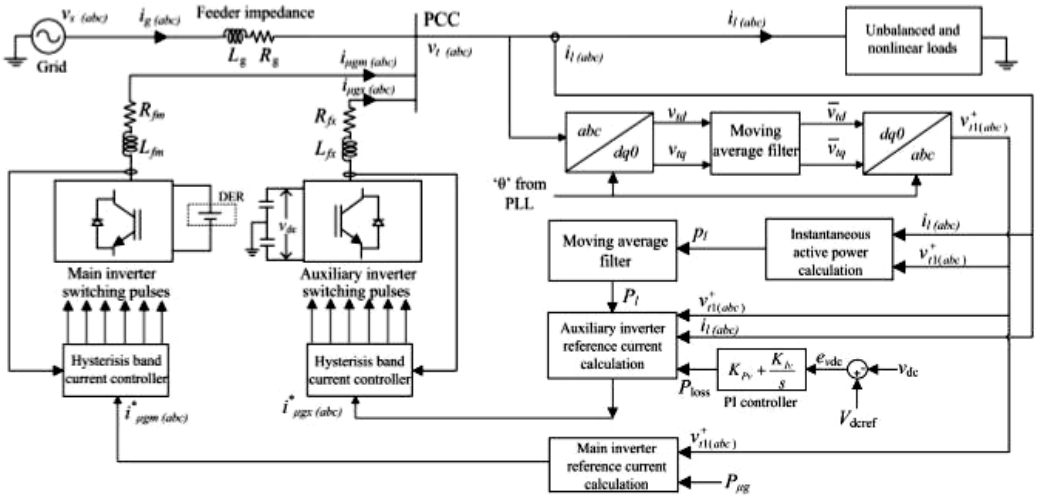


Fig.4: Schematic diagram showing the control strategy of proposed DVSI scheme.

D. Multi Level Inverter

A Multi level inverter is mainly used to synthesize a sinusoidal voltage from several levels of dc voltages. As the number of levels increases, the synthesized output wave form has more steps which provides a staircase wave that approaches a desired waveform. The harmonic distortion of the output wave decreases approaching zero as the number of voltage levels increases.

A five level inverter is developed and applied for injecting real power of the renewable power in to the grid to reduce the switching power loss, harmonic distortion and electromagnetic interference caused by the switching operation of power electronic devices.

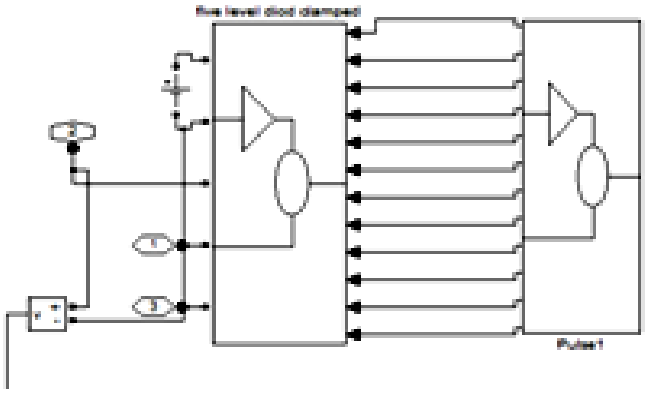


Fig 5: Five Level Inverter

IV. SIMULATION STUDIES

The recreation model of DVSI plan appeared in Fig. 1 is created in PSCAD 4.2.1 to assess the execution. The recreation parameters of the framework are given in Table I. The reproduction study shows the lattice sharing and matrixinfusing methods of operation of DVSI plan in consistent state and additionally in transient conditions. The mutilated PCC voltages because of the feeder impedance without DVSI plan are appeared in Fig. 5(a). On the off chance that these contorted voltages are utilized for the reference current era of AVSI, the present remuneration won't be legitimate. Along these lines, the essential positive arrangement of voltages is removed from these misshaped voltages utilizing the calculation clarified as a part of Section III-A. These separated voltages are given in Fig. 5(b).

Table I: System Parameters For Simulation Study

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
AVSI	$C_1 = C_2$ = 2000 μF V_{dcref} = 1040 V Interfacing inductor, L_{fx} = 20 mH Inductor resistance, R_{fx} = 0.25 Ω Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, V_{dcm} = 650 V Interfacing inductor, L_{fm} = 5 mH Inductor resistance, R_{fm} = 0.25 Ω Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	Z_{la} = 35 + j19 Ω Z_{lb} = 30 + j15 Ω Z_{lc} = 23 + j12 Ω
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, K_{Iv} = 0.05

These voltages are further utilized for the era of inverter reference streams. Fig. 6(a)–(d) speaks to dynamic force requested by burden (Pl), dynamic force supplied by framework (P_g), dynamic force supplied by MVSI ($P_{\mu g}$), and dynamic force supplied by AVSI (P_x), individually. It can be watched that, from t =0 .1 to 0.4 s, MVSI is producing 4 kW power and the heap interest is 6 kW. Amid this period, the proposed strategy comprises of double voltage source inverter (DVSI), the reason for utilizing this is to enhance power quality and dependability of Microgrid.

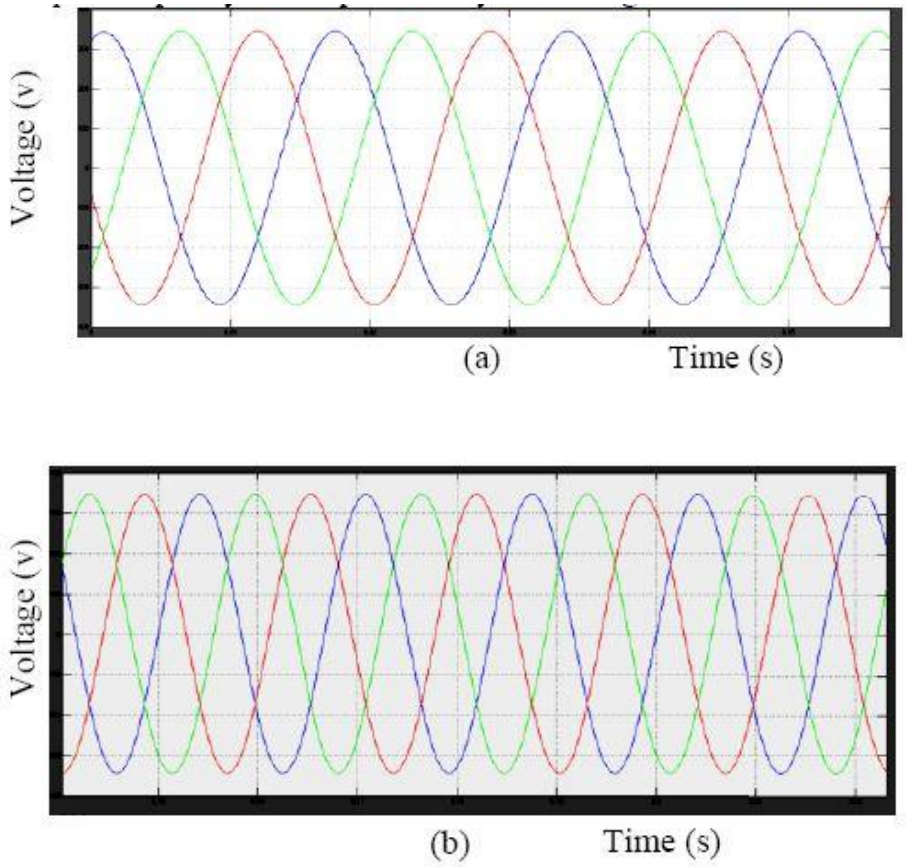
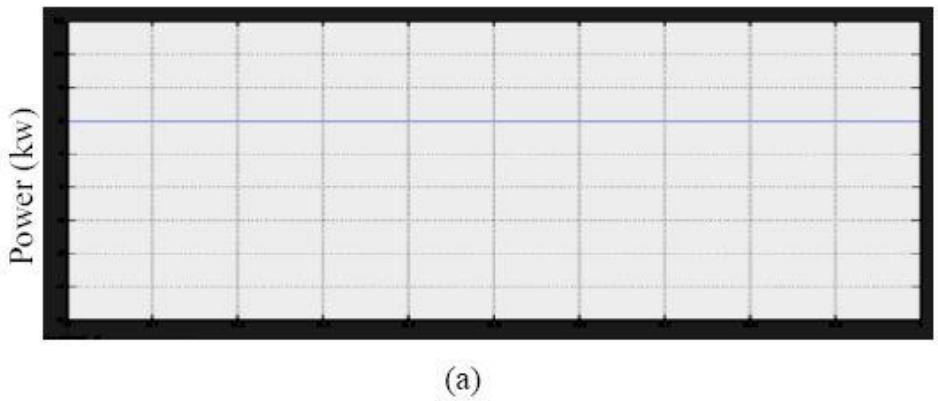


Fig.5: Without DVSI scheme: (a) PCC voltages, (b) fundamental positive sequence of PCC voltages

Fig Simulink model for DVSI scheme. The outputs for this model shown below



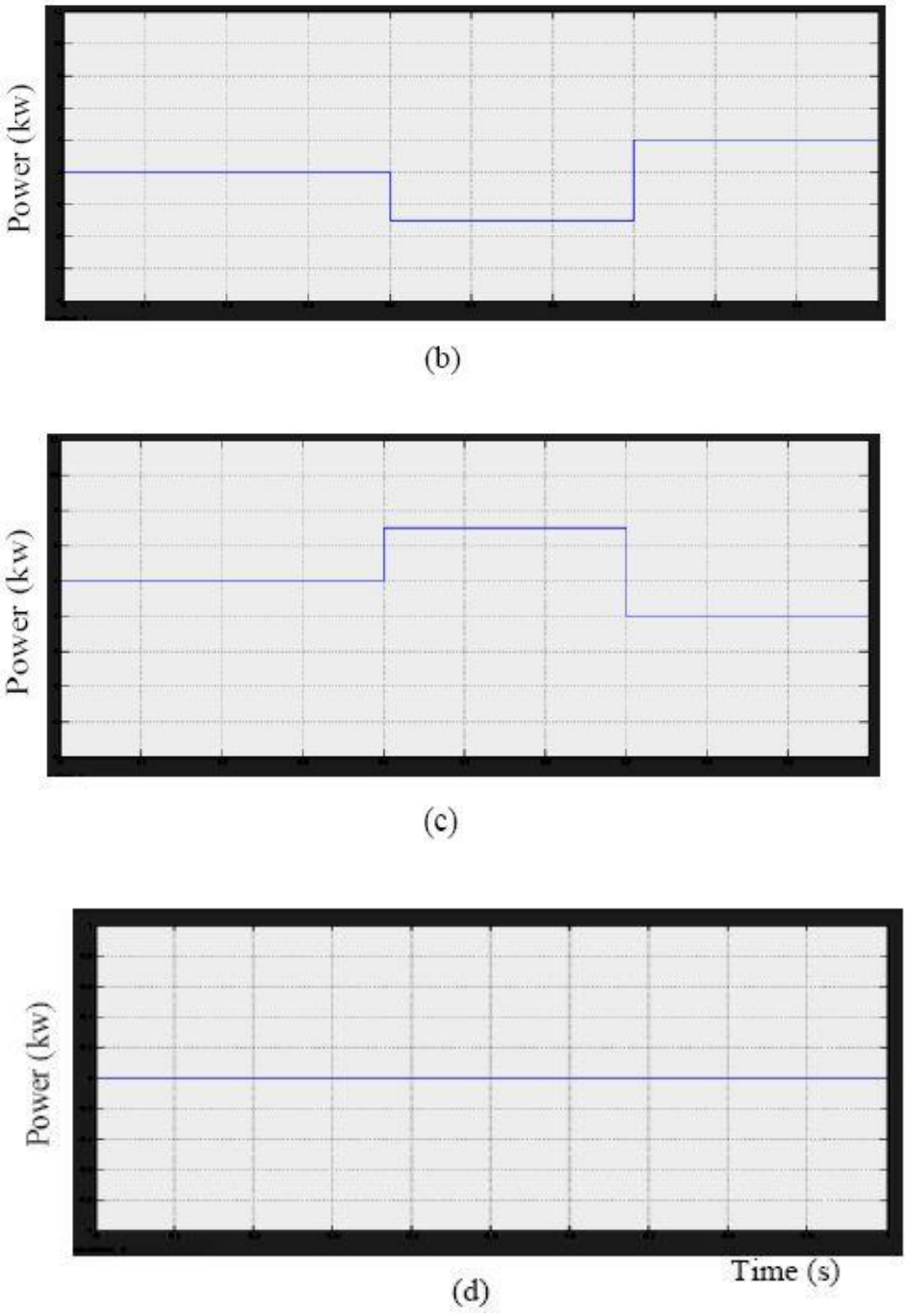


Fig.6: Active power sharing: (a) load active power;(b) active power supplied by grid;(c) active power supplied by MVSI;(d) active power supplied by AVSI.

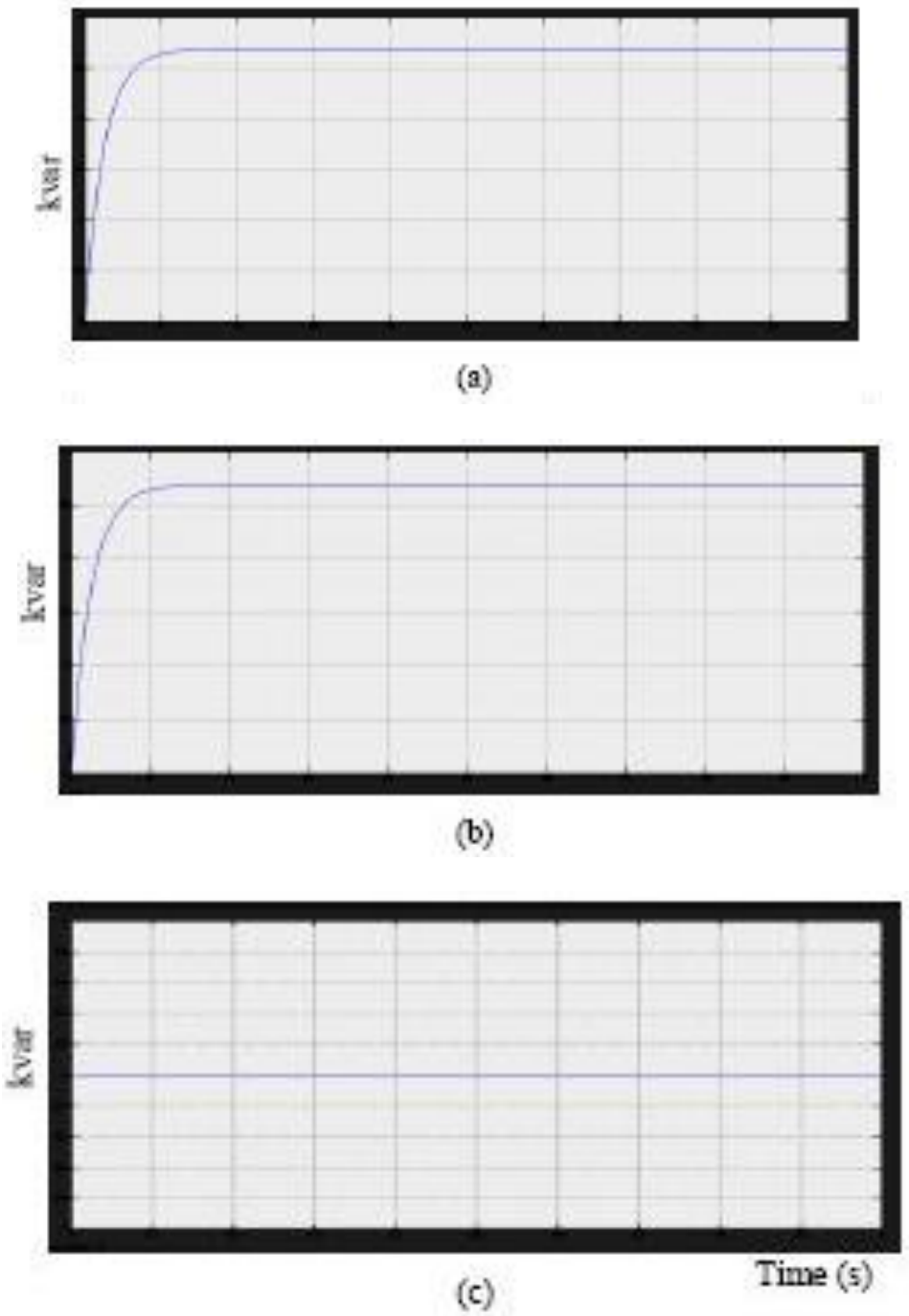


Fig.7: Reactive power sharing: (a) load reactive power(b) reactive power supplied by AVSI(c) reactive power supplied by MVSI.

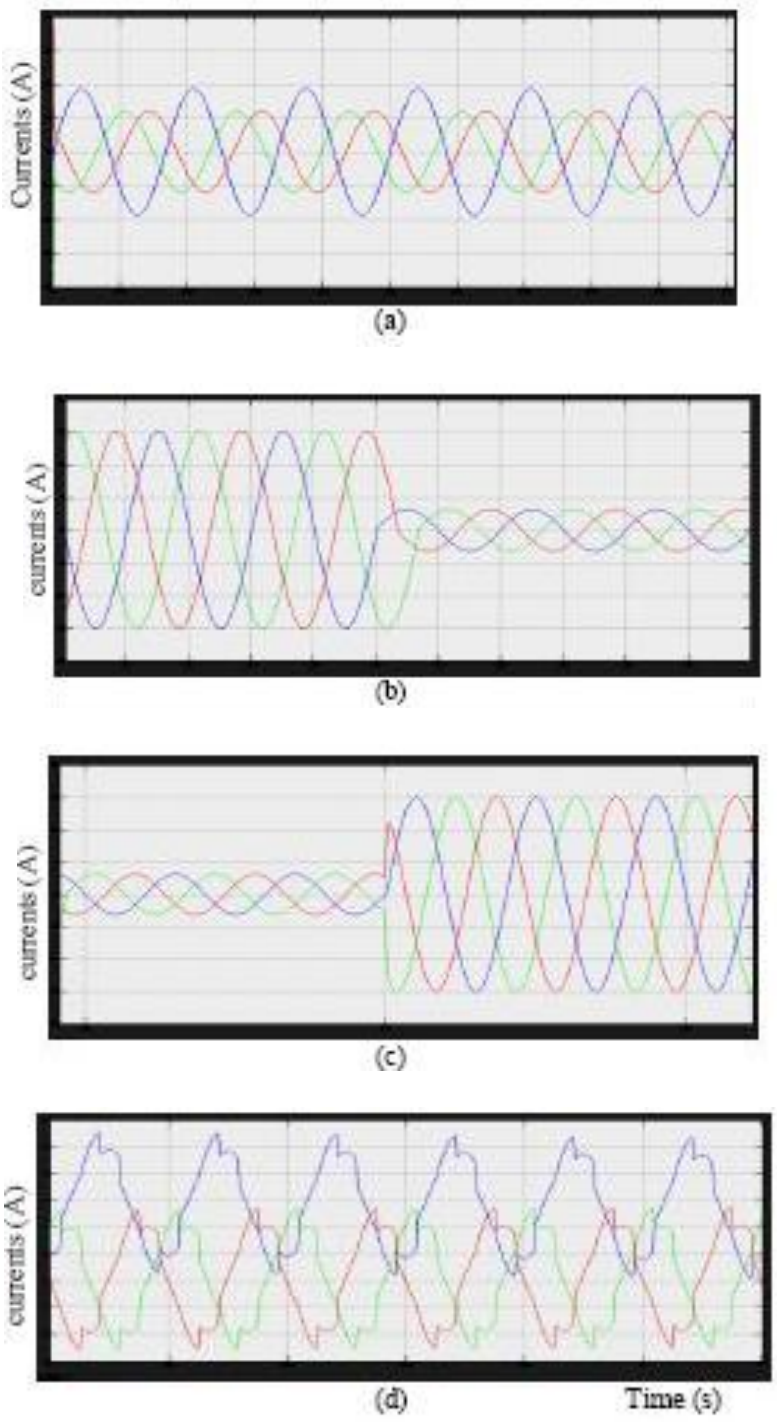


Fig.8: Simulated performance of DVSI scheme:(a) load currents (b) grid currents (c) MVSI currents; (d) AVSI currents

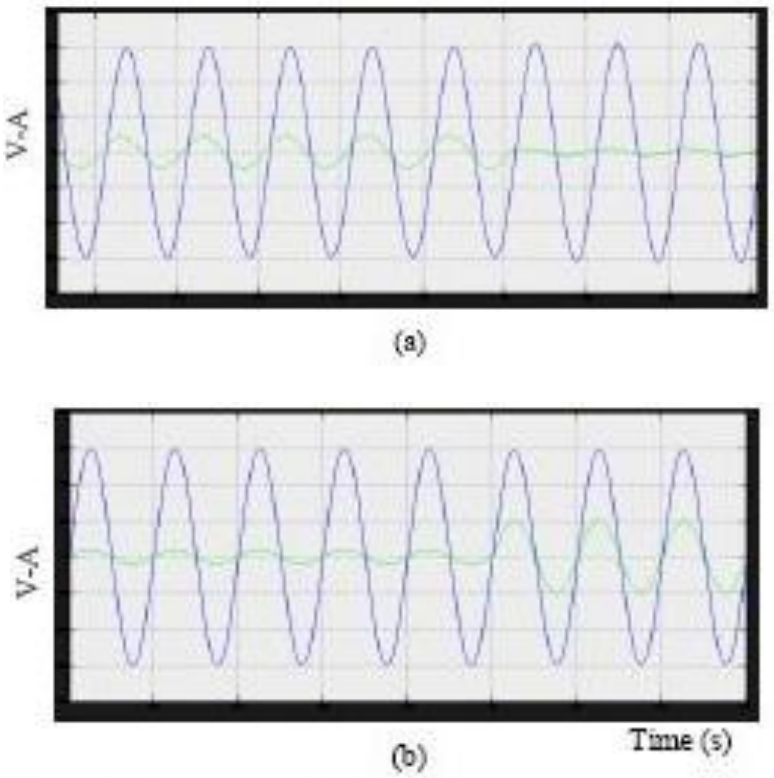


Fig.9: Grid sharing and grid injecting modes of operation: (a) PCC voltage and grid current (phase-*a*)(b) PCC voltage and MVSI current (phase-*a*).

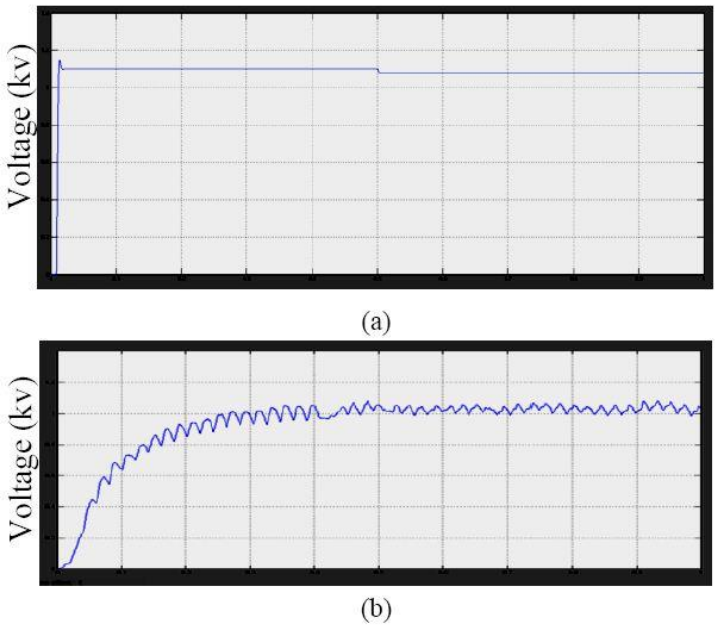


Fig.10: (a) DC-link voltage of AVSI(b) Zoomed view of dc-link voltage dynamics during load change

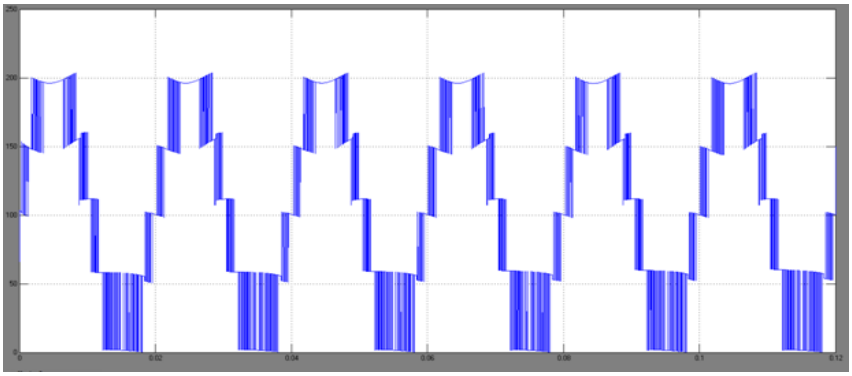


Fig.11: Five level output for main inverter

Comparison between three level and multi-level is shown below by using FFT analysis

Load voltage:

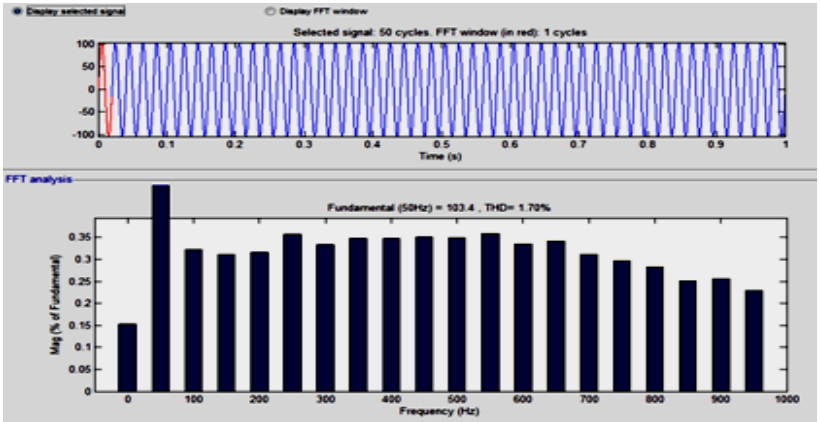


Fig.12: THD of load voltage for three level inverter

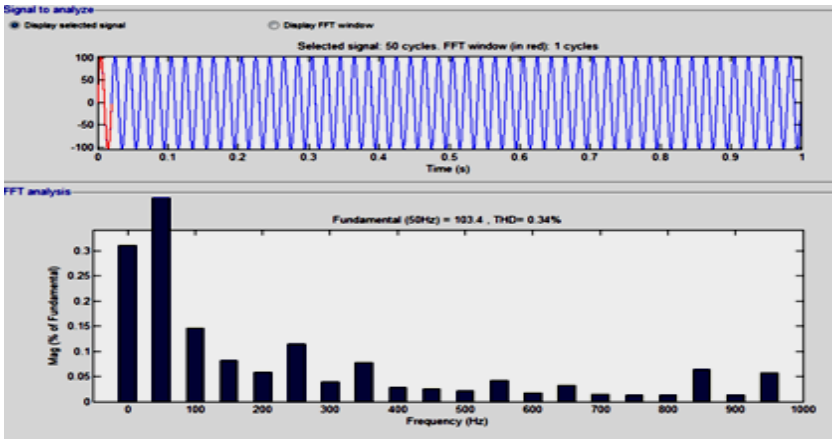


Fig.13: THD of load voltage for multi-level inverter

Load current:

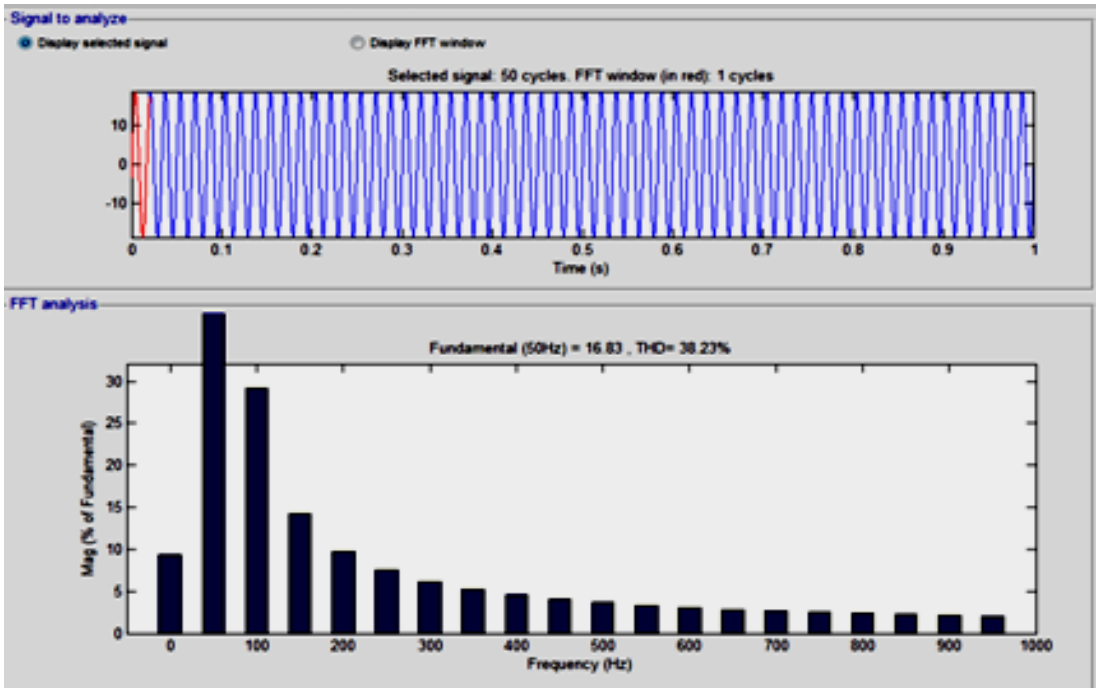


Fig.14: THD of load current for three level inverter

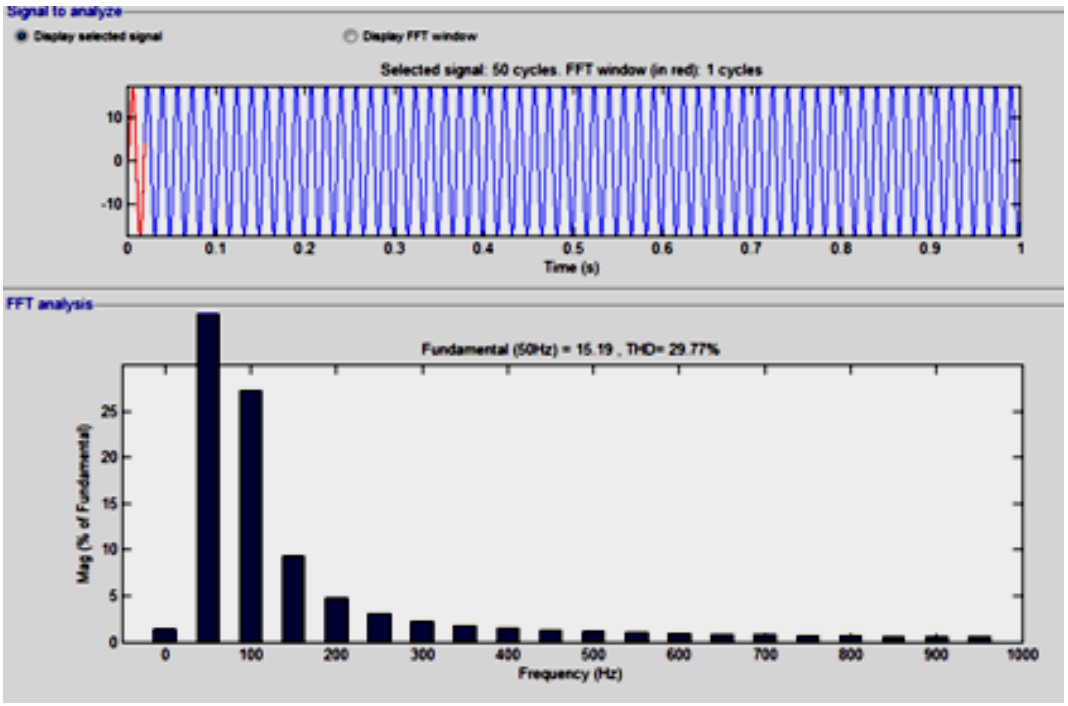


Fig.15: THD of load current for multi-level inverter

Comparison Table of the THD of the Load voltage and Load current between proposed and extension Methods

System Parameters	**three level** (total harmonic distortion)	**Multi-level** (total harmonic distortion)
Load Voltage	1.70%	0.34%
Load Current	38.23%	29.77%

unmistakably the aggregate consonant mutilation (THD) will be decreased contrasted with proposed technique and augmentation strategy that is the heap voltage in proposed technique is 1.70% that is lessened to 0.34% in extension technique in like manner the heap current in proposed strategy is 38.23% that is likewise diminished to 29.77% in view of the we utilize multi-level (5Level) inverter set up of the MVSI inverter. We utilize multilevel inverter set up of ordinary inverter we build number of levels as a result of that reason we get lessened THD in multilevel inverter we get low THD that implies we get appropriate sine wave in inverter yield. On account of this reason we utilize multilevel inverters set up of typical inverters

Multilevel inverter advantages

- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.
- Total harmonic distortion will be decreased

Advantages of the DVSI Scheme

The different favorable circumstances of the proposed DVSI plan over a solitary inverter plan with multifunctional abilities [7]–[9] are talked about here as takes after:

1) Expanded Reliability: DVSI plan has expanded unwavering quality, because of the lessening in disappointment rate of parts and the decline in framework down time cost [13]. This decreases the lost vitality and subsequently the down time cost. The decrease in framework down time cost enhances the unwavering quality.

2) Diminishment in Filter Size: In DVSI plan, the current supplied by every inverter is lessened and subsequently the present rating of individual filter inductor decreases. This diminishment in current rating lessens the filter size. Since the lower current evaluated semiconductor gadget can be exchanged at higher exchanging recurrence, the inductance of the filter can be brought down. This reduction in inductance further decreases the filter size.

3) Enhanced Flexibility: Both the inverters are nourished from isolated dc joins which permit them to work freely, in this way expanding the flexibility of the framework.
4) Better Utilization of Microgrid Power: DVSI plan uses full limit of MVSI to exchange the whole power produced by DG units as genuine energy to air conditioning transport, as there is AVSI for symphonious and receptive force remuneration. This builds the dynamic force infusion capacity of DGs in microgrid.
5) Lessened DC-Link Voltage Rating: Since, MVSI is not conveying zero arrangement load current parts; a solitary capacitor three-leg VSI topology can be utilized.

CONCLUSION

A three level inverter is replaced with multilevel inverter in DVSI scheme to increase power quality and reliability of Microgrid by decreasing THD. With a five level inverter we increasing levels of inverter to get pure sinusoidal wave by reducing THD percentage, and also it improves efficiency of system. Control alg-orithims are developed to operate DVSI scheme in grid sharing and grid injected mode. when compare to proposed method the multilevel inverter has an advantages of all the phases share a common dc bus, which minimizes the capacitance requirements of the converter, the capacitors can be pre-charged as a group, efficiency is high for fundamental frequency switching, total harmonic distortion will be decreased. On account of this reason we utilize multilevel inverters set up for typical networks.

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