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Design and Development of Programmable Pulse Generator using CPLD

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Abstract

Pulse generators use digital techniques, analog techniques or combination of both to form output pulse sequences. Simple pulse generators usually allow control of pulse repetition rate (frequency), pulse width and high and low voltage levels of the pulses. Sophisticated pulse generators may allow control over the rise and fall times of the pulses along with waveform parameters (frequency, amplitude and pulse width), which will decide the shape of the output, pulse sequence.

Pulse generators can be of two types (i) programmable and (ii) non-programmable. The programmable pulse generators are software controlled and non-programmable ones are hardware controlled. The hardware controlled pulse generators have fixed modes of operation. The software controlled pulse generators are more flexible and their modes of operation can be changed easily.

Here we developed a programmable Pulse generator system to produce pulse sequences with variable pulse widths, pulse repetition and height to be used in Deep Level Transient Spectroscopy (DLTS) for characterizing the deep levels in semiconductor materials/junctions. The Pulse generator has been developed using CPLD. The advantage of our Pulse generator is it produce pulses with sharp rise and fall times (<10 ns) with variable pulse width and height. We used VHDL to develop the program. The details of the design and development of the Pulse generator is discussed in the paper. The pulse widths can be varied from 0.048 mS to 68 mS, pulse repetition time from 0.08 mS to 88 mS and pulse height from 1V to 4V.

Keywords: DLTS, CPLD, Macro cells, Programmable inter connect array.

Introduction

A variety of pulse generators are available commercially. The software controlled pulse generators are more flexible and their modes of operation can be changed easily. The aim of the present work is to develop a programmable pulse generator in the laboratory using CPLD devices, which belongs to MAX3000A family – (EPM3128-144-10). This pulse generator is proposed to be used in the Deep Level Transient Spectroscopy system (DLTS) that has been developed in our laboratory. It has been developed to produce pulses with sharp rise and fall times (<10 ns) with variable pulse width and height. The software used for programming the CPLD is VHDL.

In DLTS experiment, a semiconductor diode is normally kept under reverse bias and a positive pulse is applied for a short duration to bring the diode under forward bias. When the diode is under forward bias, the charge carriers occupy deep traps in the band gap of the semiconductor. When the forward bias is removed, the charge carriers will emit back to the respective conduction/valence bands. As a result, the junction capacitance changes with time. By measuring the junction capacitance as a function of temperature, the trap parameters such as activation energy, capture cross-section, trap density etc., can be determined. The present pulse generator is required to apply forward bias to the device and to produce sampling pulses to acquire our data corresponding to the capacitance signal.

The pulse generator has been developed using VHDL software, the hardware descriptive language and the CPLD/FPGA programming system supplied by Silicon Micro Systems, Bangalore that is interfaced to a PC. The VHDL language has been used since it is a powerful tool to synthesize, analyze and simulate the software needed to program the CPLD, which produces the pulse sequences.

Pulse Generator Hardware

The software for the pulse generator system has been developed in VHDL language, and is synthesized, analyzed and compiled, before downloading into the CPLD on CPLD/FPGA programming system connected to parallel port of a PC. The CPLD on UVLSI system is interfaced to digital-to-analog converter . The DAC output is connected to level shifter and amplifier circuit to produce an output of desired amplitude and pulse width.

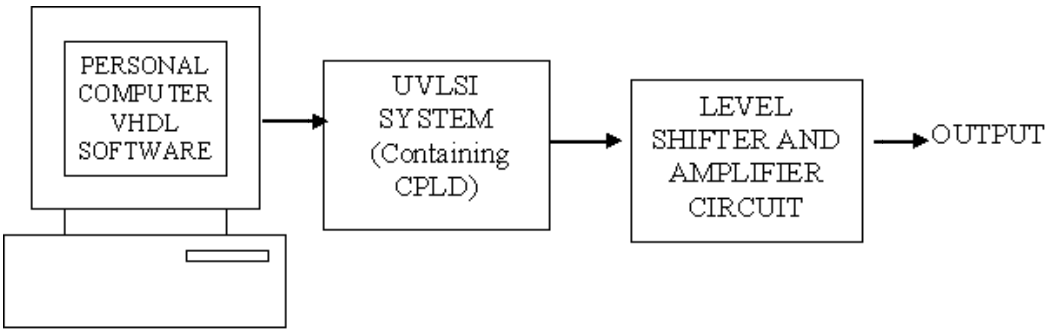

Figure 1: Block Diagram of Pulse generator.

The VHDL

The VHDL is a hardware description language intended for modeling digital systems ranging from a small to large systems. VHDL stands for very high-speed integrated circuit hardware description language. VHDL is standardized by IEEE (Institute of Electrical and Electronics Engineers) and is known as VHDL-1076. Any digital systems can be designed in VHDL using structural, dataflow, behavioral or mixed models.

Attractive Features of VHDL

- The language supports flexible design methodologies (top down, bottom-up, flat).
- It supports both synchronous and asynchronous timing models.
- It is an IEEE and ANSI standard, and the models described using VHDL is portable.
- VHDL is independent of used technology but is capable of supporting technology specific features.
- The language has elements like components, functions, procedures and packages that make large-scale design modeling easier.
- Arbitrarily large designs can be modeled using the language, and there are no limitations imposed by the language on the size of the design.
- Models written in this language can be verified by simulation since precise simulation semantics are defined for each language construct.
- The capability of defining new data types provides the power to describe and simulate a new design technique at a very high level of abstraction without any concern about the implementation details.
- For the above reasons VHDL has become powerful tool to design digital systems.

The General Architecture of Max 3000A CPLD

The high density CPLD contains macro cells that are interconnected through PIA. This type of architecture provides high speed and predictable performance. These are EPROM based devices i.e., the devices store the program and also their configuration even when power is switched off. It is having in system programmability pin-to-pin delays as fast as 4.5ns. It works with a frequency up to 227.3MHZ. It has pin count of 144 AND package is thin quad flat pack (TQFP). It has configurable expander product terms per macro cells. The EPROM based MAX 3000A (EPM 3128 144-10), devices operate with a 3.3V supply voltage.Architecture of MAX 3000A consists of

- Logic array blocks(LABs)
- Macrocells
- Expander product terms
- Programmable inter connect array (PIA)
- I/O control blocks.

Logic Array Blocks (LAB)
A logic cell is the smallest unit of logic in a Logic array block (LAB) and is called Logic element. A Programmable Array Logic (PAL) like block consists of 16 macrocell arrays. Multiple LABS' are linked together via the Programmable Interconnect Array (PIA) which is a global bus that is fed with all dedicated I/O pins and macrocells. Each LAB is fed with 36 signals from PIA for general logic inputs and global controls.

Macrocells
The macro cells in MAX 3000A, EPM 3128-144-10 can be individually configured for either sequential or combinational operation. Each macro cell consists of three functional blocks: logic array, product-term select matrix and programmable register. Combinational logic is implemented in the logic array, which provides five product terms per macro cell. The product-term select matrix allocates these product terms for use as either primary logic inputs to implement combinational functions or as secondary input to the macro cell's to implement register preset, clock and clock enable control functions.

***Expanded Product Term*s**
The most of logic functions can be implemented with the five product terms available in each macro cell. Highly complex logic functions require additional product terms. Sharable and parallel expander product terms have been provided in MAX 3000A such that additional product terms can be directly connected to any macro cell in the same LAB. These expanders help ensure that logic is synthesized with a fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders
Each LAB has 16 sharable expanders that can be viewed as pool of uncommitted single product terms with inverted outputs that feed back into the logic array. Each sharable expander can be used and shared by any or all the macro cells in the LAB to build complex logic functions

Parallel Expanders
Parallel expanders are unused product terms that can be allocated to a neighboring macro cell to implement fast complex logic functions. Parallel expanders unto 20 product terms can directly feed the macro cell or logic, 5 product terms from the macro cell and 15 product terms provided by the parallel expanders from neighboring macro cells in the LAB.

Programmable Interconnect Array (PIA*)*
Logic is routed between LABs via the PIA. PIA is a global bus and is a programmable path that connects any signal source to any destination on the device. All MAX 3000A CPLDs/FPGAs dedicated inputs, I/O pins and macro cell outputs are connected to the PIA, and hence the signals are available throughout the device. The

PIA is used to predict the design timing performance of the MAX 3000A CPLDs/FPGAs.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output or bi-directional operation. All I/O pins have tri-state buffers that are individually controlled by one of the global output enable signals or directly connected to the ground or VCC. The I/O control block has 6 or 10 global output enable signals. When tri-state buffer control is connected to the ground, the output is tri-stated, and I/O pin can be used as a dedicated input. When tri-state buffer control is connected to VCC the output is enabled. The MAX3000A architecture provides dual I/O feed back, in which macro cell and feedback pins are independent.

Level Shifter and Amplifier Circuit

The level shifter has been implemented for shifting the low and high voltage levels of the pulses in a sequence and amplifier circuit is for adjusting the pulse amplitude according to the requirement. The op-amp IC CA3140E is a BiMOS operational amplifier. It provides very high input impedance, very low input current and high-speed performance. This operational amplifier is internally phase compensated to achieve stable operation in unity gain follower operation. It provides amplitude adjustment. The output of the op-amp is a pulse with desired amplitude. The pulse width is software programmable.

Experimental Results

The pulse repetition selection, width selection, height selection are shown in tables 1, 2, 3.

Table 1

Pulse repetition selection input (p_rep_sel)	Output pulse repetition time (msec)	DAC clock
00000000001	88	Count(0)
00000000010	44	Count(1)
00000000100	22	Count(2)
00000001000	11	Count(3)
00000010000	5.5	Count(4)
00000100000	2.7	Count(5)
00001000000	1.35	Count(6)
00010000000	.68	Count(7)
00100000000	.34	Count(8)
01000000000	.17	Count(9)
10000000000	.08	Count(10)

Table 2

Width Selection (W_h_sel)	Pulse width (sec)		Count value
	Min	Max	
00	80u	88m	256
01	56u	62m	300
10	52u	56m	350
11	48u	52m	400

Table 3

Height selection (w_h_sel)	Height count (hgt)	Pulse height (volts)
00	490	4
01	430	3
10	370	2
11	310	1

Conclusion

A programmable pulse generator has been designed and developed using CPLD/FPGA programming system. The pulse generator system has been constructed using MAX 3000A device (EPM 3128 144-10), and IC CA3140E.

The pulse width can be varied from 0.048 msec to 68 msec pulse repetition time from 0.08 msec to 88 msec and pulse height from 0 to 4V. The pulse rise and fall times are of the order of 10 nsec. This pulse generator has been designed and developed to use in the Deep Level Transient Spectroscopy (DLTS) system. The necessary software has been developed in VHDL.

Future Plan of Work

It is proposed to generate pulse sequences < 10 nsec, since such pulses are required in DLTS system to measure the capture cross – section of the traps.

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