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Sleepy Keeper Approach for Power Performance Tuning in VLSI Design

K. Gnana Deepika, K. Mariya Priyadarshini and K. David Solomon Raj

Department of Electronics and Communication
Andhra Loyola Institute of Technology
gnanadeepika423@gmail.com
Department of electronics and communication
S.R.K. Institute of Technology
mariyapriyadarshini@gmail.com
Department of Avionics, JNTU Kakinada
raju.f22@gmail.com

Abstract

There are several techniques that reduce leakage power in efficient way but the disadvantage of each technique limits the application of each technique. In this paper sleepy keeper approach is introduced to reduce the power dissipation of the circuit in idle state when its logic is not needed. The sleepy keeper approach uses traditional sleep transistors and two additional transistors which are driven by already calculated gate output. This saves the state during sleep mode. Multi threshold transistors are used in order to reduce subthreshold leakage power and also to increase the switching speed of the circuit.

Key words- Leakage power, subthreshold leakage currents, sleep mode, idle mode.

I.INTRODUCTION

For the most recent CMOS feature sizes, leakage power dissipation has become an overriding concern for low power VLSI designers. When the threshold is scaled down the transistors turn on even for lower swing input signals creating a short circuit path between power supply and ground. One of the main reasons for increase in leakage power is sub-threshold leakage power which occurs because of subthreshold drain currents and the tunneling currents.

Sub threshold drain current is the current that flows from source to drain when the transistor is in weak- inversion region i.e. when gate to source voltage is below the threshold voltage. Tunneling currents are the currents that flow through the oxide when it is made thinner. The following figure shows the different leakage currents that flow across MOSFET.

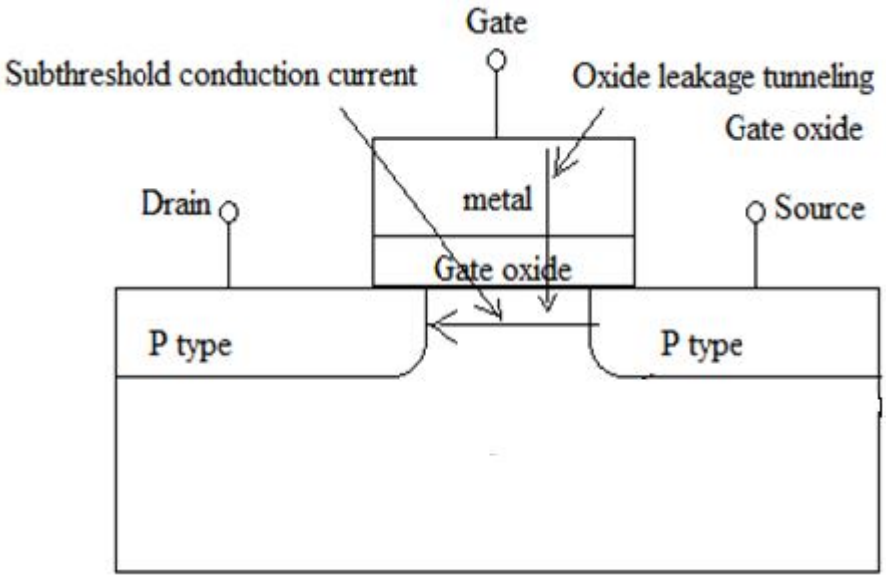

Figure.1 Different types of leakage currents in MOSFET

In order to design high density high performance CMOS devices the transistors feature size is reduced which results in exponential increase of leakage power. Therefore we can say leakage power dissipation has become a significant portion of total power consumption for current and future silicon technologies. One of the most popular approaches to leakage power reduction relies on the insertion of sleep transistors which are placed between the ground (or Vdd) terminal of the gates and the ground (or Vdd) distribution network. the sleep transistors are turned off during sleep mode, and the source nodes of the gates in the functional block float, thus cutting off the leakage path to the ground.

In general, the source voltage should be raised as much as possible to achieve a maximum leakage reduction. On the other hand, in order to preserve the state of the cells in the standby mode, this voltage must not exceed a certain level. Also, with the technology scaling down to smaller geometries, the exacerbated variation of device parameters causes a significant die-to-die and within-die variation in the stability of the cells. The within-die variation results in cells which have different hold stabilities even on a single chip.

This technical paper presents a new approach for low leakage power, Very Large Scale Integrated Circuits. This includes test procedures with schematics for all considered approaches.

II.RELATED WORK

The Power consumed in high-performance microprocessors has increased to levels that impose a fundamental limitation to increasing performance and functionality [1]–[3]. A dual threshold voltage circuit technique was proposed in [4] for reducing the subthreshold leakage energy consumption of domino logic circuits. The technique proposed in [4] utilizes both high and low threshold voltage transistors. High threshold voltage transistors are employed on the noncritical precharge paths. Alternatively, low threshold voltage transistors are employed on the speed critical evaluation paths. The energy and delay overhead for entering and leaving the sleep mode, however, has not been addressed in [4].

In [5], a dynamic sleep transistor technique has been introduced in which an accurate fine-tuning of the cell bias voltage is achieved, but it is not able to dynamically adapt to run-time variations in temperature and voltage. A variation of the sleep approach, the zigzag approach, reduces wake-up overhead caused by sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected input vector [6]. With application of dual threshold voltage (Vth) techniques, the sleep, zigzag and sleepy stack approaches result in orders of magnitude subthreshold leakage power reduction [7].

In this paper, a new leakage reduction technique, which we call the "sleepy keeper" approach, is discussed. The following sections explain the structures of different leakage reduction techniques along with the sleepy keeper approach as well as how it operates.

III. PREVIOUS TECHNIQUES

In case of sleep approach, transistors gating V_{dd} and GND are added to the base case. The added transistors cut off supply of power when in sleep mode. Each added transistor is referred to as "sleep transistor" and takes the width of the largest transistor in the base case. A PMOS transistor is placed between V_{dd} and the pull up network, and NMOS sleep transistor is placed between GND and pull down network.

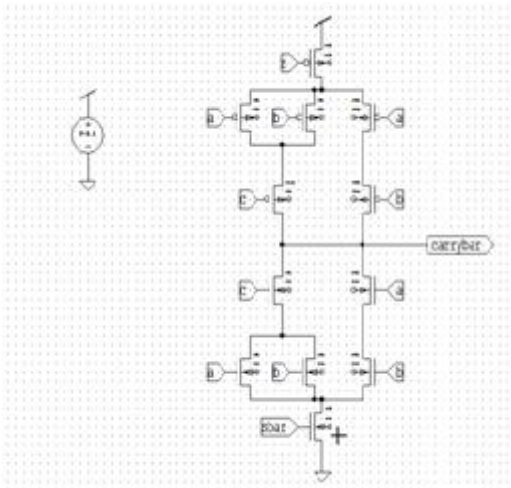

Fig.2. Carry Logic Using Sleep Approach

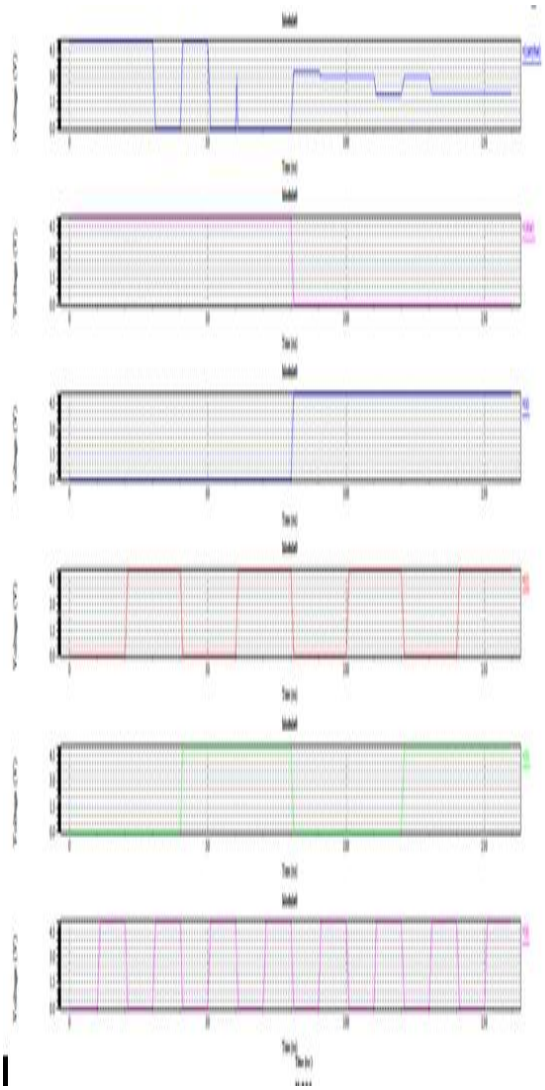

Fig.3 waveform of inverted carry logic using sleep approach

The disadvantage in sleep approach is destruction of state and floating outputs which can be observed in the first wave from the above waveforms.

In stack approach every transistor in basic carry logic network using CMOS logic is duplicated with both original and duplicate bearing half the original transistor width. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because subthreshold current is exponentially dependent on gate bias, a Substantial current reduction is obtained. As all transistors are placed in between two parallel rows of continuous V_{dd} and GND, stack approach design forces an increase in row length because of an increase in number of transistors and decrease in transistor width.

The following circuit shows the implementation of inverted carry logic of a full adder using stack approach.

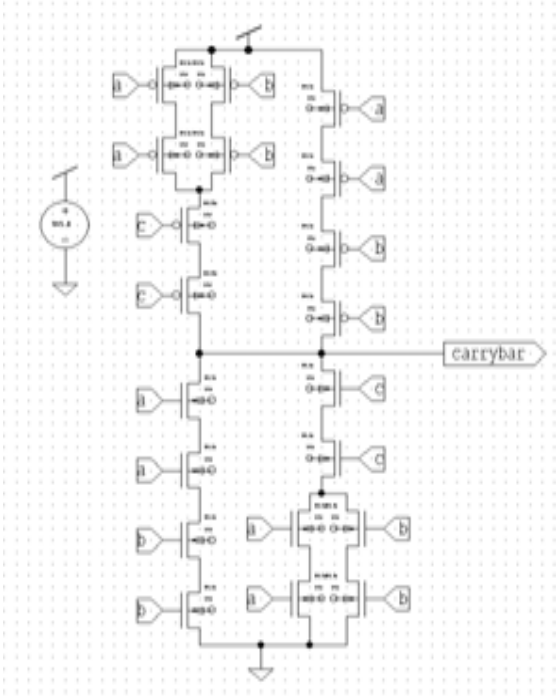

Fig.4 inverted carry logic using stack approach

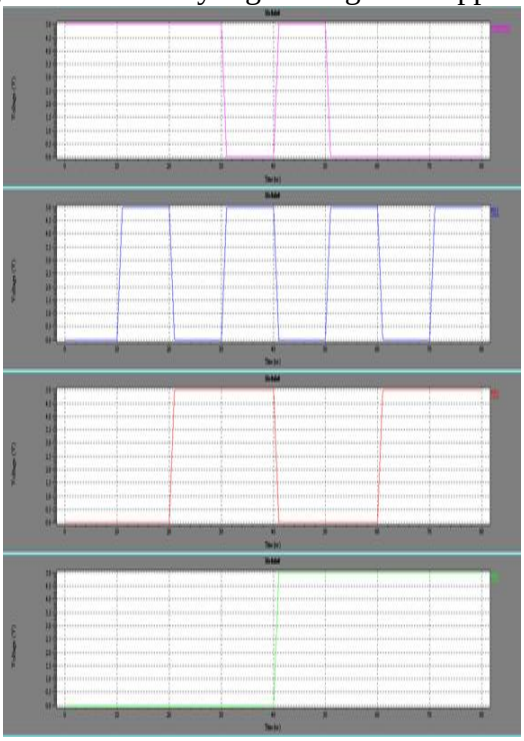

Fig.5 waveform of inverted carry logic using stack approach

Even though state saving is done in stack approach delay is increased because of duplication of transistors

The sleepy stack approach has a structure combining the stack and sleep approaches by dividing every transistor into two half width and placing a sleep transistor in parallel with one of the divided transistor. Sleep transistors are placed in parallel to the divided transistor closest to V_{dd} for pull-up and in parallel to the divided transistor closest to GND for pull down. The sleepy stack approach can have advantages of both the stack approach and the sleep approach. During the active mode, the sleepy stack approach results in lower delay than the stack approach because sleep transistors placed in parallel reduce resistance and are already on. The following figure shows the inverted carry logic using sleepy stack approach.

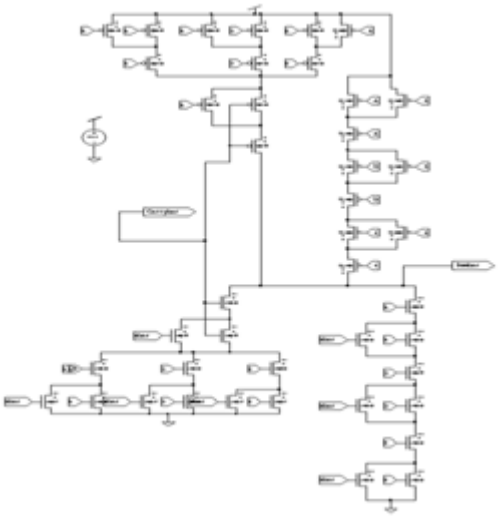

Fig.6 Inverted carry logic using sleepy stack approach

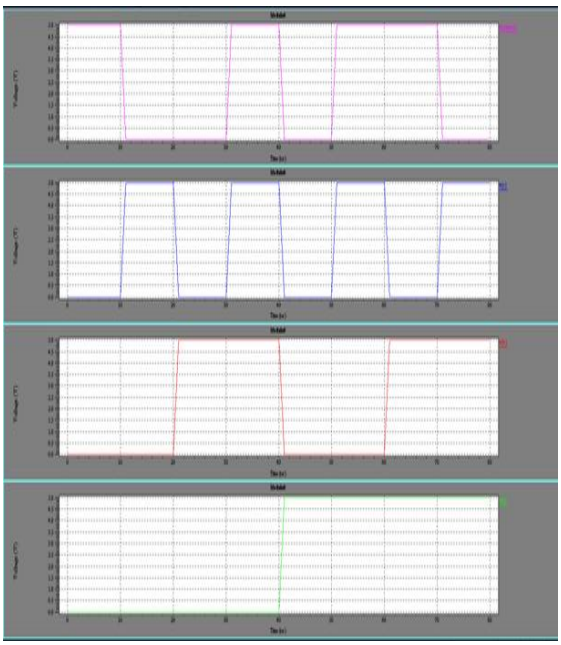

Fig.7. waveform of inverted carry logic using sleepy stack approach

The above approach reduces dynamic power and the output voltage levels stay in the defined ranges of logic-1 and logic-0, but circuit complexity increases as the number of transistors increase which also increases the area.

The zigzag approach reduces wakeup overhead delay caused by the sleep transistors, by placement of alternating sleep transistors based on which the particular network (pull up or pull down) is off given a specific input vector. In order to evaluate this approach, the result of static power dissipation for all zero inputs is chosen for comparison with other approaches because the reset values are typically all zeros in most cases. In addition to this, the threshold leakage can further be reduced by using high threshold voltage sleep transistors. The reduced number of sleep transistors in this zigzag approach results in smaller increase in area than by using the sleep approach.

The disadvantages in zigzag approach are to estimate the pre scaled vectors for sleep transistors, and output voltage levels will be floating.

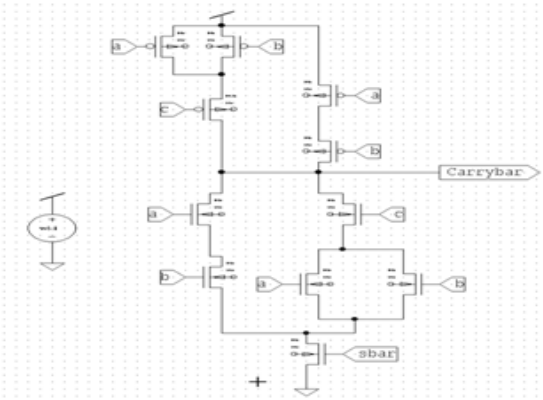

Fig.8 Inverted carry logic using zigzag approach

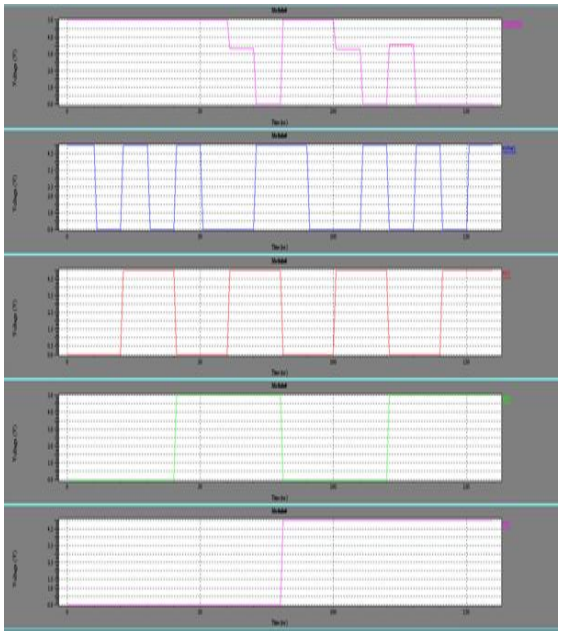

Fig.9 waveform showing floating output in zigzag approach.

The leakage feedback approach is based upon the sleep approach it uses two additional transistors to maintain the logic state during the sleep mode and the two transistors are driven by the output of an inverter which is driven by the output of the circuit implemented utilizing the leakage feedback. A PMOS transistor is placed in parallel to the sleep transistor and a NMOS placed transistor is placed in parallel to the sleep transistor. During the sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with appropriate power rail.

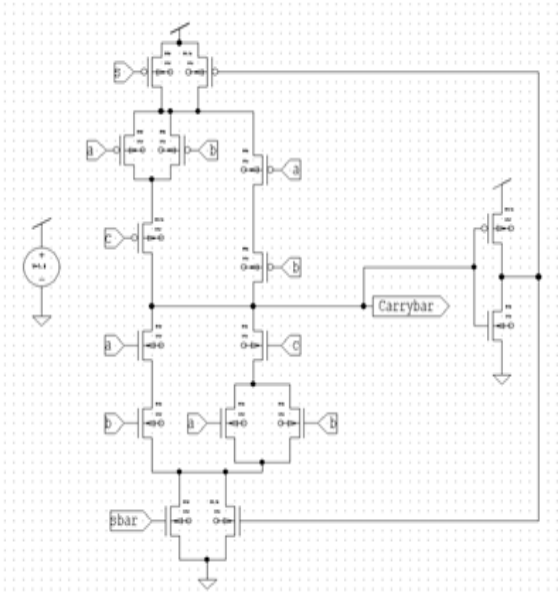

Fig.10 Inverted carry logic using Leakage Feedback approach

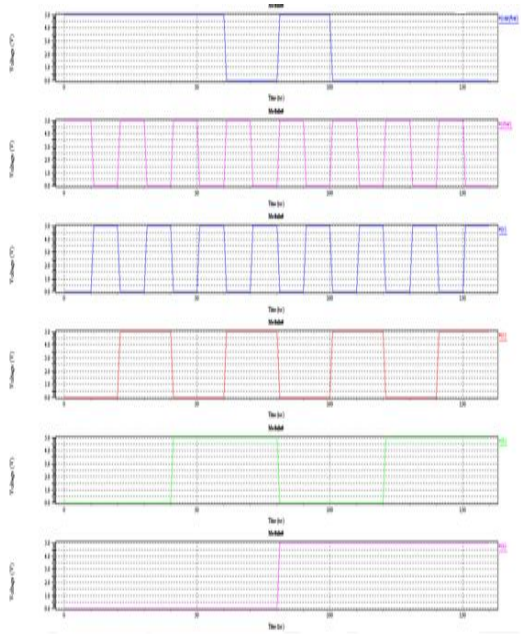

Fig.11. waveform of inverted carry logic using leakage feedback approach

The leakage feedback method increases the area and leakage current flows across the static CMOS inverter connected in the feedback path.

IV.PROPOSED TECHNIQUE

In this section a solution against all the drawbacks in the previous techniques is presented. This is a new leakage reduction technique which we call the sleepy keeper.

The basic problem with traditional CMOS is that the transistors are used only in their most efficient and natural inverting way. That is PMOS transistor is connected to V_{dd} and NMOS transistor is connected to GND. It is well known that PMOS transistors are not efficient at passing GND. Similarly it is well known that NMOS transistors are not efficient at passing V_{dd}. however to maintain the value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor is connected to V_{dd} to maintain output value equal to '1' when in sleep mode.

As shown in figure, an additional single NMOS transistor placed in parallel to pull-up sleep transistor connects V_{dd} to pull up network. When in sleep mode, this NMOS transistor is only source of V_{dd} to the pull-up network since the sleep transistor is off.

Similarly to maintain a value of '0' in sleep mode, given that the '0' value has already been calculated, the sleepy keeper approach uses this output value of '0' and PMOS transistor connected to GND to maintain output value equal to '0' when in sleep mode. As shown in figure, an additional single PMOS transistor placed in parallel to the pull-down sleep transistor is only source of GND to the pull-down network which is the dual case of the output '1'.

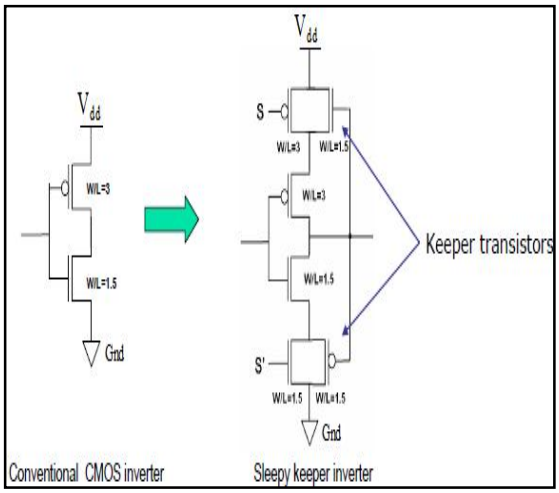

Fig12. Sleepy keeper for CMOS inverter

The following circuit shows inverted carry logic using sleepy keeper approach.

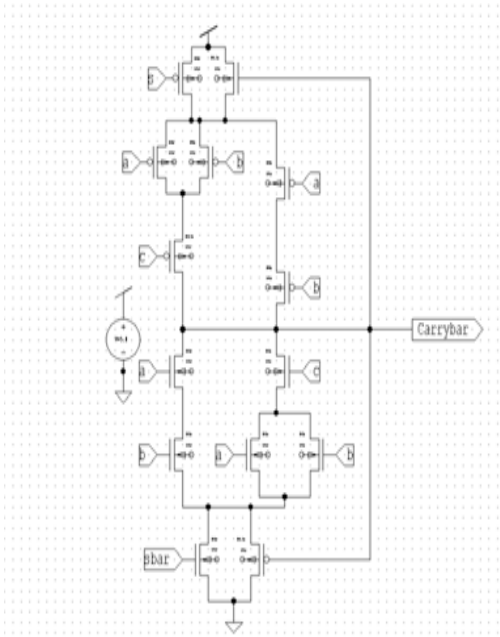

Fig.13.Inverted carry logic using sleepy keeper approach

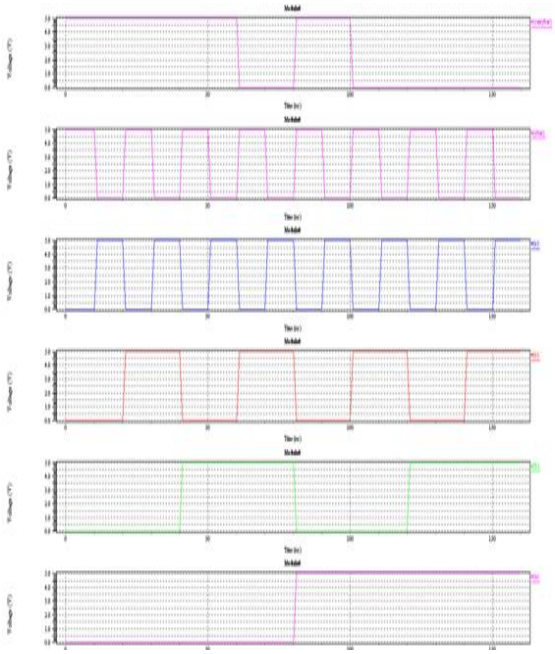

Fig.14 Waveform of inverted carry logic using sleepy keeper approach

For this approach to maintain proper logic NMOS is to be connected to V_{dd} and the PMOS connected to the GND.

The following table shows the comparison between the previous techniques and the proposed technique of the paper. We observe dynamic power static power is reduced along with the leakage power.

Table.1 Power values for Different Techniques

Techniques	Static power (watts)	Dynamic power (watts)	Leakage power (watts)
Static CMOS logic	3.52n	1.57m	153.5p
Sleep approach	1.512n	1.00m	69.7p
Stack approach	3.18n	434u	71.2p
Sleepy stack	17.9n	150.002u	94.1p
Zigzag approach	2.31n	470u	97p
Leakage feedback	2.145n	1.27m	1.15517p
Sleepy keeper	657p	720.002u	96.7p

Table.2 Power delay product values for Different Techniques

Techniques	Total power dissipated (watts)	Delay (sec)	Power Delay product
Static CMOS logic	1.57003m	1.0214×10^{-5}	16.3×10^{-9}
Sleep approach	1.00158m	$2.68\text{x}10^{-15}$	1.38×10^{-12}
Stack approach	434.003µ	$2.90\text{x}10^{-5}$	26.90×10^{-9}
Sleepy stack	150.019 µ	$2.90\text{x}10^{-5}$	4.025×10^{-9}
Zigzag approach	470.024 µ	$2.650\text{x}10^{-5}$	12.45×10^{-9}
Leakage feedback	1.27033m	$1.4\ \text{x}10^{-5}$	30.48×10^{-9}
Sleepy keeper	720.075µ	$0.3\ \text{x}10^{-5}$	2.16×10^{-9}

V.CONCLUSIONS

Though there is a decrease in leakage power in the sleep approach than base case, there is a destruction of state and floating output voltage. In the case of zigzag approach even though state destruction is eliminated floating output voltages still exist. In stack approach because of delay penalty sleepy stack approach is proposed which increases area. So leakage feedback is preferred, but leakages in the feedback network and area penalty are the drawbacks of leakage feedback network. So the proposed technique sleepy keeper is implemented. In case of sleepy keeper approach, static power, dynamic power dissipation and leakage power is reduced when compared with leakage feedback approach. Power delay product is less when compared with all the other approaches.

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