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FPGA Based Phase Computation for Active Phased Array Radar (APAR)

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Abstract

In active phased array radars, the Beam Steering Controller plays a crucial role in directing the antenna beam. It manages the Transmit/Receive (T/R) Modules, which are essential components of advanced phased array radar systems. To generate a beam from multiple radiating elements, each T/R Module must be assigned a calculated phase angle. Common phase gradients are distributed to all Transmit/Receive Controllers, which then calculate the phase values based on the position of each T/R Module in the array.

This paper introduces a time-optimized algorithm for calculating 6-bit phase angles from the phase gradients. It thoroughly discusses the VHDL implementation of the algorithm and its hardware design using FPGA. The implementation utilizes the Xilinx Virtex-5 chip, model XC5xfx70t-1ff1136.

Keywords— Active phased array radar, Digital phase shifter, Plank controller, Transmit/receive modules(T/R modules).

Introduction

Active electronically scanned arrays (AESA) or the **Active Phased Array Radar (APAR)** [1] antennas represents one of the most important developments in radar technology. Electronically steered antenna of this ilk is designed with an individually electronically controlled device behind each antenna element, which can manipulate the time delay or phase of the microwave signal passing through it, i.e each antenna array element has its own transmitter and receiver module, every transmit/ receive element (T/R Module) [2] in an AESA has its own source of radar energy. With a computer controlling each element, the beam direction and its shape could be digitally controlled, within a matter of milliseconds or tens of milliseconds.

As compared to radar which has mechanically steered antenna, AESA-based radars show an unprecedented degree of operational flexibility and are currently on the verge of revolutionising the performance of spaceborne and air as well as naval and ground based radar [3]. The primary advantage of an Active electronically scanned arrays (AESA) over a Passive electronically scanned arrays (PESA) [4] is there is no longer a single point of failure, capability of the different modules to operate on different frequencies, this allows AESA to produce numerous sub-beams and actively paint multiple targets.

Beam Steering Controller

Forming a beam and electronically scanning it over a range of space can be done using an array of antennas with input/outputs that can be phase shifted with respect to one another. To steer the beam formed by the array, an electronically controlled phase shifter is placed immediately behind each antenna element i.e within T/R module. The phase shifter is controlled by a local processor called beam steering controller(BSC).The beam steering controller is an important part of AESA which plays an important role in carrying the phase angle data to all radiating elements. The radiated beam direction and angle is determined by relative phase relationship between adjascent radiating elements [5] [6].The mathematical relationship between phase difference of adjascent radiating elements and radar beam steering angle θ is

$$\Phi = (2\pi\boldsymbol{\lambda}/d) \sin \theta \quad (1)$$

Where $\boldsymbol{\lambda}$ is the radar wavelength = c/f, c is the speed of light= $3x10^8$, f is the radar frequency and d is spacing between adjascent radar elements.The phase shifter within the T/R Module is responsible to form a beam .Phase shifter must be assigned with specific phase shift value.Phase shifters can be analog with continuously variable phase from 0 to 360 or digital with discrete phase steps from 0 to 360 degrees.Digital phase shifters are characterized by their number of bits, for 6-bit phase shifter will have 2^6= 64 levels of adjustments or an adjustment resolution of 5.625 degrees. Δϕ is the phase error compensation value,kept in the FLASH in advance. According to the address provided from radar controller FPGA takes off the concept in FLASH. And then stored in register to take part in the calculation of phase shift value.

There are centralized architecture, distributed architecture for beam steering controller. In the centralized architecture, single controller controls all the T/R Module and performs

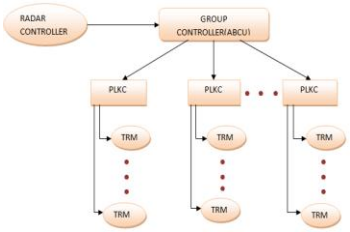


Figure.1. Hierarchical architecture of Beam steering controller

A centralized operation.Centralized architecture is suitable only for passive phased arrays since the array requires only phase control.Distributed architecture is suitable for active phased arrays since it requires both amplitude and phase control [7].
Broadly, the architecture followed by the radar is given above. The Radar Controller serves as the top-most control point.The ABCU (Antenna Beam Steering Unit) receives data from the radar controller in a source synchronous fashion.The data is forwarded to PLKC (Plank Controller), which in turn forwards it to the TRMC (Transmit/Receive Module Controller).Each ABCU can control more than one PLKC, and each PLKC can control more than one TRMC. PLKC provides required data to the individual TRMs.
In this beam steering controller, the calculated 16-bit phase gradients from azimuth and elevation angles are sent to Plank controller (PLKC) at the rate of 50 Mbps from the developed Front end GUI.After receiving the phase gradients, the Plank controller (PLKC) calculate the 6- bit phase values and then broadcasts the 6- bit phase values to 32 TRM at the rate of 20Mbps, send it to the 6-bit digital phase shifters of the TRM. The digital phase shifter converts the 6-bit phase value to the corresponding analog phase value for further beam forming.

6-Bit Phase Angle Calculation from 16-Bit Phase Gradients

Beam steering subsystem receives instruction which comes from radar controller and those information will be command words indicating the two phase gradients (PA, PB). The phase gradients are calculated at the radar controller with the azimuth and elevation angle of the beam to be steered [8]. The two phase gradients are calculated by the following equation

$$PA = (2\pi\boldsymbol{\lambda}/d)*dh*\sin\theta*\cos\phi \quad (2)$$

$$PB = (2\pi\boldsymbol{\lambda}/d)*dv*\sin\theta*\sin\phi \quad (3)$$

Where θ = Azimuth angle in *degrees*
Φ = Elevation angle in degrees
$\boldsymbol{\lambda}$ = Operating wavelength in cm
dh= Horizontal spacing between TRU
Controller in *m*
dv= Vertical spacing between T/R module in *m*

Here PA is calculated for azimuth position and PB is calculated for elevation position.The phase gradients are calculated at ABCU level as decimal values and later converted to binary value.To improve the angular accuracy, calculated values are multiplied by 10 to carry the fraction part of phase gradients.

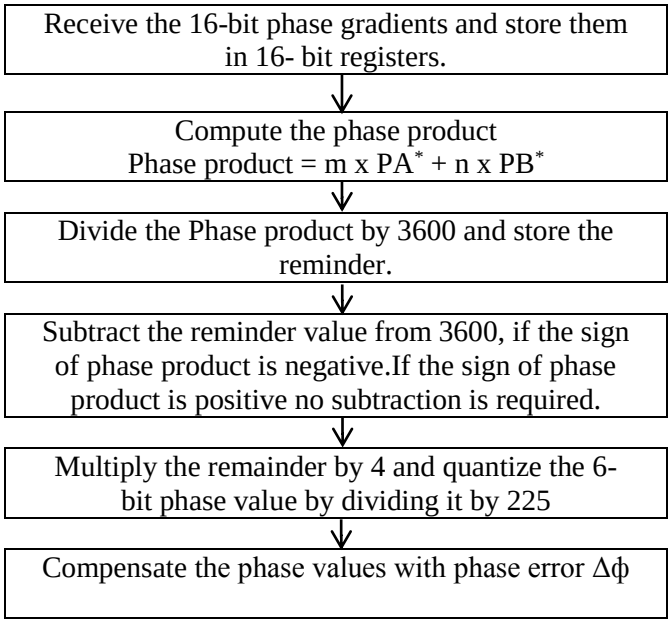
$$PA^* = 10 * PA \quad (4)$$

$$PB^* = 10 * PB \quad (5)$$

Thus a command word of 16-bit with phase gradients
(PA*, PB*) are then forwarded from ABCU to PLKC. The calculation of 6-bit phase value from the two phase gradients is carried out in PLKC. The 6-bit phase value is calculated at each module using the following formula.

$$\textbf{Phase product} = \mathbf{m}\ \mathbf{x}\ PA^* + \mathbf{n}\ \mathbf{x}\ PB^* \quad (6)$$

Where m= plank controller number, n=TRM number, PA^*& $PB^*$are 16-bit phase gradients received from Radar controller. Since the phase gradients are multiplied by 10 at the ABCU level to carry the fraction part of the original phase angle, it is important to divide the phase value by 10 after performing the necessary computation at the Plank controller.The algorithm for calculation of 6-bit phase value from phase gradients in a Plank controller is explained in steps as follows:



Design Aspects

PLKC is designed for beam steering, which includes the calculate board and other control and storage elements for phase value computation [9].It receives command from top level controller, calculate phase value as well as compensate phase value with phase error that is read from flash memory The PLKC design includes SPI protocol for 20 mbps of data communication between upper and lower level controllers via LVDS link.The 100MHz clock is used as reference clock.

Phase computation is the important part carried out by the PLKC using a time optimized algorithm. VHDL implementation of the algorithm requires different submodules of Multiplier, Divider and Adder. Multiplier IP core is used for implementing two 16x6 multiplication. A time optimized division algorithm has been implemented for two division operations. An external flash memory contains the phase error values already.A FIFO (First in first out) module read and stores the value from respective addresses of FLASH according to the control instructions given by the radar controller.This phase error value is not more than 6-bits.

Figure 2. Simulation result for 6-bit phase computation

Simulation Result

The computation of phase value for the first T/R Module is performed as follows. Suppose the 16-bit phase gradients provided to PLKC are

$$PG1 = (10101011000000)_2 = (10944)_{10} = (2ac0)$$

$$PG2 = (10000101001)_2 = (1065)_{10} = (429)$$

$$m = 17 = (11);\ n = 1$$

$$Product = m * PG1 + n * PG2$$

$$= ((11 * 10944) + (1 * 1065))$$

$$= (187113)_2 = (2DAE9)$$

The above value is obtained by the signal vector ‘product1’ in the simulation. A single multiplier IP core is used. The output from multiplier has 23 bits.The output of two multiplication are added and then given for division. Two division operations are performed during the computation of 6-bit phasevalue of each T/R Module. The maximum value of phase product occupies 23 bits. So the dividend is chosen as 23 bits. After computing the product, the resulting value is assigned to‘div_1’signal.

So div_1 =$(10110110101110100 1)_2$.Even though the phase values have to be computed for 32 T/R Modules, only one divider is used in the design to reduce the number of slices occupied in FPGA. So the division is performed one by one for all the 32 T/R Modules starting Fig.3. Simulation result for 6-bit phase computation from T/R Module 1.A time optimized division algorithm has been used for this purpose. A common dividend is used which assigns values one after the other as soon as the division is completed.3 The div_1 value is first taken and it is divided by ‘div_2’. The aim of this division is to reduce the phase value within 3600.

$$\text{div\_1} = (187113)_{10}$$
$$= (101101101011101001)_2$$
$$= (2DAE9)$$
$$\text{div\_2} = (3600)_{10}$$
$$= (111000010000)_2 = (E10)$$

The reminder of the above division operation div_1/div_2 is considered for further manipulation.The remainder is $(110110111001) = (3513)_{10}$ = DB9. In the simulation result, the signal **'remd'** represents the reminder resulting from the first division. Since the phase gradients are multiplied by 10 in the front end GUI, the values are divided by 3600 at Plank controller. The other reminders are calculated one by one and they are stored in separate registers.

In the second division process, the divisor is taken as 56. This division aims at finding the 6-bit phase value of a T/R

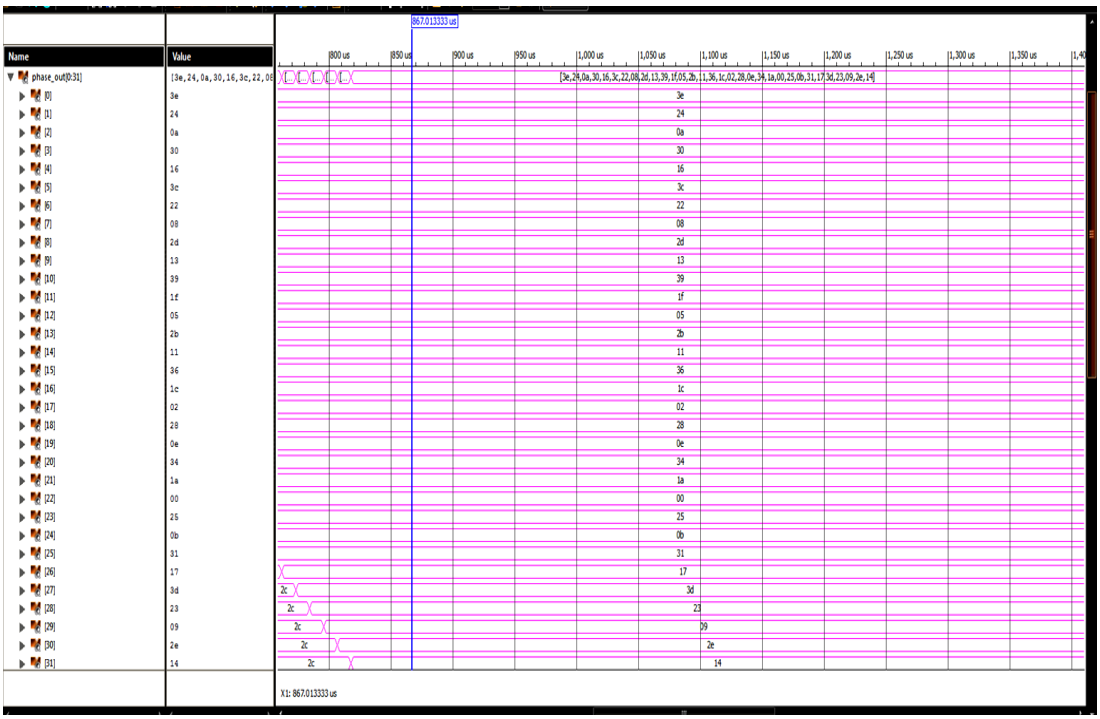


Figure 3. Phase computed for 32- TR modules

Module by quantizing the phase value. A 6-bit phase shifter attached to each T/R Module, 64 combinations of bits, representing different phase value can be given as input to each T/R Module.The 6-bit input "000001" represents 5.625º and the combination "111111" is for 354.375º. The 6-bit phase can be obtained by dividing the phase values by 5.6º. The first division possess remainder value below 3600º.To reduce the phase values within 360º, the reminder values are divided by 56 thereby quantize the phase value to 6-bit. In order to improve the resolution of phase value the numerator and denominatorof second division are multiplied by 4.Thus second division is done by 225.

$$\text{div\_1} = (\text{remd} * 4) = (14052)_{10}$$
$$= 36e4 = (11011011100100)_2$$
$$\text{div\_2} = (225)_{10} = E1 = (11100001)_2$$
$$\text{Phase\_out} = \text{div\_1} / \text{div\_2} = (62)_{10}$$
$$= 3E = (111110)_2$$

The phase angle to be steered by the T/R Module1 can be done by assigning the digital phase shifter with a value $(111110)_2$ .The output bit vector **'Phase-out'** will be the input to digital phase shifter of T/R Module1. In a similar fashion as stated above, the phase values of other T/R Modules can be calculated. The total time taken for computation of 6-bit phase values for all the T/R Modules is 10 microseconds.

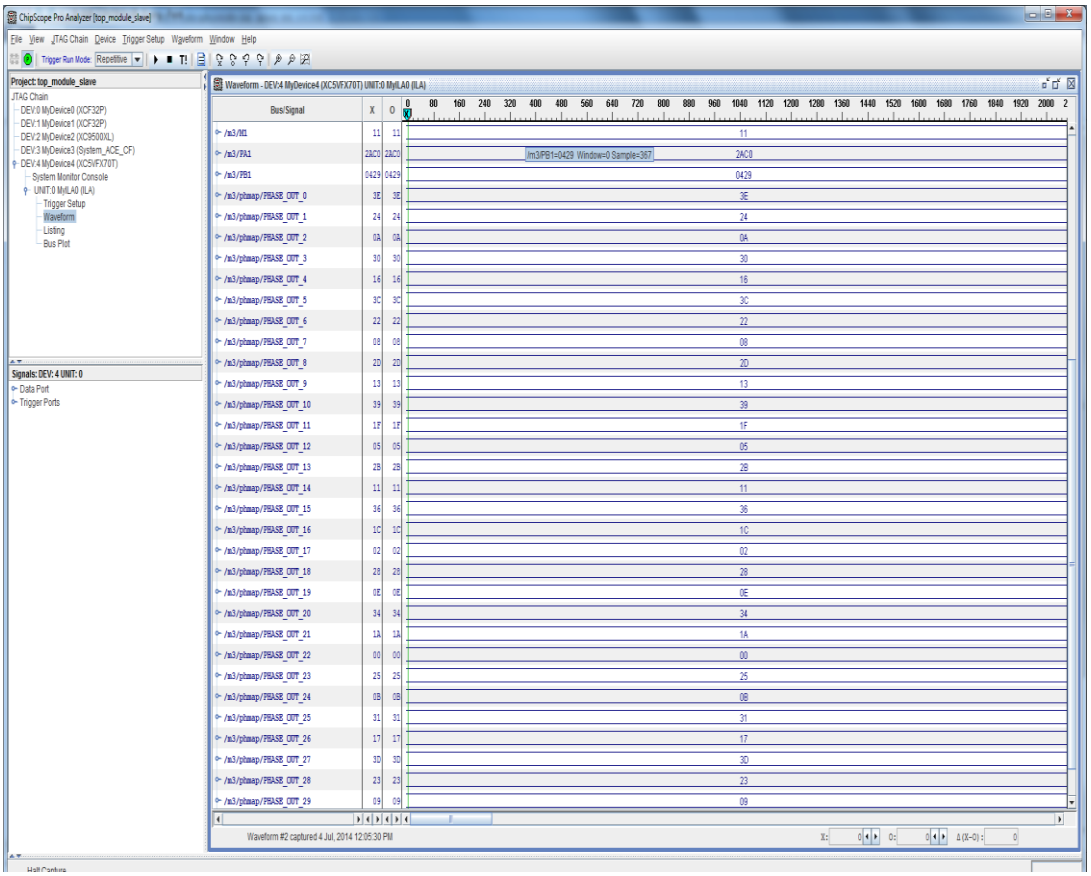


Figure.4.Hardware result

Hardware Implementation

The hardware implementation of the PLANK controller design was done with Xilinx Virtex-5[10] .Two multiplier logic core in this chip were used in the design.The chip had a crystal oscillator of 100-MHz oscillator and is powered by the 3.3V supply. The user constraints File (UCF) was created to assign 25 pins for forwarding data towards 32 T/R Modules.

1) Synthesis Report

Table 1. Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of slice registers	702	44800	1%
Number of slice LUTS	417	44800	0%
Number of fully used LUT-FF pair	273	846	32%
Number of bonded IOBs	234	640	36%
Number of BUFG/BUFCTRLS	1	32	3%
Number of DSP48Es	1	128	0%

2) Hardware Debugging Report

Chipscope resut of phase computed for 32 T/R Modules represented as phase_out [0:31] in the Waveform given in the **Figure.4**.

CONCLUSION

An efficient PLANK controller design for active phased array radars must offer high speed beam switching from one direction to another and an appropriated angular accuracy that affects the improvement of the radar detection.In this design a time optimized method has been put forward to improve the beam switching efficiency. By employing the proposed method the beam switching is achieved in microseconds.Angular accuracy has been improved by taking in multiplied by 10 value ,to carry the fraction part of phasegradients.VHDL firmware is optimized for the application. FPGA based solutions enable the use of new architectural concepts, without the constraints forced by standard devices.The system can be made more effective in future improving the angular accuracy by taking in multiplied by 100 value of the phase gradients.

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