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# Detection of Bare PCB Defects by using Morphology Technique

**Ms. Nadaf F.B.[1] and Mr. V.S. Kolkure[2]**

*Department of Electronics Engineering,*
*Bharat Ratna Indira Gandhi College of Engineering, (Solapur University),*
*Kegaon, Solapur Maharashtra, India.*

**Abstract**

A Printed Circuit Board (PCB) consists of circuit with electronic components mounted on surface. There are three main steps involved in manufacturing process, where the inspection of PCB is necessary to reduce the defects printing, components fabrication over the PCB surface and components soldering. Inspection of PCB can be done by two methods human inspection and machine inspection. Machine inspection is an approach used to counter difficulties occurred in human's manual inspection that can eliminates subjective aspects and then provides fast, quantitative, and dimensional assessments. Machine Vision PCB Inspection System is applied at the first step of manufacturing, i.e., the making of bare PCB. We first compare a standard PCB image with a PCB image to be inspected, using a simple subtraction algorithm that can detect the defected regions. Our focus is to detect defects on printed circuit boards. Typical defects that can be detected are over etchings (opens), under-etchings (shorts), holes etc.

**Keywords:** Machine vision, PCB defects, Image subtraction, PCB inspection.

## I. INTRODUCTION

Visual inspection is generally the largest cost of PCB manufacturing. It is responsible for detecting both cosmetic and functional defects and attempts are often made to ensure 100% quality assurance for all finished products. There are different algorithms are developed for PCB defect detection. Contact method tests the

connectivity of the circuit but is unable to detect major flaws in cosmetic defects such as mouse-bite or spurious copper and is very setup-sensitive [4]. Any misalignment can cause the test to fail completely. Non contact methods can be from a wide range of selection from x-ray imaging, ultrasonic imaging, thermal imaging and optical inspection using image processing [5 - 8]. These systems have advantage over human inspection in which subjectivity, fatigue, slowness and high cost is involved.

In order to reduce cost spending in manufacturing caused by the defected bare PCB, the bare PCB must be inspected. Moganti et al. (1996) proposed three categories of PCB inspection algorithms: referential approaches, non-referential approaches, and hybrid approaches.

- Referential approaches consist of image comparison and model-based technique.
- Non-referential approaches or design-rule verification methods are based on the verification of the general design rules that is essentially the verification of the widths of conductors and insulators.
- Hybrid approaches involve a combination both of the referential and the non-referential approaches.

## II. MATERIAL AND METHODS

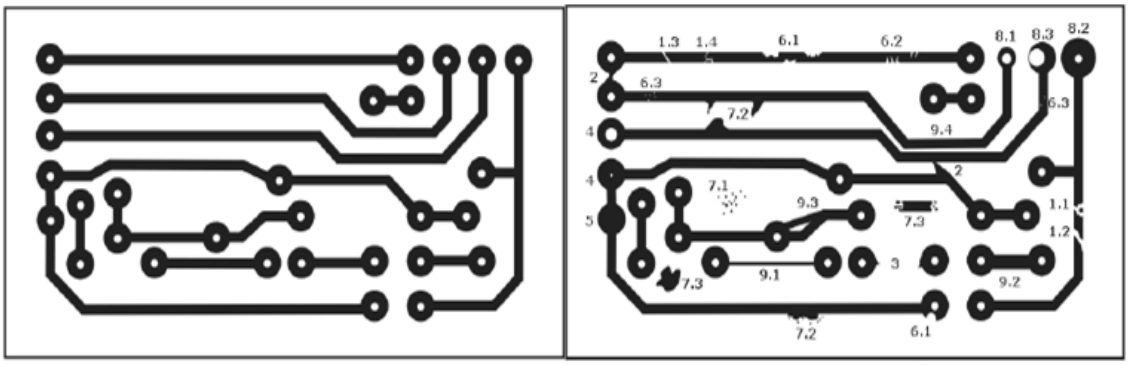
During the manufacturing there are some defects commonly found on PCB. These defects are divided into two categories, potential and fatal defects. Short-circuit and open-circuit defects are in fatal defects category. Breakout, under etch, missing hole, and wrong size hole fall in potential defects category [6], [7], [8]. Fatal defects are those in which the PCB does not meet the objective for which it is designed, while the potential defects are those which compromise the PCB performance during utilization. There are many ways to designate PCB errors as shown in Table I

Fig. 1 (a) and (b) show the examples of reference PCB image and defective image. Each defect shown in Fig.1 (b) is a representative example of certain defects as listed in Table I, though the shape and the size of the defects may vary from one occurrence to another.

During the manufacturing of printed circuit boards, widths of insulators and conductors can change because of manufacturing defects such as dust, over etching, under etching, and spurious metals. The objective of printed circuit board (PCB) inspection is to verify that the characteristics of board manufacturing are in conformity with the design specifications [Mesbahi and Chaibi, 1993]. As PCBs normally contain complex and detailed patterns, manual visual inspection is very tiring and very subjective to errors.

**Table 1:** Defect on Single Layer Bare PCB

| | | |
|---|---|---|
| FATAL | 1 Breaks | 1.1 Fracture |
| | | 1.2 Cut |
| | | 1.3 Scratches |
| | | 1.4 Cracks |
| | 2 Shorts/bridges | |
| | 3 Missing conductor | |
| | 4 Incorrect hole dimension | |
| | 5 Missing hole | |
| POTENTIAL | 6 Partial Open | 6.1 Mouse bit |
| | | 6.2 Nicks |
| | | 6.3 Pinholes |
| | 7 Excessive spurious | 7.1 Specks |
| | | 7.2 Spurs/protrusions |
| | | 7.3 Smears |
| | 8 Pad violations | 8.1 Under etching |
| | | 8.2 Over etching |
| | | 8.3 Breakout |
| | 9 Variations between the printed lines | 9.1 Small thickness wiring |
| | | 9.2 Large conductors |
| | | 9.3 Excessive conductors |
| | | 9.4 Incipient short (conductor too close) |




(a) (b)

**Figure 1:** PCB without error (a) PCB with error (b)

**A. Concepts of logic Operator for Image*:***

An arithmetic or logic operation between images is a pixel-by-pixel transformation. It produces an image in which each pixel derives its value from the value of pixels with the same coordinates in other images [9].

If *A and B* are the images with a resolution *XY*, and *Op* is the operator, then the image *N* resulting from the combination of *A* and *B* through the operator *Op* (fig.2) is such that each pixel *P* of the resulting image *N* is assigned the value

*pn* = (*pa*)(*Op*)(*pb*) ; where *pa* is the value of pixel *P* in image *A*, and *pb* is the value of pixel *P* in image *B*.

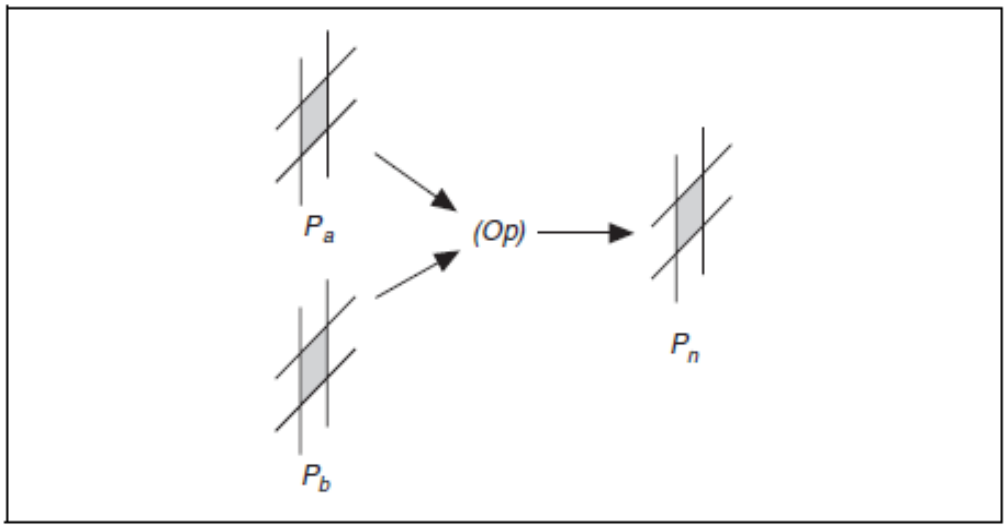



**Figure 2:** Operator Concept

**B. Logic and Comparison Operators:**

*Logic operators* are bitwise operators listed in Table II. They manipulate gray-level values coded on one byte at the bit level [9]. In the case of images with 8-bit resolution, logic operators are mainly designed to combine gray-level images with mask images composed of pixels equal to 0 or 255 (in binary format 0 is represented as 00000000, and 255 is represented as 11111111), or to combine or compare images with a binary or labeled content (after thresholding the image).

**Table 2:** Logical Operators

| | |
|---|---|
| Logical Operators Operator Equation | AND pn = pa AND pb |
| NAND pn = pa NAND pb | OR pn = pa OR pb |
| NOR pn = pa NOR pb | XOR pn = pa XOR pb |
| Logic Difference pn = pa AND (NOT pb) | |
| Logical Operators Operator Equation | AND pn = pa AND pb |
| NAND pn = pa NAND pb | OR pn = pa OR pb |
| NOR pn = pa NOR pb | XOR pn = pa XOR pb |

Furthermore, manual inspection is slow, costly, and can leads to excessive scrap rates. Besides, it also does not assure high quality of inspection. The technology of computer vision has been highly developed and used in several industry applications. One of these applications is the automatic visual inspection of PCB. The automatic visual inspection is important because it removes the subjective aspects and provides fast and quantitative assessments. It also relieve human operator from tedious, boring, and repetitive tasks of inspection. On the other hand, automatic systems do not get tired and are consistent [Moganti et al, 1996].

The reference comparison approach is based on a comparison between the image of the PCB to be tested and that of an ideal PCB which is conform to pre-defined design specifications. There are two major techniques: image comparison methods and model-based inspection. Image comparison, which is the simplest approach, consists of comparing both images pixel-by-pixel using simple logic operators such as XOR. The main difficulty found in these techniques is determining a precise alignment of the reference image and the test image, which makes its utilization difficult. More sophisticated proposals under the same idea, involve feature and template matching [Moganti et al, 1996], but suffer from the same problem and normally require a large number of templates. Model-based methods are techniques, which match the pattern under inspection with a set of predefined models. They are also called *Graph-Matching Methods* [Moganti et al, 1996] and are based on the structural, topological, and geometrical properties of the image. The major difficulty of those methods is related to the matching complexity. Although Sun and Tsai [Sun and Tsai, 1993] proposed a technique called *Pattern Attributed Hypergraph* to make the method more practical, it still remains a complex and time-consuming method.

The design rule checking approach is based on the verification of the general design rules that is essential in the verification of the widths of conductors and insulators. As a kind of automatic inspection algorithm for bare PCB, the design rule checking has been proposed and well known to the automatic visual inspection system manufacturers [Hong et al, 1998].

The design rule checking (DRC) method checks if all patterns and spaces of PCB surface meet or violate common knowledge, which is called the design rule. Because a simple algorithm is applied directly to an image, the implementation of this algorithm is comparatively easy. This means that it does not require severe alignment and adjustment of a mechanical part to get a non-distorted image. However, this method is a very time consuming process and a great computing power is needed to meet user's requirement of inspection time.

Nowadays, considering the state of affairs of an inspection system, the combined inspection methods are used. This hybrid approach merges the advantages of the reference comparison method and the DRC method to overcome the weaknesses of each method. For example, most of the design-rule verification methods are limited to verifying minimum conductor trace, angular errors, and spurious copper. Then, PCB defects which do not violate the design rules are detected by reference comparison methods. These methods can detect missing features or extraneous features. The design rule process detects all defects within small and medium features while the comparison methods are sensitive to the largest features. Hybrid approach makes use

both of these methods as they complement each other and therefore achieve a full sensitivity of PCB inspection.
Defect detection stage is accomplished using subtraction procedure while the second stage is completed using three indices: the type of object detected, the difference in object numbers, and the difference in background numbers between the inspected image and the template.

Figure 3 and Figure 4 show the examples of defect free PCB image and defective image, respectively. Though each defect shown in the Figure 4 is a representative example of certain defects, the shape and the size of the defects may vary from one occurrence to another.

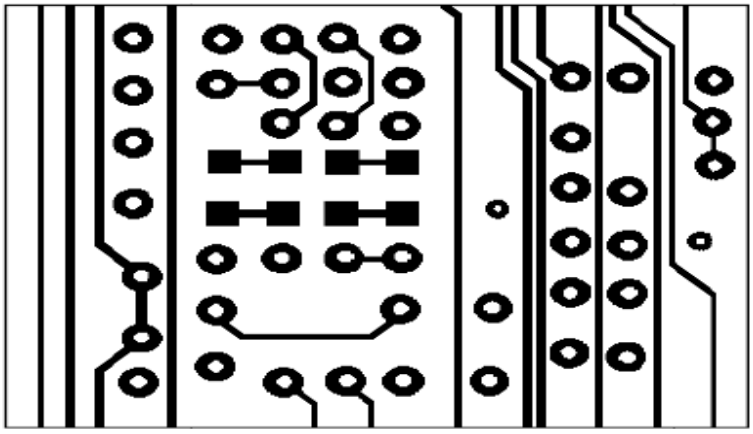


**Figure 3:** Template image of a bare PCB

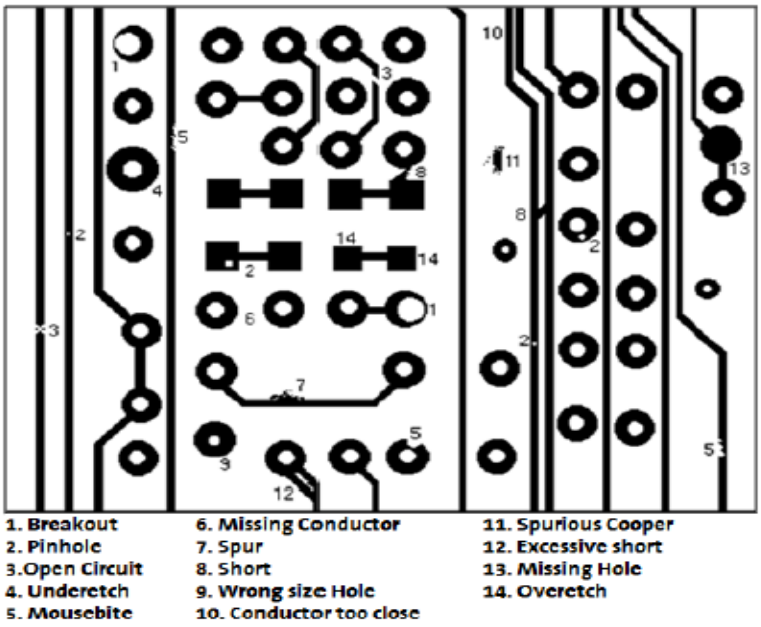



**Figure 4:** Defective image of a bare PCB

## III. IMPLEMENTATION OF METHOD

### A. Inspection Flow Chart

The PCB inspection using Image subtraction method [7],[10], [11] is performed in steps. As shown in flow chart (fig.5) the first step load a reference image, second step buffers the reference image so that it can be used for subtraction operation. The third step loads the image which is going to be inspected. To find the PCB error, inspected image is XORed with reference image; this process is also called Image subtraction.


**Figure 5:** Inspection flow chart-I

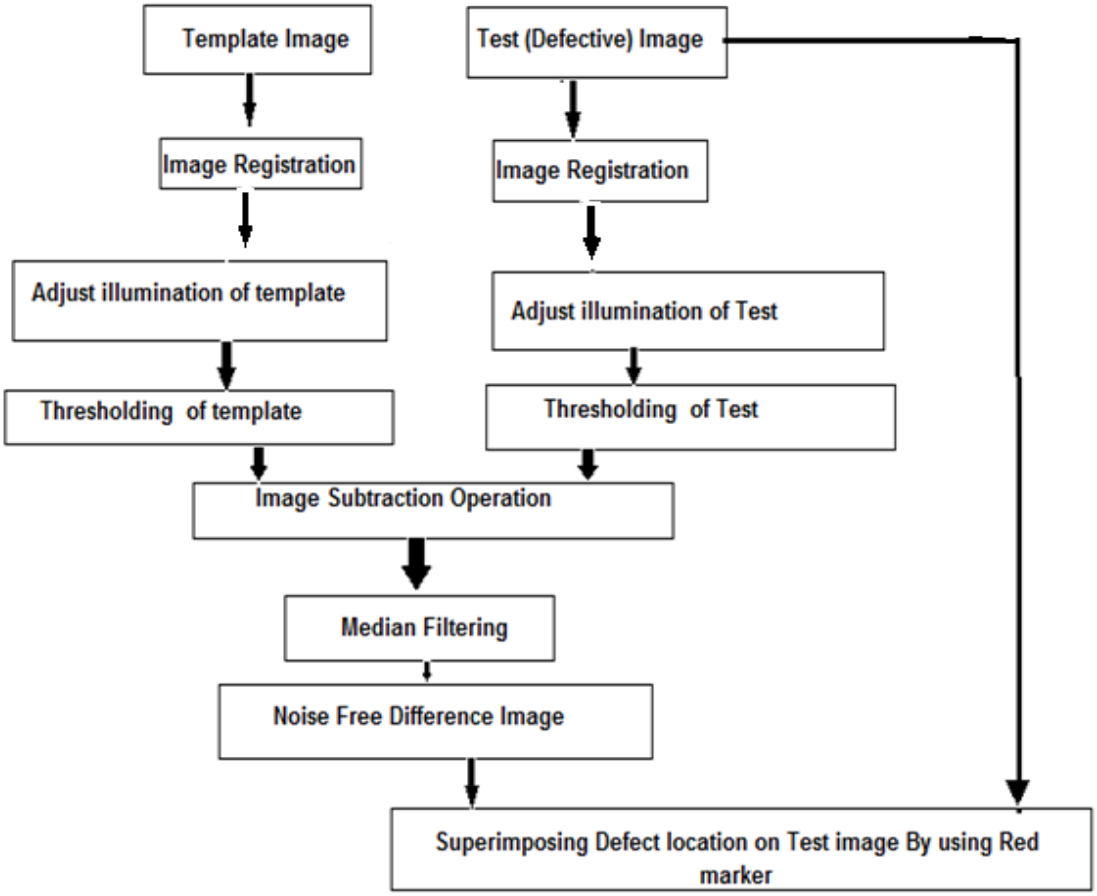



**Figure 6:** Inspection flow chart-II

**B. Image Subtraction Operation**

Image subtraction operation is performed in order to get the differences between two images [3], [4]. The images are the reference image and the inspected image. The method compares both images pixel-by-pixel using XOR logic operator [7], [9], [12]. The resulting image obtained after this operation contains defects.

The subtraction operation will produce either negative or positive image, '1' represents white pixel and '0' represents black pixel in a binary image.
Two rules exists for image subtraction operation
Rule 1: If 1-0 = 1 then it gives positive pixel image
Rule 2: If 0-1 = -1 then it gives negative pixel image.

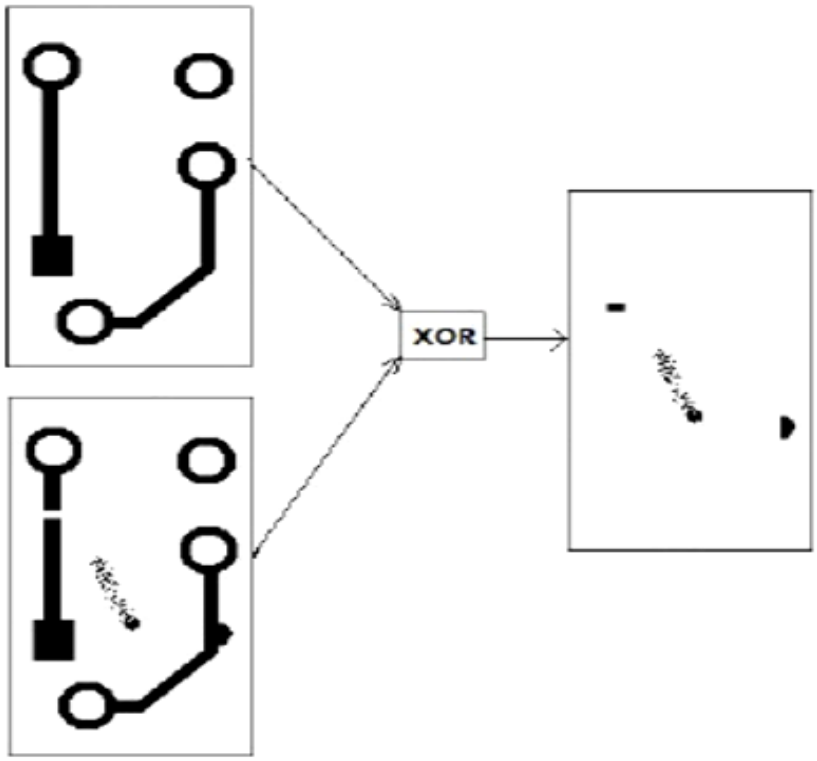



**Figure 7:** Image subtraction operation

These images are converted into grayscale and added into image buffer before subtraction process. The conversion of image into grayscale is needed for obtaining binary image and this image is further processed for measurement purposes.

**C. Algorithm**

There are a two step process to detect and classify the defects. In the first step, defects have been detected and in the second step, the defects have been classified.

***Step-I: Detection of defects in PCB image***

For detection of defects the template image (It) fig(3) and the defective image (Id) fig(4) are compared using image subtraction operation to obtain positive image (Ip) and Negative image (In) as shown below

$$In=It-Id \quad (1)$$

$$Ip=Id-It \quad (2)$$

The addition of the positive image and the negative image gives all the defects present in the defective image as shown in equation (3).

$$Ia=In+Ip \quad (3)$$

***Step-II: Classification of defects:***

Here the defects have been classified and grouped into 5 groups as given under:

Group 1: Wrong size hole and missing hole

Group 2: spur,short,conductor or too close,underetch,spurious copper and excessive short.

Group3: Pinhole and breakout

Group4: overetch,mousebite and opencircuit

Group5: Missing conductor

*a.* ***Classification of group1 and group 2 defects:***

In this image has been used along with the complement of template image (Itc). imfill operation (fill all the empty spaces and holes) has been applied on the complement of the template image (Itcf). The In image has been subtracted from the Itcf image to form difference image (Idh). Finally the resultant image Idh has been subtracted from Itcf. Thegroup1 defects i.e.wrong hole size defect and missing hole defect has been presented by the output image (Ig1).Difference of In and Ig1 images gives group 2 defects.

Itc=complement (It) (4)

Itcf=flood fill (Itc) (5)

Idh=Itcf-In (6)

Ig1=Idh-In (7)

Ig2=In-Ig1 (8)

***b. Classification of Group3 defects:***

In this Ip image has been used along with the complement of defective image (Idc). Im fill operation (fillall the empty spaces and holes) has been applied on the complement of the defective image(Idcf). The Ip image has been subtracted from the Itcf image to form difference image(Ide). Finally the resultant image Ide has been subtracted from Idcf. The group3 defects i.e. Pinhole defect and breakout defects hve been presented by Ig3.

Idc=complement (Id) (9)

Idcf=floodfill(Idc) (10)

Ide=Idcf-ip (11)

Ig3=Idcf-Ide (12)

***c. Classification of Group 4 defects and group 5:***

In this the group 3 defects image(Ig3) is subtracted from Ip to obtain result image Ir presenting 4 more defects namely overetch, opencircuit, mousebite and missing conductor .opening of Ir after flood filling it(Irf) is done using disk structuring element of appropriate radius and subtracting it from Irf to separate missing conductor

defect from other 3 defects. The group 4 defects have been presented by Ig4.

Ir=Ip-Ig3 (13)

Irf=floodfill Ir (14)

I1=opening of (Irf,se);where se= disk structuring element (15)

Ig4=Ir -I1 (16)

Subtracting the group 4 defect image from Ir gives the group 5 defect i.e. missing conductor.

Ig5=Ir -Ig4 (17)

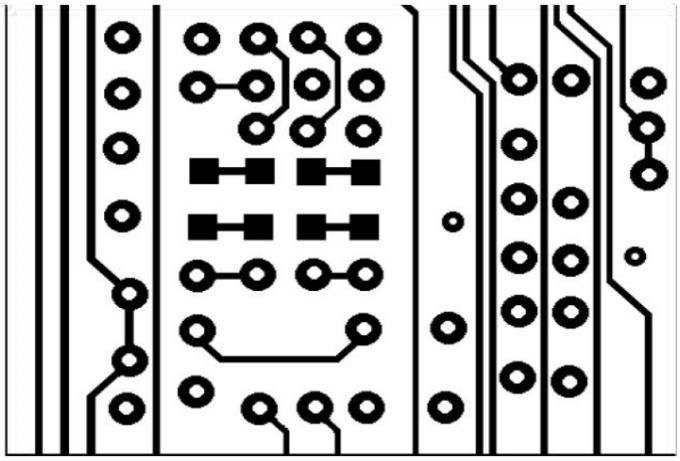


**Figure 8:** Reference image

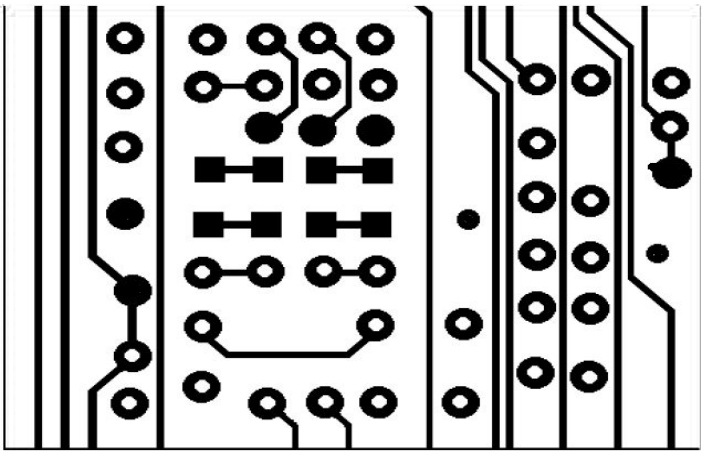


**Figure 9:** Image for inspection: - Missing holes

The resultant image is further processed for thresholding in order to convert the resultant image in binary form. The binary form of image shows the resultant area into ‘1’and ‘0’ form. The image area which contains information is represented by ‘1’

and rest of portion is considered as'0'.

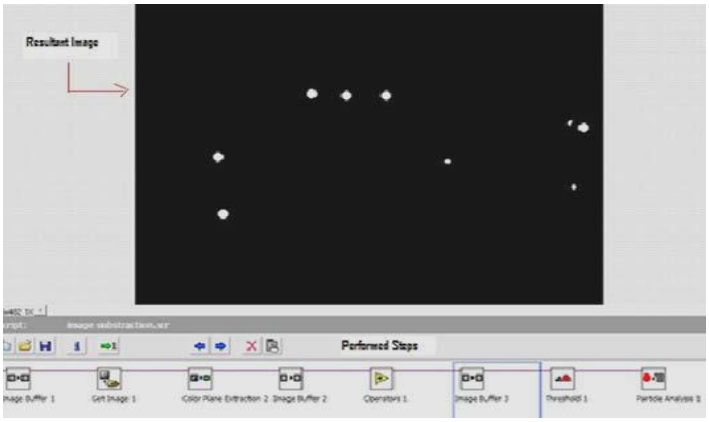



**Figure 10:** Resultant image after subtraction operation

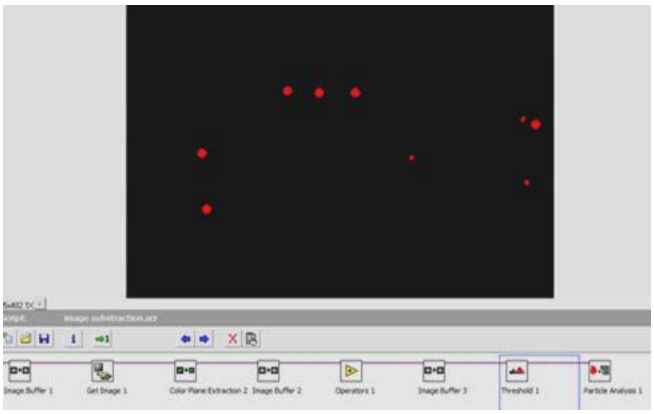


**Figure 11:** Resultant image after thresholding

For the measurement purpose 'Particle Analysis' function of the NI Vision Assistant is used [9]. This 'Particle Analysis' is applied on the obtained defected area of PCB and outputs are represented in terms of parameters such as area, orientation, X and Y coordinate etc. All measurements can be done in terms of pixel or system calibrated units.
Here pixel is being used as a unit for measurement.

**Morphological Processing** is one of the widely used techniques in PCB inspection. The inspection involves the expansion-contraction process, which does not require any predefined model of perfect patterns. Ye and Danielson presented an algorithm for verifying minimum conductor and insulator trace widths. The method iteratively applies shrinking (similar to contraction operation) and connectivity preserving shrinking (similar to thinning) operations on the image.

After some number of iterations, the difference (logical AND) between the results gives the defects present in the patterns. The main advantage of these methods is that the alignment problem is eliminated

## IV. CONCLUSION

The bare PCB is analyzed and the defects of PCB are extracted in terms of various parameters. These parameters can be taken as referential data base for further analysis to fabricate defect free PCB and can assist in making an automated system for inspection. In order to use this method in an industrial application some improvements need to be done. Future work consists of inspecting and analyzing a PCB with Surface Mounted Devices.

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