Efficient Current Feedback Operational Amplifier for Wireless Communication

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Abstract

In this proposed work, the working of current mode feedback operational amplifier (OP-AMP) is being studied. A current feedback operational amplifier (CFOA) is presented in this paper at 180nm technology. The drawbacks of voltage mode operational amplifier are completely overcome by CFOA. The circuit employs MOSFET transistors, so it can be used for standard CMOS fabrication. Results of simulations includes power dissipation 0.44mW, bandwidth 129.96MHz, and gain 0.437.

Keywords: OP-AMP, CFOA, MOSFET, CMOS.

INTRODUCTION

In recent years, current feedback operational amplifier and current conveyor has been receiving great interest to the design and analysis, mainly because these circuits have better performance, particularly high speed and better bandwidth than voltage mode amplifiers. CFOA is transimpedance amplifier which produces an output voltage proportional to input current. Current-conveyors are three-port networks with terminals X, Y and Z as represented in Figure 1 [1]. The network of the first generation current-conveyor CCI [2] [3] [4] has been formulated in a matrix form.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$



Figure 1: The First Generation Current-Conveyor (CCI)

CFOA [5] [6] [7] [8] [9] started getting attention of researchers working in analog and mixed signal design when it was realized that it can act as an alternative to conventional voltage amplifier mainly because of its independent gain-bandwidth product, which is not inherent in voltage feedback amplifiers [10]. Due to its gain-bandwidth independence, designers are allowed to operate over wide range of frequency without compromising with gain. This feature makes CFOA more efficient as well as preferable over the conventional voltage amplifiers. When a voltage is applied at node Y shown in figure 1, the same voltage is replicated at node X. This is similar to the virtual short on an op-amp. Also when a current is injected into node X, that same current gets copied into node Z. Thus the terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits zero input impedance.

The paper is organized as follows. In section II, the design methodology which has been used to design proposed circuit is explained. In section III, the detailed description of proposed CFOA and its CMOS realization are given. In section IV, SPICE simulation results of the proposed circuit using CMOS 180nm technology are illustrated. In section V, conclusion is given.

DESIGN METHODOLOGY

Figure 2 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors, such as the inverting node bias current and the offset voltage, are excluded from this model. The most important parameter limiting the dc gain is the transresistance Rt, which is ideally infinite. A finite value of Rt is analogous to the finite open-loop voltage gain in a conventional op amp. The current applied to the inverting input node is replicated by the current conveyor to flow in Resistor Rt. The voltage developed across Rt is buffered by the unity gain voltage follower. Voltage gain is the ratio Rt/RIN, with typical values of Rt = 3 M and RIN = 50.

The important parameters defining ac behavior are the transcapacitance, C_t , and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp and thus cannot be reduced

below a critical value if the closed-loop system is to be stable. In practice, C_t is held to as low a value as possible (typically4.5pF) so that the feedback resistor can be maximized while maintaining a fast response.



Figure 2: Schematic of Circuit

PROPOSED CIRCUIT OF CFOA

The circuit diagram of the proposed CFOA is shown in figure 3. It uses two stage conventional voltage op amp in closed loop configuration and an additional pair of transistors to design CCII+.



Figure 3: Current Feedback Operational Amplifier

Transistors M1, M2, M3 and M4 serve the purpose of differential amplifier, whereas two additional current mirrors are used for inversion. The output stage of op amp is made using the same VFA which was used in the first stage, but the transmission gate coupled to capacitor is removed. It was observed that absence of transmission gate in the output stage affected the output characteristic slightly, but it was improved by changing the aspect ratio of the transistors employed in the design. The aspect ratios of different transistors are given in Table 1 and the values of bias voltages and different passive components used inside the proposed circuit are specified in Table 2.

Transistor	W/L Ratio
M1	60/.18
M2	60/.18
M3	90/.18
M4	90/.18
M5	28/.18
M6	28/.18
M7	17/.18
M8	17/.18

Table 1: Aspect Ratio of Transistors

Table 2: Component Value

Component	value
IB1	2.5uA
IB2	2.5uA
VDD	2.5v
VSS	-2.5v
IIN	10A
Iin2	-300uA
CL	100pf
RL	1Ω
Ri	170Ω

SIMULATION RESULTS

The performance of the proposed CFOA circuit was verified by performing PSpice simulations with supply voltage 2.5V using 180nm CMOS technology parameters.



Figure 4:CFOA Amplified waveform

The static power reduction is an important optimization constraint in circuit design. The output of the amplification of current feedback op-amp is shown in figure 4. The power of this designed op-amp is 0.44mW.



Figure 5: Differential Current Gain

As the gain and bandwidth are independent of each other in CFOA, when bandwidth increases there is no any effect on gain of the product. Above figure 5 shows the graph of differential current gain which is obtained using Pspice simulation.

CONCLUSION

A new design of CFOA based on op amp and current conveyor was presented and simulated using PSpice. In this work, very accurate, fully efficient CFOA is proposed and simulation results are presented. As expected in simulations, the new CFOA has a better results which plays important role in wireless communication, such as less power dissipation of 0.44mW, current gain of 0.437, and efficient bandwidth 129.96MHz.

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