International Journal of Electronics and Communication Engineering.
ISSN 0974-2166 Volume 11, Number 1 (2018), pp. 1-6

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A Study on Power Implementation and Validation at Higher Level of Abstraction

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Abstract

Timing and silicon area were the prime parameters of concern in an earlier generation of IC design technologies. The rising demand for high-performance, battery-operated, system-on-chips in communication and computing has shifted the focus from traditional constraints to power consumption. During the design process, the most critical power requirements could be tested after power pins become explicit. Despite so many design strategies to reduce power consumption, it becomes crucial to make the power-aware design even if power pins are not exact or at the very abstraction level of the design flow. UPF is used to provide a consistent way to specifying power implementation intent throughout the design process. The paper explains the impact of HDL models at very high abstraction level to meet specific power constraints and their validation using an industry-accepted IEEE 1801 standard UPF low power validation.

1. INTRODUCTION

According to Harris & Harris (2017), Hardware description language (HDL) allows the designer to specify logic function only. Then a computer-aided design (CAD) tool produces or synthesizes the optimized gates. Most commercial designs built using HDLs. The two leading HDLs are Verilog and VHDL. Verilog developed in 1984 by Gateway Design Automation, and it became an IEEE standard (1364) in 1995. VHDL developed in 1981, and it became an IEEE standard (1076) in 1987. VHDL stands for "very high-speed integrated circuit hardware description language." Both VHDL and Verilog are officially endorsed IEEE (Institute of Electrical and Electronics Engineers) standards (Mohammed Ferdjallah, 2011). Now both Verilog and VHDL are used extensively, and probably exclusively, by circuit designers everywhere. So many simulation and synthesis tools have been developed and marketed which automate the analysis and realization of various hardware description language models.

2. POWER UTILIZATION IN ELECTRONICS DESIGN

According to Silicon Laboratories Inc, the dynamic power consumption occurs due to switching activity while the reason for static power consumption is leakage current. For reducing the power consumption, there are different methods, such as clock gating, power down modes in design, power gating, multiple threshold libraries, reducing supply voltage and voltage and frequency scaling.

3. CONVENTIONAL HDL MODEL AT HIGHER LEVEL OF ABSTRACTION

Traditionally HDL models have only logical functionality information no power information given in HDL models. At the very higher level of abstraction, the HDL models functionality can give regarding truth table. If **i1** and **i2** are logical inputs, and **Z** is the output, then an input i1 & i2 and the output Z are related as –

$$\mathbf{Z = f(i1, i2)}$$

It shows that the output is the only function of logical inputs. The logical functionality is equivalent to the design functionality. Regarding truth table, the functionality is given as –

Table 1: Logical Functionality Truth Table

i1	i2	Z
0	0	0
0	1	0
1	0	0
1	1	1

The algorithmic description of the electronic design is given in higher level of abstraction. We have information about the input and output but no information how input produces output within the design? We can say that as the level of abstraction decreases we reached more close to the actual design.

4. POWER IMPLEMENTATION AT VERY HIGHER LEVEL OF ABSTRACTION

The amount of design decisions that have specified in the description of the circuit is known as levels of abstraction. The abstraction level will be high at the fewer design decisions. The design functionality consists both logical as well as power functionality when we talk about the power implementation at the abstraction (higher level).

If **i1** and **i2** are logical input, **Z** is output**, gnd** is ground pin, and **sup** is power supply then the output is given as –

$$\mathbf{Z = f\ (i1, i2, sup, gnd)}$$

It shows that the output is a function of not only logical inputs as well as the power and ground pins. The design functionality contains both logical as well as power functionality on which basis the truth table is below–

Table 2: Complete Design Functionality Truth Table

sup	gnd	i1	i2	Z
0	-	-	-	X(CORRUPT)
-	1	-	-	X(CORRUPT)
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1

As per the truth table, we can say that when power pin is in high logic state and ground pin is in the low logic state then only logical functionality comes into the picture, if power and ground pins are not connected correctly, then it shows no significance of logical functionality.The power implemented HDL model can be used with complete functionality or for low power validation can be demonstrated by following flow diagram –

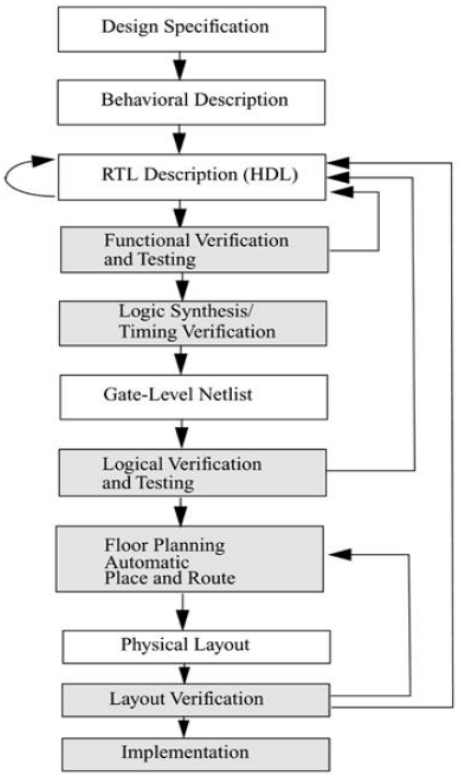

Fig 1: Flow for Low Power Validation of Power Implemented HDL Model

At a higher abstraction level power and ground pin is not in the top port list, so we have to implement a power and ground pin logic generation block in the HDL description so that the model becomes power implemented model which also used for functional validation just like traditional non-power aware HDL model. This power and ground pin logic generation block help us to skip the checking of power pins logic as shown in fig 2. The flow for normal functional validation of power implemented HDL model is given as –

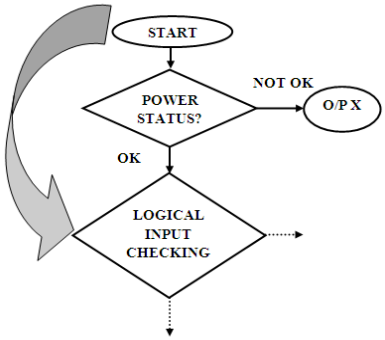

Fig 2: Flow for Normal Functional Validation of Power Implemented HDL Model

After the implementation of power functionality at the very high level of abstraction, the HDL model consists the complete functionality of design and power & ground pin logic generation block. The power implemented HDL model is given as –

```
modulepower_imple_hdl_model (Z, i1, i2);
output Z;
input i1;
input i2;
.
.
INTERNAL
SUPPLY & GROUND
GENERATION
.
.
.
.
LOGICAL + POWER
Functionality
Description
.
.
endmodule
```

5. VALIDATION AT HIGHER LEVEL OF ABSTRACTION USING UPF

Power implemented model can be generated easily, but their validation at the abstraction level is the most difficult task because we don't have any direct port to port contact for power and ground pins as they are not present at the top port list. In the module description, these power and ground pin is defined as an internal variable. Unified Power Format (UPF) provides a way to validate the power implemented model by creating the power switches, power nets and connecting those nets directly to the domain supply of the design (Macii et al., 1998). Before this, we have to specify the different supply domain. In UPF we use a combination of HDL and UPF intent. All these things at CAD level can be created and connected by using TCL commands. After creating all these things, we have to validate our design regarding power functionality by toggling the power and ground pin through power controller block. Power controller block can invoke through some variable used in the test bench. For UPF validation there are different EDA tools available in the market like Incisive Enterprise Simulator (IES) from cadence, Native VCS from Synopsys.

6. RESULTS AND CONCLUSION

We have validated the traditional HDL model functionality which is equivalent to the logical functionality given in Table 1. The waveform generated by the SimVision is given below. This type of validation is known as functional validation.

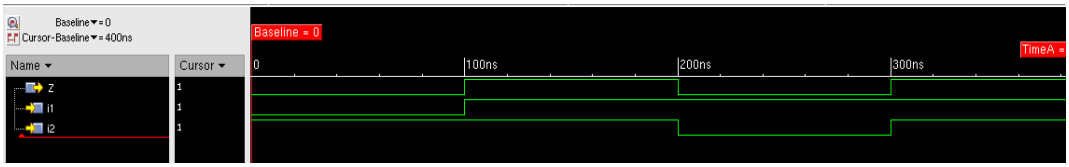

Fig 3: Functional Validation Result of Traditional Non-Power Implemented HDL Model

After implementation of power at very abstraction level we need UPF validation, through waveform it is clear that when supply goes down the device output is X irrespective of the logical input as shown in Table 2.

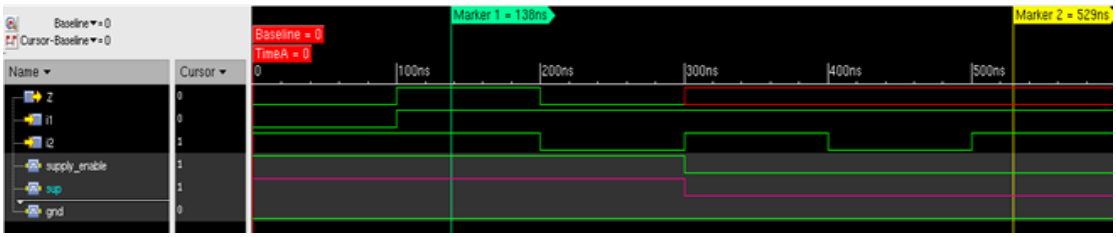

Fig 4: UPF Validation Result of Power Implemented HDL Model

At marker2 in fig 4, the power supply goes down, so the output is corrupted, i.e. with the logical input variation, there is no variation in output which in turn reduces power consumption. In conclusion, we can say that UPF is an excellent way to validate the power functionality of power implemented HDL model at the very higher abstraction level of design flow which reduces efforts in the further design process and saves money as well as time.

7. FUTURE ENHANCEMENT

Design complexity is increasing day by day. Therefore the power requirement and speed of the system becomes a crucial parameter. Besides the demand for energy efficiency for environmental concern is a constant motivation factor for low power energy efficiency electronics. As design complexity increases in future, we needed some excellent CAD tools which provide easy debugging and user-friendly power validation techniques.

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