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A Novel Approach to Design and Implement Low Power High-speed HDL Model

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Abstract

In recent years device densities and clock frequency have increased dramatically in devices thereby increasing the power consumption significantly. During the design process, the most critical power requirements can be tested only after power pins becomes explicit. There are different design strategies for reducing power consumption, and it also becomes critical to make the power-aware design even if power pins were not precise or say at very high abstraction level of the design flow.

1. INTRODUCTION

In any design process, the first step is to write desired specifications of the design. During this process, the developer does not need to think about circuit implementation of the design. The behavioural description is created to analyse the design regarding performance, functionality and compliance to standards with other high-level issues at the higher level of abstraction of the design flow. HDLs are often used to develop the behavioural description of the design. Top-down design and Bottom-up design are the two basic types of design methodologies used in different integrated circuit design industries. There is two most popular and widely used industry accepted hardware description languages are- 1) Verilog HDL, 2) VHDL. HDLs have many advantages over traditional schematic-based design flow such as Designs can be described as a very higher abstraction level by use of HDLs. The designer can write their RTL description without choosing a fabrication technology, means RTL description is technology independent. Logic synthesis tools can automatically convert or say link the design to any specific fabrication technology. If a new technology emerges, designers do not need to redesign their circuit. They simply input the RTL description of the design into the logic synthesis tool and then create a new gate-level netlist by using the new fabrication technology. The logic synthesis tool will optimize the circuit regarding area and timing for the specified new technology. Most design bugs

or errors are eliminated at very higher level of abstraction. It cuts down design cycle time as well as design costs significantly because the probability of hitting a functional bug or error at a later stage of design flow either in the gate-level netlist or the physical layout is minimized. Designing with HDLs is simply analogous to write a computer program, which is nothing but a textual description of the design functionality. A textual description with comments is an easier way to develop and debug the design. This also provides a concise and clear representation of the design itself at a higher level, compared to gate-level schematics.

2. TOOLS FOR DESIGNING & VERIFICATION

There are different EDA companies like Cadence, Synopsys, Mentor Graphics etc. They provide various tools for design & verification purposes. Some of the tools are, 1) NCSim by Cadence, 2) VCSMX by Synopsys.

2.1 Low Power Design Strategy

As CMOS technology consumes lesser power, so we called it as low power technology when the clock frequency is relatively low. The leakage current is negligible with CMOS design technology. As device functionality becomes complex and the frequency of clock increases the device density increases rapidly dramatically. The increased device density contributed to higher power consumption as the threshold is lowered and the supply voltage is continuously reducing. The threshold and the supply voltage taking participation in higher leakage current which increases the power consumption. On a conclusion, we can say that power also becomes critical as timing and area.

2.1.2 Low Power HDL Model Generation

Once the complete understanding of any design completed, then we go for model generation.

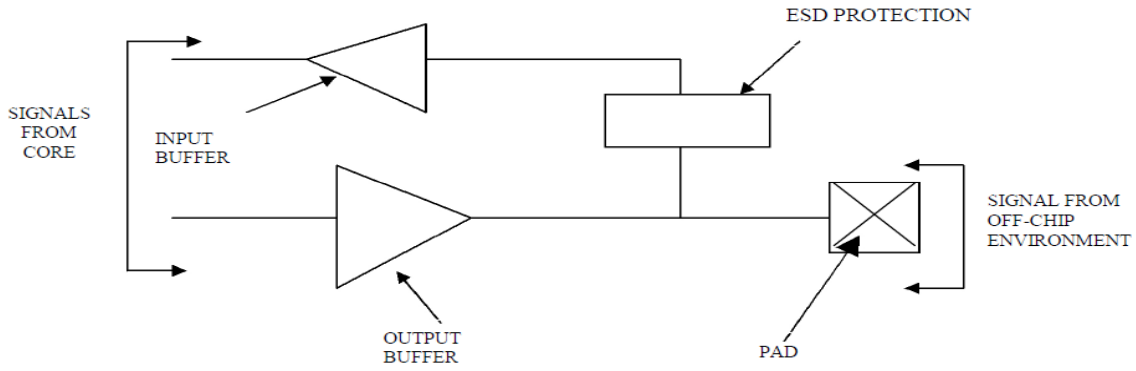

FIG 1: BLOCK DIAGRAM OF BIDIRECTIONAL BUFFER

2.2 Model Generation of bidirectional I/O buffer

In Verilog model, only logical pins are present at the top port list. Functional section of the model has only logical functionality; traditional Verilog module description gives no power functionality information.

The Verilog model can be described as –

module<module_name> (<logical pins>);

...

<logical functionality>

...

endmodule

3. HDL MODEL VALIDATION

The prime importance of validation is finding bugs in the design. The process of verification parallels the design creation process.

3.1 The method of validation

The design should be validated in terms of Functional validation and Low power validation. Various methodologies were developed from time to time for low power validation of HDL models, which are 1) CPF – Common Power Format and 2) UPF – Unified Power Format.

3.1.1 Low power validation of OTG USB using UPF

The IEEE 1801 Standard for Design and Verification of Low Power Integrated Circuits, also known as the Unified Power Format (UPF), provides a consistent way to specify power implementation intent throughout the design process, including synthesis, physical implementation, and verification.

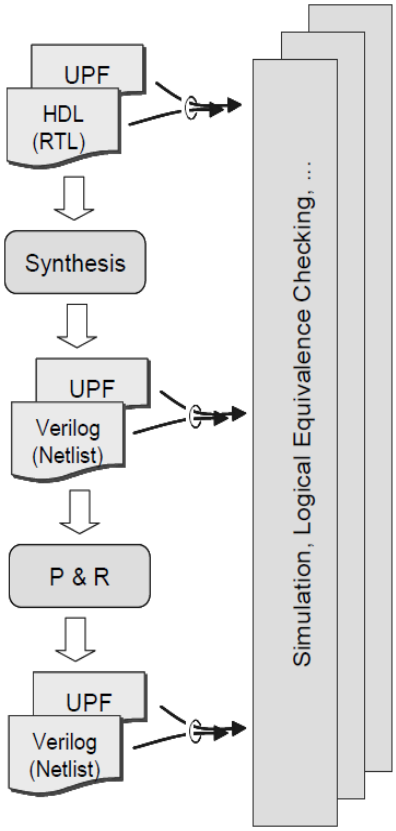

FIG 2: UPF VALIDATION AT DIFFERENT DESIGN STAGES

4. Results and Conclusion

The snapshot of traditional Verilog module description is given below –

```
1  module NON_PA_BIDIR_MODEL (PAD, CORE_IN, CORE_OUT, EN_IN_BUF, EN_OUT_BUF);
2
3   inout PAD;
4
5   output CORE_IN;
6
7   input CORE_OUT;
8   input EN_IN_BUF;
9   input EN_OUT_BUF;
10
11  bufif1 IN_BUF (CORE_IN,PAD,EN_IN_BUF);
12  bufif1 OUT_BUF (PAD,CORE_OUT,EN_OUT_BUF);
13
14 endmodule
15
```

FIG 3: SNAPSHOT OF TRADITIONAL VERILOG MODULE DESCRIPTION

As power and ground pins are not at the top port list, we can control these pins through UPF interface between testbench and power-aware module. When supply goes down we corrupt output pins logic in low power designs (at marker 2 & 4).

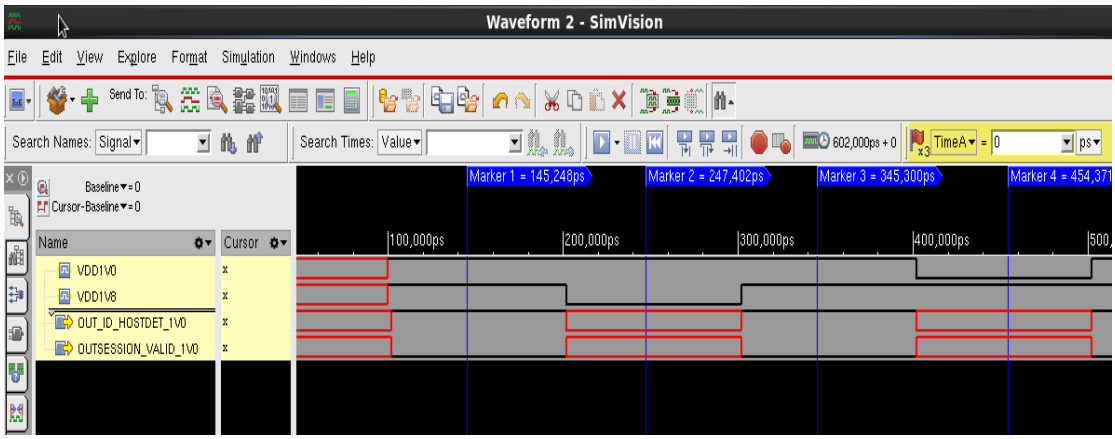

Fig 4: Snapshot of USB OTG low power validation

5. FUTURE RESEARCH SCOPE

The design complexity is increasing day by day. Nowadays the power requirement and speed of the design becomes crucial parameters. The need for long battery life for portable handheld devices like mobile phones and medical equipment is key driver for low power design. Besides, the increasing demand for energy efficiency for environmental concerns continues to be a key motivating factor for energy efficient electronics. Power management has become far trickier in the shrinking technology nodes. Along with power requirements validation continues to play an essential role by increasing the product quality, and indirectly affecting the overall production time. New methods and tools should be introduced to enhance the design productivity. It is necessary to raise the level of abstraction for design and for verification to contain the growing complexities.

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