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Implementation of Convolution Encoder and Viterbi Decoder Using Verilog

P.Saidulu[1]

Department of ECE,
MLR Institute of Technology,
Hyderabad, India.

Md. Abdul Rawoof[2]

Assistant Prof. Department of ECE,
MLR Institute of Technology,
Hyderabad, India.

Dr. S. V. S. Prasad[3]

Professor, HOD of ECE,
MLR Institute of Technology,
Hyderabad, India.

Abstract

In the today's digital communication Systems, transmission of data with efficiency and reliability is the most concerning issue for the communication channels. Error correction technique plays a important role in communication systems. The error correction technique improves the capacity of data by adding the redundant information for the source data while transmitting data through channel. This Project work mainly focus on the realization of the convolutional encoder and Viterbi decoder. The Viterbi algorithm, It is the most Preferred decoding algorithm for convolutional codes.

Keywords: Viterbi Encoder, Convolution Encoder, Xilinx power estimator.

1. INTRODUCTION

In the today's digital Communication, data transmitting between the systems play a important role. as the technologies are increasing day-by-day the number of usage of Viterbi is also simultaneously increasing. This wide usage leads to major issues in the digital communication systems and it results in data corruptions. It is necessary for the telecommunication to reduce the data corruption by finding a suitable solutions to the error Viterbi occurred in the communication process. One such method is Viterbi

Algorithm. It decodes the process by simultaneously correcting the process effectively. To decodes the convolution codes Viterbi algorithm is the most recognizable algorithm. This algorithm will be described with software and hardware implementations. To engage well organized communications an efficient data is presented by the digital systems. Data corruption is the important issue confronted by the digital communication systems. To decrease the data corruption error correcting codes is only best technique. Almost all communication systems followed this technique because it has the power to decode efficiently, even Viterbi algorithm needs very typical hardware. While the decoding operation is in advance, the functioning obstructions will be eliminated, So that an improved method, Viterbi Algorithm is used. The decoding of codes can be done very fast, as this algorithm is very effective in high-speed functions. Convolution codes are used to gain a possible code sequence AVA uses maximum likelihood decoding process. Hardware description language(HDL) is used to evaluate this project, where it is one of the hardware descriptive languages. This language is employed in designing the electronic systems to semiconductor and electronic design industries as well as for assuring the analog and mixed signal circuit.[3]

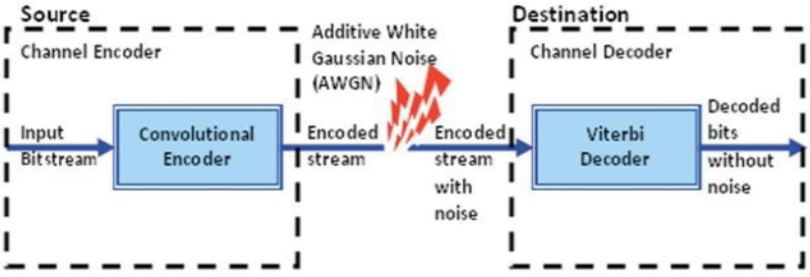

Fig 1: Convolutional encoder and Viterbi decoder.

2. CONVOLUTIONAL ENCODER

Encoding or decoding is the translation of a message that is easily understood. When you decode a message, you are extracting the meaning of that message into terms that you are able to easily understand. Decoding has both verbal and non-verbal forms through communication. Decoding behavior without using words would be observing body language. People are able to decode body language based on their emotions. For example, some body language signs for when someone is upset, anger, or stressed would be a use of excessive hand/arm movements, red in the face, crying, and even sometimes silence.

Sometimes when someone is trying to get a message across to someone, the message can be interpreted differently from person to person. Decoding is the understanding of what someone already knows, based on the information given throughout the message being received. Whether there is a large audience or exchanging a message to one person, decoding is the process of obtaining, absorbing, understanding, and sometimes using the information that was given throughout a verbal or non-verbal

message. Convolution code is the error correcting code that generates parity symbols via the sliding application of a Boolean polynomial function to a data stream. The sliding application represents the 'convolution' of the encoder over the data, which gives rise to the term convolution coding.

The sliding nature of the convolution codes facilities trellis decoding using a time-invariant trellis. Time invariant trellis decoding allows convolution codes to be maximum likelihood soft decision decoded with reasonable complexity. Convolution codes are often characterized by the base code rate and the depth (or memory) of the encoder [n, k, K]. The b, K code rate is typically given as n/k, where n is the input data rate and k is the output symbol rate. The depth is called the "constraint length" 'K', where the output is a function of the previous K-1 inputs. The depth may also be given as the number of memory elements 'v' in the polynomial or the maximum possible number of states of the encoder (typically 2^v).[2]

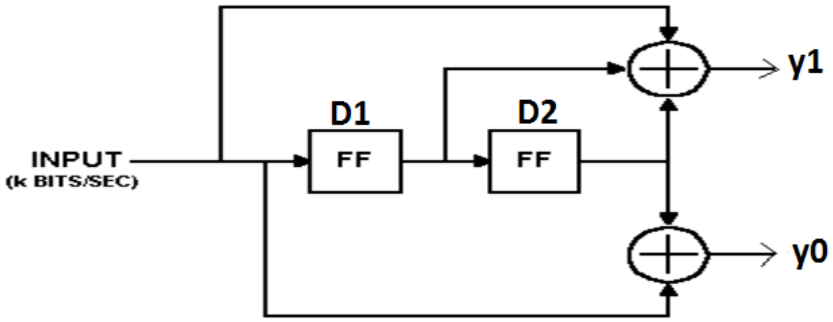

Fig 2: Convolutional encoder.

Input Bitstream for Encoder is 1011 then output(y1y0) of encoder is 11 10 00 01

3. VITERBI DECODING ALGORITHM

Decoding is the process of converting from code to plain text or any format that is useful for subsequent processes. Decoding is the reverse Process of encoding. It converts encoded data communication transmissions and files to their original states. Most computers use an encoding methodology to transfer, save or use data. Encoded data by Encoder is transformed via an encoding mechanism (for example, the Bin Hex or American Standard Code for Information Interchange (ASCII)) and transmitted via a communication medium. As an example, when sending an email, all data, including certain attachments and images, are encoded using a format such as Multipurpose Internet Mail Extensions (MIME). When data arrives, the decoder converts the email message content to its original form. A Viterbi decoder uses the Viterbi algorithm for decoding a bitstream that has been encoded using a convolution. There are other algorithms also available for decoding a convolutionally encoded stream (for example, the Fano algorithm). The Viterbi algorithm is the most resource-consuming,

but it does the maximum likelihood decoding. It is mostly used for decoding convolution codes with constraint lengths k<=10, but values up to k=15 are used in practice. When decoder decodes a message, you are extracting the meaning of that message into terms that you are able to easily understand. Decoding has both verbal and non-verbal forms through communication. [3]

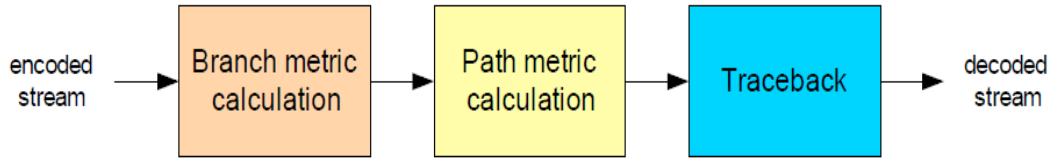

Fig 3: Block diagram of a Viterbi decoder.

4. IMPLEMENTATION OF VITERBI DECODER

The major tasks in the Viterbi decoder process are as follows:

1. Branch Metric Unit(BMU).
2. Path Metric Unit(PMU).
3. Traceback Unit(TU)

The fig.3 Block diagram shows the proposed Viterbi decoder. This section discusses the different parts of the Viterbi decoding process. Analog signals are quantized and converted into digital signals in the quantization block. The frame boundaries of code words and symbol boundaries were detected by the synchronization block. The Viterbi decoder receives parallel successive code symbols, in which the boundaries of the symbols and the frames have been identified.[8]

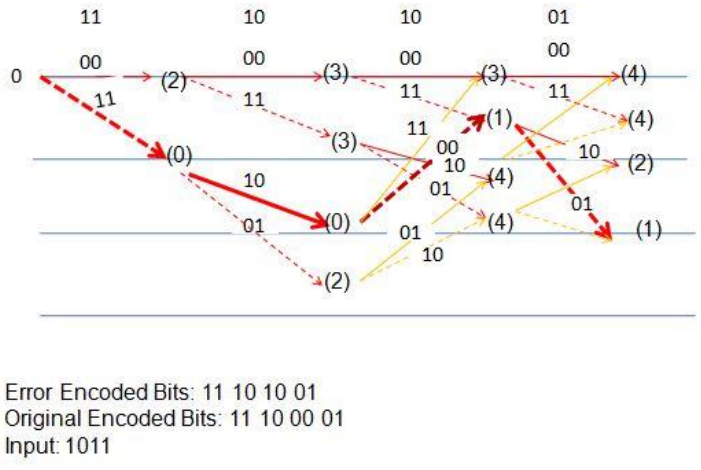

Fig 4: Convolution code trellis tree and Viterbi algorithm

4.1 Branch Metric Unit

Branch metric unit is used to generate branch metrics, which are hamming distances of input data from 11, 10, 00 and 01. The BM unit is used to calculate branch metric for all trellis branches from the input data. We choose absolute difference as a measure for branch metric. These branch metrics are considered as equaling the weights of the branches.[10]

4.2 Path Metric unit

Memory is required to store the survivor Path Matrix Unit (PMU). The word length of the memory depends on the number of the ACS sub-blocks used in the design or the total number of states in the decoder or k^2 (where k is the International Journal of Modeling and Optimization, Vol. 3, No. 1, February 2013 16constraint length, 5 in our case), and the depth of the memory depends on the trellis length[7]. The memory depth usually should be kept two times the trellis length or two blocks of memory equal to trellis length. We have for our project k = 5and trellis length equal to 32, so the memory block used is64x16. The memory used is a dual port. One port for writing the data and other for reading the data, as we need to write and read the data simultaneously and that too from different addresses. Memory should write data synchronously but the reading of the data should be asynchronous to keep the latency low or better manage the synchronous behavior of the full system.[9]

4.3 Traceback Unit

Results of these are written to the memory of traceback unit. It Traces back from the end of any survivor paths to the beginning.[2]

5. SIMULATION AND SYNTHESIS RESULTS

5.1 Synthesis Report

Synthesis is a process of constructing a gate level netlist from a register transfer level model of a circuit described in Verilog HDL.Increase the design size and complexity, as well as improvement in design synthesis and simulation tools, have made Hardware Description Languages (HDLs) the preferred design languages of most integrated circuit designers. The two important HDL synthesis and simulation languages are Verilog and VHDL. Both have been adopted as IEEE standards.

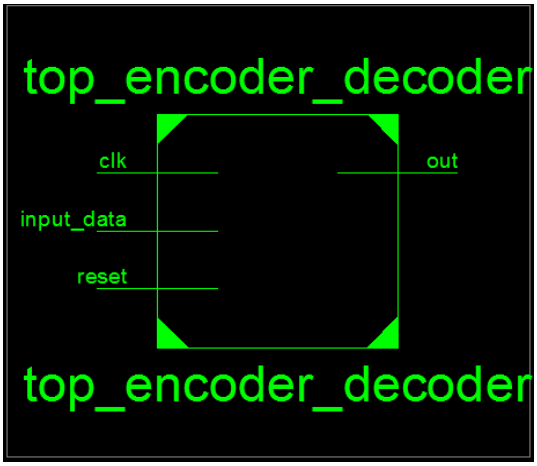

Fig 5:Encoder_Decoder(RTL1)

The above figure is the simulation representation of convolution encoder and Viterbi decoder at the circuit level. The entire code developed for this project can be visualized using Xilinx hardware device. How the VITERBI algorithm code for encoder and decoder is working in a step by step process can be analyzed based on results of implementation

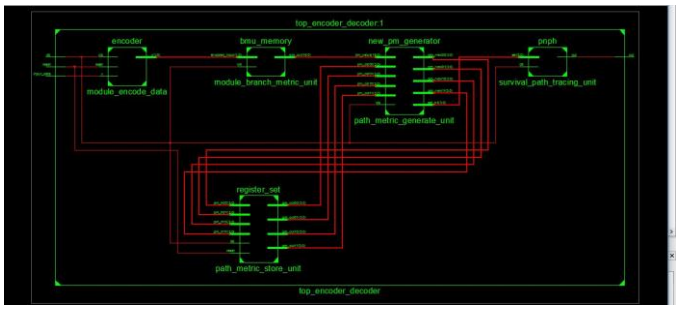

Fig 6:Encod6er_Decoder(RTL2)

The above figure shows the RTL schematic of convolution encoder and Viterbi decoder which consists of different modules like branch metric unit, encoder unit, path metric unit, survival path tracing unit and path metric store unit.

Table 1: Device Utilization of Viterbi Decoder

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	84	3584	2%
Number of Slice Flip Flops	78	7168	1%
Number of 4 input LUTs	124	7168	1%
Number of bonded IOBs	4	141	2%
Number of GCLKs	1	8	12%

Table 2: Device Utilization of Viterbi Decoder[11]

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	287	5472	5%
Number of Slice Flip Flops	217	10944	1%
Number of 4 input LUTs	558	10944	5%
Number of bonded IOBs	12	240	5%
Number of FIFO16/RAMB16s	2	36	5%
Number of GCLKs	1	32	3%

Compare to Ref[11] My Project used less number of gates.

5.2SimulationWaveforms of Convolution Encoder

The Simulation Waveform of Convolution Encoder for input 1011 is shown in Figure 7 (For Rate ½ and K = 9) and It gives Encoded output as 11 10 00 01. The simulation is done by using Modelsim and the speed and resource utilization are generated and synthesized using Xilinx Synthesis Tool (XST).

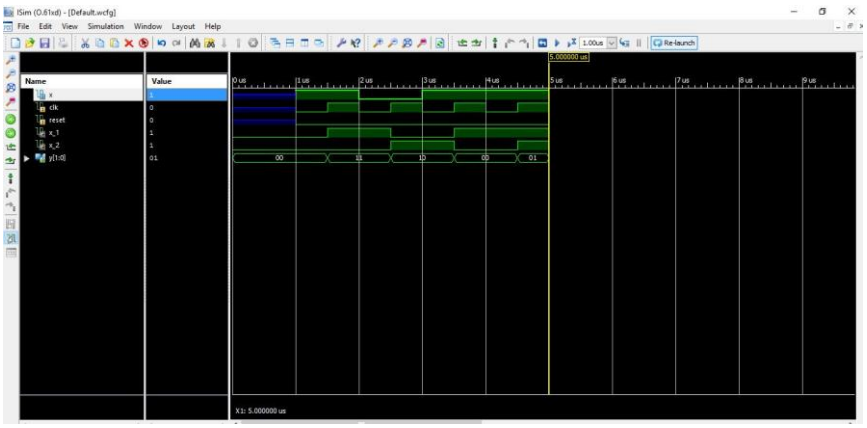

Fig 7: Xilinx simulation results for convolution encoder

5.3 SimulationWaveforms of Viterbi Decoder

The Simulation waveform of the Viterbi decoder is shown below Fig. 8. Viterbi decoder decoded the encoded bit stream(11 10 00 01) and gives the output(1011) in the second half of the cycle.

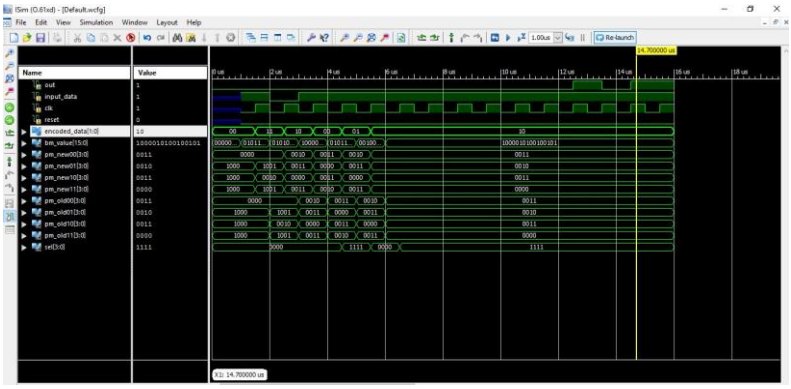

Fig 8: Xilinx simulation results for convolution encoder and Viterbi decoder

CONCLUSION

As the Viterbi algorithm is conceived more interesting and challenging for this research topic, it is considered, and also it has a wide variety of applications in the digital communications field. This research helps to generate more profits by the develop Viterbi using Viterbi algorithm. Anyone besides students can easily analyze these Viterbi algorithm concepts and can gain more knowledge about it. This research mainly concerned with the implementation of the Viterbi algorithm using Verilog coding. The Viterbi algorithm has many advantages like low power consumption and the main advantage is error correcting using Verilog. Anyone reading this document will have to gain the cognition of working with different tools like Xilinx ISE and MODELSIM.

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