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Control of DC-DC Converters

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Abstract

A constant voltage regulator, to supply constant power loads, is realized using a Switched-capacitor converter. Exhaustive studies have been carried out to find the suitability of available control schemes and finally one control scheme investigated with (i) operation of the converter at different crossover frequencies (ii) operation of the converter at different phase Margins. Various operating modes have been analyzed and then a mathematical model is formulated to carry out the dynamic performance and controller design studies. State-space averaging method is employed in the modeling stage. The switched capacitor converter mathematical analysis, modeling and controller design of the single loop control scheme are presented and closed loop simulation results of the switched capacitor dc-dc converter with this control scheme are obtained through PSIM simulator. In the first stage a simple voltage-mode, single-loop; controller is adopted for load voltage regulation. Four important open-loop system small-signal model transfer functions required for controller design are derived, using these transfer functions together with the K-factor design oriented method the controller is designed to meet the frequency response specifications, gain margin and phase margin, and to ensure stability of the system. Taking this designed controller the closed-loop converter system is simulated in the PSIM power electronics simulator and tested the controller regulation capability against source and load disturbances. To verify the simulation results, experimental investigations have been carried out and the measured results are closely matching with the simulated results

Keywords: Constant Voltage, PSIM, VMC.

Introduction

The primary goal of any switching-mode power converter is to provide a constant voltage at its load, despite variations in the source voltage or load. A control element, therefore, has to be introduced in the process of transmitting energy so that the converter changes its topology cyclically, and the durations of the switching topologies are adjusted for regulation purposes. One of the main orientations in power electronics in the last decade has been the development of switching-mode converters without inductors and transformers. Lightweight, small size and high power density are the result of using only switches and capacitors in the power stage of these converters. Thus, they serve as ideal power supplies for mobile electronic systems (e.g. cellular phones, personal digital assistants, and so forth). Switched-capacitor (SC) converters, with their large voltage conversion ratio, promise to be a response to such challenges of the 21st century as high-efficiency converters with low EMI emissions and the ability to realize steep step- down of the voltage (to 3V or even a smaller supply voltage for integrated circuits) or steep step-up of the voltage for automotive industry or internet services in the telecom industry. In recent years, SC based converters, which comprise primarily, switches and capacitors, have been proposed and commercialized. They have the advantage of eliminating inductive element in power conversion. Thus, possibilities of integrated circuit (IC) fabrication and high power density are much more promising. Starting from an original idea of using a basic SC cell in digital filter design for power conversion, many methodologies of operating the switches and the capacitors, and the control schemes have been proposed. Each capacitor is basically going through a charging process from the supply and/or other capacitors, and a discharging process to the load and/or other capacitors, periodically. However, the voltage conversion ratio of the converters in [1] and [2] and those cited as commercially available and are dependent on the circuit structure, having a drawback of weak regulation capability. In order to improve voltage regulation, an on-resistance control scheme has been used in [3]. The MOSFET is driven into the triode region during the charging phase, forming a voltage-controlled resistor. In [4] and [5], the charging time of the capacitors is controlled by a pulse width modulation (PWM) control scheme, providing adjustable voltage conversion ratio. Nevertheless, all of the above converters have the common drawbacks of: (i) drawing pulsating input current that causes conducted electromagnetic interference (EMI) with the supply network and (ii) having high current stress on the switching devices in charging the capacitors. In order to reduce the current stress on switches, use of the current control scheme (CCS) in the charging process has been proposed in [9] - [10], which has the advantageous feature of suppressing current spikes, but it still suffers from the drawback of unidirectional power conversion. Recently, a single-capacitor bi-directional converter has been developed. A single converter structure provides voltage step-down, step-up and bi-directional power flow. A current control scheme is applied in the capacitor charging, resulting in a near-constant capacitor charging current and low EMI.

Small-Signal Analysis of Power Stage

To understand the features of the converter the following mathematical analysis [3], [5], based on the state space averaging technique is performed. The power stage dynamics of the proposed converter are analyzed based on the state- space averaging technique. Equations for the small-signal transfer functions are derived in terms of power stage parameters. Since the proposed converter (Fig.1) goes through two topological stages in each switching period, its power stage dynamics can be described by a set of state equations.

$$X = A_k + B_k V_g \, (k = 1,2) \tag{1}$$

$$V_o = C_K X \tag{2}$$

here X = [iL 1 iL2 VC1 VC2]T, and { AK, BK } are the coefficient matrices for the k th topological stage. The coefficient matrices for two topological stages are given by

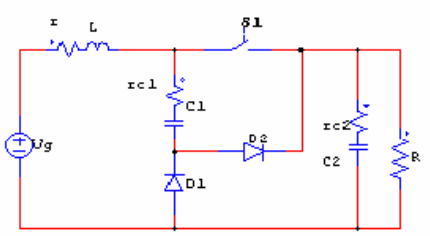


Figure 1: HSBC converter.

A proposed converter is shown in Fig. 1. In Continuous Conduction Mode (CCM) where the inductor current flows continuously over one switching period, the converter exhibits two circuit states. The first state is when the MOSFET is turned on. The second State is when the MOSFET is turned off. State space equations for each circuit configuration can be expressed by State model for ON-state condition is

$$\begin{pmatrix} \frac{di_l}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{1}{L}\left(\frac{Rr_{c2}}{k}+r_L\right) & -\left(\frac{r_{c2}c_2R}{kL}\right) & -\left(1-\frac{r_{c2}c_2(R+r_{c1})}{k}\right)\frac{1}{L} \\ \left(\frac{r_{c2}c_2R}{ck}\right) & \left(\frac{c_2R}{cr_{c1}k}+\frac{1}{r_{c1}c_1}\right) & \left(\frac{r_{c1}c_2(R+r_{c1})}{cr_{c1}k}-\frac{1}{r_{c1}c_1}\right) \\ \frac{R+r_{c1}}{k} & \frac{R}{k} & \left(\frac{R+r_{c1}}{k}\right) \end{pmatrix} \begin{pmatrix} i_l \\ v_{c1} \\ v_0 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \end{pmatrix} v_g \tag{3}$$

State model for OFF-state condition is

$$\begin{pmatrix} \frac{di_l}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{1}{L}\left(\frac{Rr_{c2}}{R+r_{c2}}+r_L\right) & \frac{-1}{L} & -\frac{1}{L}\left(1+\frac{r_{c2}}{R+r_{c2}}\right) \\ \frac{1}{c_1} & 0 & 0 \\ \frac{1}{c_2}\left(\frac{R}{Rr_{c2}}\right) & 0 & -\frac{1}{c_2}\left(\frac{1}{Rr_{c2}}\right) \end{pmatrix} \begin{pmatrix} i_l \\ v_{c1} \\ v_0 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \end{pmatrix} v_g \tag{4}$$

The average state-space model is

$$X = [A]\,[X]+[B][u] \tag{5}$$

Where $A = A_1 D + A_2 (1-D)$; $B = B_1 D + B_2 (1-D)$ Where r_{c1},r_{c2} are the equivalent series resistances (ESR) of the capacitor C_1, C_2 respectively. r_L, R are inductor series resistances and Load resistances. By perturbing and linearising under the small-signal assumption, an equation representing the small-signal control-to-output and control to inductor current dynamics of the power stage can be obtained from the following equations

$$G_d(s) = C[sI-A]^{-1}[(A_1-A_2)X+(B_1-B_2)U]+(C_1-C_2)X \tag{6}$$

$$G_{id}(s) = [(sI-A)]^{-1}[(A_1-A_2)*X+(B_1-B_2)*V_g]*[1\ \ 0\ \ 0]^T \tag{7}$$

Upon substitution of various matrices and after simplification gives the following transfer function.

$$G_d(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{8}$$

$$G_{id}(s) = \frac{k_2 s^2 + k_1 s + k_0}{p_3 s^3 + p_2 s^2 + p_1 s + p_0} \tag{9}$$

After substitution of the power stage parameters the control to output transfer function is simplified as follows

$$G_d(s) = \frac{7.771e018s^2 + 4.632e023s + 4.953e027}{1.025e015s^3 + 1.93e019s^2 + 1.303e023s + 1.068e027}$$

$$G_{id}(s) = \frac{2.497e-009\,s^2 + 2.329e-005\,s + 0.003551}{8.825e-015\,s^3 + 1.259e-10\,s^2 + 1.067e-006\,s + 0.005663}$$

Design of Power Stage Parameters

Inductor Design

To obtain the critical inductance expression the minimum inductor current equal to zero and then simplification results the following equation.

$$L_{cri} = \frac{R(1-2D)(1-D)^2 DT}{2} \tag{10}$$

To operate the converter in CCM the inductance should be chosen based on operating frequency, load. In any case it should satisfy($L > L_{cri}$).

Table 1: Specifications of Proposed Converter.

Operating conditions: $Vg = 42V, V_0 = 28V, D = 0.5, f_s = 100kHz$	
Power stage parameters	**Compensator Parameters**
Switch(S1):IRF530N Diodes(D1,D2):MUR880 C1,C2:100uF,220uF rc1,rc2:0.3,0.25ohms(ESR) RL=40ohms L=100uH	Control IC:TL494 R1=10k R2=15k R3=3.5k C1=712pF C2=317pF C3=793pF

Voltage-Mode Control (VMC)

The most common control method used for PWM converters is the single-loop voltage mode control as shown in Fig. 2. In this method the load voltage from the converter is sensed through a voltage divider and is compared with a reference voltage, within the error amplifier, and the error signal is then compared with the saw tooth ramp to generate the PWM of desired duty ratio. The comparator output provides a fixed frequency PWM signal, which will be fed to the drive circuit of the electronic switch of the converter topology [12].

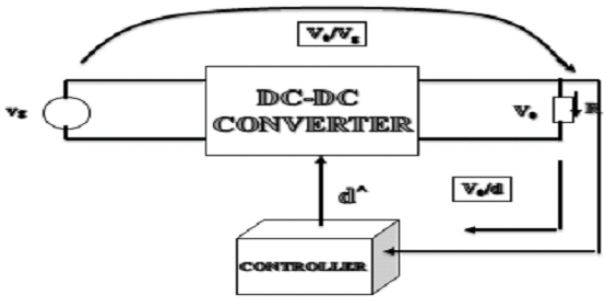


Figure 2: Block diagram of VMC.

Feedback Compensator Design

Once the power stage transfer functions are known, then the feedback compensation can easily be designed to obtain the desired closed-loop performance. Several compensator design approaches have been reported in the literature. However, the K-factor method [9] is simple and effective and hence this method is used in this paper. Few salient design steps of the K-factor approach are given below for ready reference.

Step-1: Plot the frequency response, bode, plot of the open- loop transfer function. Choose the desired crossover frequency, depending on the transient response

requirements, and determine the phase shift and gain of the open-loop SC converter.

Step-2: Choose the desired phase margin depending on the maximum allowable overshoot requirement

Step-3: Calculate the required phase boost and hence determine the K-value. Here this K-value will be useful for selecting the appropriate compensator PI or PID type etc.

Step-4: Using pole-zero locations determine the compensator parameter values.

By using above steps the compensator design can done with help of popular MATLAB soft ware. If the closed loop performance specifications are not matching with the requirements then repeat the above steps until fulfilling the requirements by changing the cross over frequency. By using any power electronic simulator (PSIM) verify the time domain responses through simulations.

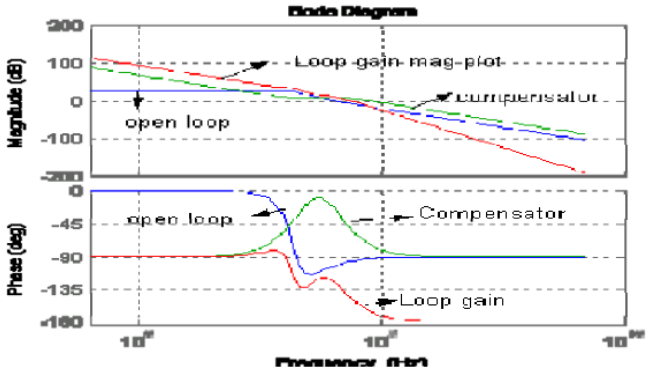
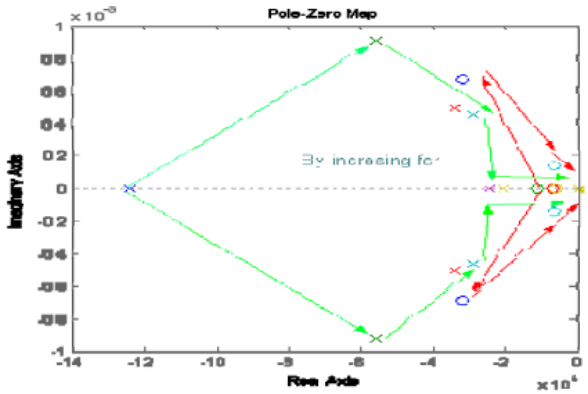


Figure 3: Compensator and loop gain bode plots.

Converter operation at different crossover frequencies and phase margins



(b) fcr as parameter (compensator)

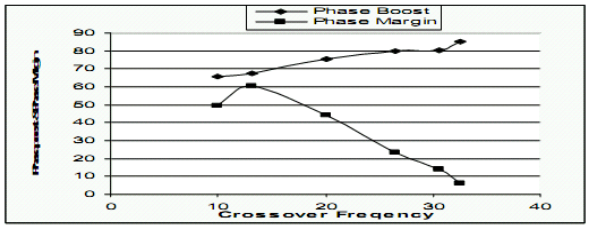
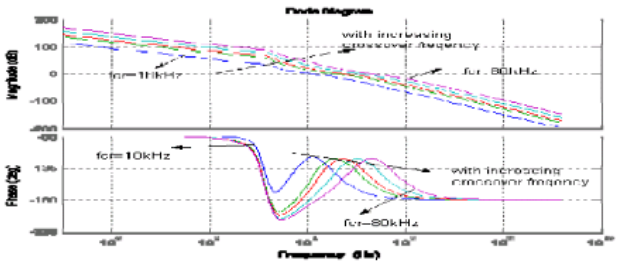


Figure 4(a-e): Movement of poles and zeros of the loop gain, compensator small-signal bode plots with fcr and PM as parameters.

Fig. 4(a) and (b) shows the pole-zero maps of the loop gain and compensator transfer functions. From those figures as the crossover frequency increasing one of the closed loop system pole and zero is moving towards the origin. It implies that at higher cross over frequencies the system becomes unstable, and also observes that some of the poles and zeros are not moving with the change of crossover frequency. Fig. 4(c) shows the compensator pole zero moment as the cross over frequency is increasing. Initially the compensator provides two real poles and zeros under these conditions the system acts like over damped system. Later as fcr increases the compensator real poles and zeros are becoming complex conjugate poles and zeros and the closed loop system acts like under damped system. Further increase of 'fcr'pushes the poles and zeros towards the origin and the closed loop system become unstable. Fig. 4(e) shows how the phase boost and phase margin are changing as the crossover frequency is changing, from the plot as the crossover frequency is increasing, the phase boost required by the closed loop system increases, which is the indication of the system may likely to be enter into unstable region.

Frequency response plots of compensator, loop gain at different crossover frequencies and phase margins



(b) f_{cr} as parameter (loop gain).

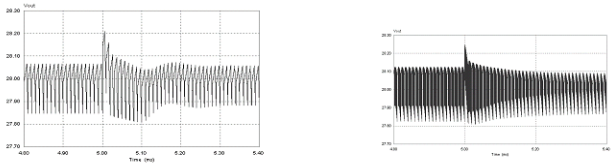
Figure 5(a-d): Variation of phase boost, bandwidth with fcr (PM as parameter).

At different crossover frequencies the compensator and loop gain bode plots are shown in Fig. 5. From these figures it can be revealed that as the crossover frequency is increasing the phase boost provided by the compensator decreases and the gain provided by the compensator is increases as evidenced by Fig. 5(a). As the crossover frequency is increasing the total phase boost required by the system is almost constant and the gain required for the system increases as shown in the loop gain bode plot. As the phase margin is increasing the phase boost provided by the compensator is increasing while the gain margin is decreasing.

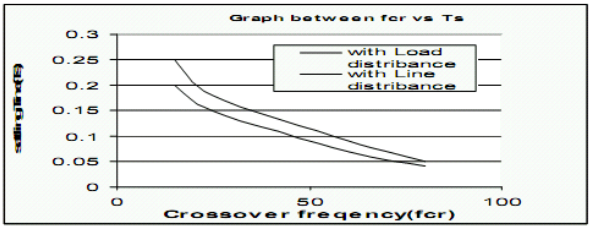
Simulation Results

To verify the controller design, obtained through the design process, the closed-loop converter system is simulated in PSIM. Several simulations have been carried out. Few voltage regulation characteristics are presented here for different operating conditions, which are: (i) for different crossover frequencies, (ii) for different phase margins. These results are shown in Figs. 8(a) to (g). From these results the settling time variation against fcr, PM is also drawn.

Load voltage with load and line disturbance at different crossover frequencies



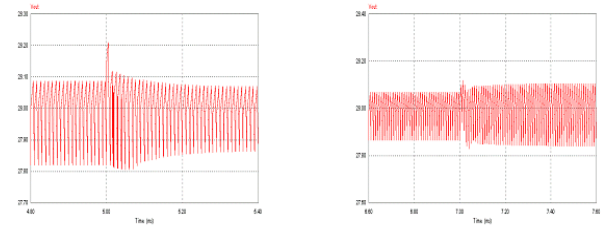
fcr=10 and 30 kHz



(g) Crossover frequency –vs- settling time.

Different controller designs are done against different crossover frequencies and the simulation results are shown in the Figs. 8(a) to (g). From these results it can be concluded that as the crossover frequency is increasing the settling time decreases, which is also shown graphically in the Fig. 8(g).

Load voltage with load and line disturbance at different phase margins



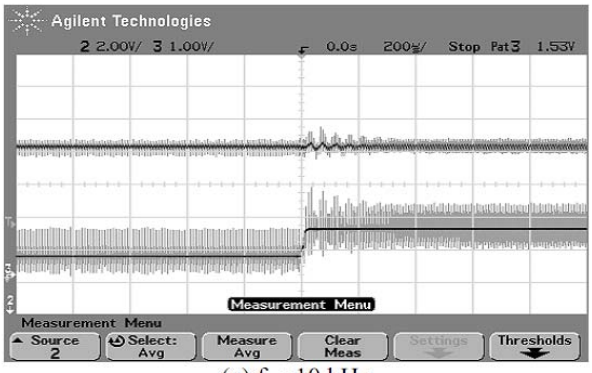
(a) PM=30^0 (b) PM=30^0

The controller design is done with different Phase Margins and the simulation results are given above. From these results it can be concluded that higher values of phase margin decreases the peak overshoot.

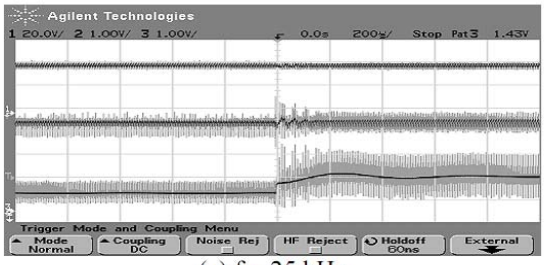
Experimental Results

To verify the controller design, obtained through the design process, the closed-loop converter system is tested experimentally. And the voltage regulation characteristics are presented here for different operating conditions, which are: (i) for different crossover frequencies, (ii) for different phase margins.

Load voltage with load disturbance at different cross over frequencies



(a) f_{cr}=10 kHz

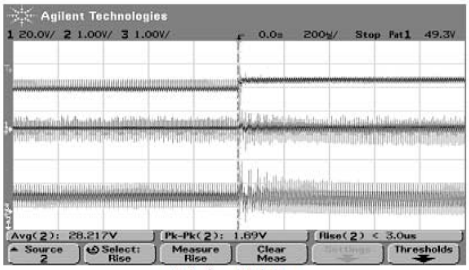


(c) f_{cr}=25 kHz

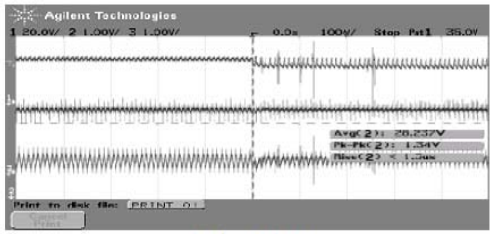
Figure 10: Dynamics of load voltage against crossover frequencies.

Different controller designs are done at different crossover frequencies and these are tested experimentally against load and line disturbances. The experimental waveforms are shown in the Figs. 10(a) to (d). From these results it can be concluded that higher values of crossover frequencies decreases the settling time.

Load voltage with line disturbance at different cross over frequencies

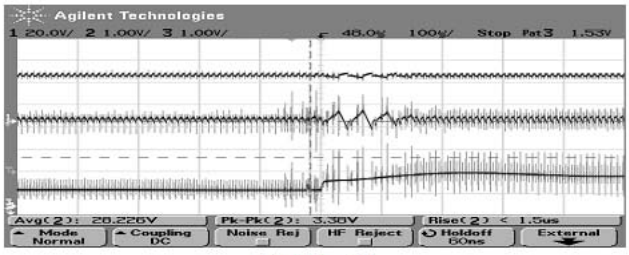


(a) f_{cr}=10 kHz



(b) f_{cr}=25 kHz

Load voltage with load disturbance at different phase Margins



(a) PM=30^0

Figure 11: Dynamics of load voltage against different PMs.

The controller designs are done against different phase margins and the experimental results are shown in Figs. 1(a) to (b). From these results it can concluded that higher values of phase margin decreases the peak overshoot.

Conclusions

Simulation models were developed for single loop control and simulated the closed

loop systems in PSIM simulator. Closed loop simulation results were verified with experimental results. The practical voltage mode control was implemented by using TL494 voltage-mode analog control IC and average current mode control was implemented by using UC3825 current mode control IC. From the exhaustive simulation and experimental studies the following conclusions have been drawn. The voltage mode controlled hybrid switched capacitor dc-dc converter is simulated and tested at different bandwidths and phase margins against load and source disturbances. To verify the simulated results, experimental prototype is implemented and tested for different bandwidths and phase margins, the measured results are in good argument with the simulation results. Boundaries for the stability of the closed loop system were verified by R-H stability criteria

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