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Implementation of ISPWM based Cascaded Multilevel Converter for Voltage Enhancement and Harmonic Reduction

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Abstract

Multilevel inverter (MLI) is a new breed of power converter that is suited for high power applications. Multilevel inverter is an effective and practical solution for increasing power and reducing harmonics in ac waveforms. This paper focuses on the implementation of Inverted Sine Carrier Pulse-Width Modulation (ISCPWM) technique for asymmetric cascaded multilevel inverter with unequal DC sources. This technique combines the advantage of inverted sine PWM technique and asymmetric cascaded multilevel inverter with unequal DC sources. Performance evaluation of the proposed PWM strategy and inverter topology is done using MATLAB/SIMULINK for single phase and three phase asymmetric multilevel inverter. For a seven level output, the proposed inverter topology comprises of two H bridges and two DC sources which is of unequal in nature is simulated using MATLAB. With the implementation of ISCPWM technique there exists an enhancement in fundamental output voltage along with the reduction in Total Harmonic Distortion.

Keywords: Asymmetric Multilevel Inverter, multi-carrier PWM, ISCPWM technique, THD, fundamental output voltage.

Introduction

Cascaded Multilevel Voltage Source Inverter (CMLVSI) structure is very popular especially in high power DC to AC power conversion applications [1]. It offers several advantages that make it preferable over the conventional VSI. With multilevel inverter, AC output voltage can be synthesized from several levels of DC voltages, and the obtained output waveform is of staircase in nature. This allows for higher output voltage and simultaneously lowers the stress on the semiconductor device. The cascade inverter not only can eliminate the bulky transformers of the ASVC's, but can also respond within 1 ms much faster than the conventional PWM converters do[2]. In addition, the proposed asymmetric inverter topology provides high conversion efficiency.

With the application of Unipolar Inverted Sine Carrier PWM (UISCPWM) technique for conventional cascaded multilevel inverter, there exists considerable reduction in THD compared to the implementation of triangular waves as carriers in the multi-carrier PWM technique [3]. Further, with the aim to reduce the number of dc sources required for the cascaded multilevel inverter, this paper focuses on asymmetric cascaded MLI that uses two unequal dc sources in each phase to generate a seven level equal step multilevel output. This structure is favorable for high power applications since it provides higher voltage at higher modulation frequencies with a low switching frequency ,improves the reliability by reducing the number of dc sources and low switching loss for the same total harmonic distortion[4].

Compared to the conventional triangular carrier based PWM, the unipolar inverted sine carrier PWM has a better spectral quality and a higher fundamental output voltage without any pulse dropping [5]. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, along with further reduction in THD variable frequency carrier based PWM is implemented for the asymmetric cascaded multilevel inverter replacing unipolar inverted sine PWM technique[6].

Conventional Cascaded Multilevel Inverter

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series [7]. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$M=2S+1 \tag{1.1}$$

Where'S' is the number of dc sources. Separate DC source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter.

The basic seven-level cascaded-cell inverter is shown in Fig.1.This circuit features three conventional full-bridges serially connected together with their power rails connected to separate isolated dc voltage supplies[8]. Each full-bridge inverter cell can apply three voltage levels to the load terminals.

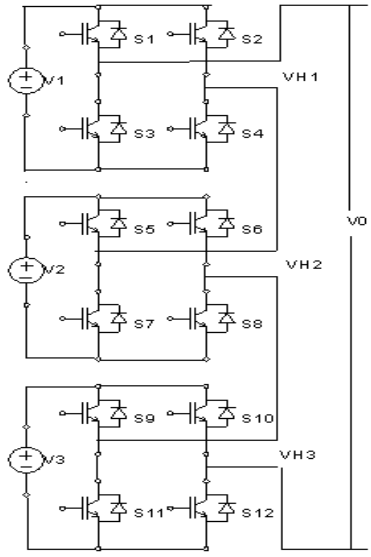

Figure 1: Conventional Cascaded seven level inverter.

Asymmetric Cascaded Multilevel Inverter

Instead of using an identical DC link for every H-bridge converters, different DC links can be used to synthesize a greater number of output voltage levels. To determine the voltage levels among different DC links, a binary system can be effectively used, i.e., $1V_{dc}$, $2V_{dc}$, $4V_{dc}$… $2(N-1)$ V_{dc}, where N is the number of H-bridge converters in one phase leg. The seven - level cascaded multilevel inverter consists of two H-Bridges.

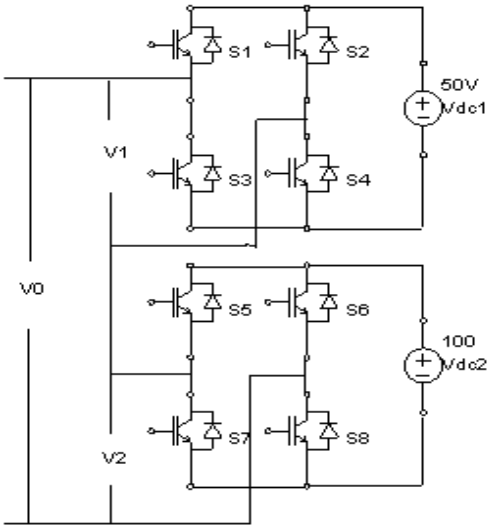

Figure 2: Asymmetric Cascaded seven level Inverter.

The first H-Bridge H_1 consists of a separate DC source V_{dc}, whereas the second H-Bridge H2 consists of a dc source Vdc/2. The advantages of asymmetric topology are: Reduced number of dc sources; Low switching losses; high conversion efficiency; Flexibility to enhance the voltage level; Reduction in complexity and cost [10].

The maximum number of the synthesized voltage levels can be up to

$$\sum_{1}^{n} 2^{n} + 1 \tag{1.2}$$

Multicarrier PWM Technique

Carrier-based methods have been used widely for switching of multilevel inverters due to their simplicity, flexibility and reduced computational requirements compared to Space Vector Modulation (SVM).The widely used multi-carrier PWM methods are known as Phase Shifted (PhS), Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposite Disposition (APOD). The methods used for diode-clamped inverter application (PD, POD and APOD) are derived from the disposition of carriers. For a M-level diode-clamped inverter, M-1 triangular carriers with the same frequency and amplitude are arranged so that they fully occupy the contiguous bands in the range of - $(M-1)V_{dc}/2$ to $(M-1)V_{dc}/2$. If all carriers are selected with the same phase, the method is known as Phase Disposition (PD) method. It is generally accepted that this method gives rise to the lowest harmonic distortion in higher modulation indices when compared to other disposition methods. This method is also well applicable to cascade inverters.

The multicarrier PWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an ‘n’ level inverter is employed, ‘n-1’ carriers will be needed [9]. The carriers will have the same frequency and the same peak to peak amplitude and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter.

Inverted Sine PWM Strategy

The control strategy uses the same reference as the conventional PWM. The control scheme uses an inverted sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater pulse area. The difference in pulse widths resulting from triangle wave and inverted sine wave with the low frequency reference sine wave in different sections can be easily understood. In the gating pulse generation of the proposed ISCPWM scheme the triangular carrier waveform of PWM is replaced by an inverter sine waveform.For the ISCPWM pulse pattern, the switching angles may be computed as the same way as PWM scheme. ISCPWM technique is classified into two types based upon the frequency of carrier waves

- Unipolar ISCPWM - employ carriers of same frequency
- VFISCPWM - employ carriers of variable in frequency

Conventional Cascaded MLI with Unipolar Iscpwm

To produce a seven-level output, conventional PWM strategy uses six carriers. The generation of triangular carrier waves is obtained using simulation. The carrier waveforms employed for conventional PWM technique are shown in the Fig.3

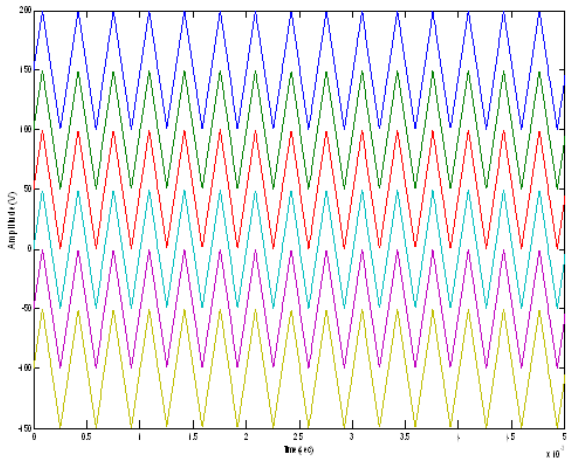

Figure 3: Triangular carrier waves.

The generated carrier waves of frequency 4000Hz are then modulated with reference sine wave of frequency 50Hz for pulse generation. The obtained pulses are then applied to conventional Cascaded seven level inverter and the obtained output voltage waveform is shown in Fig 4.

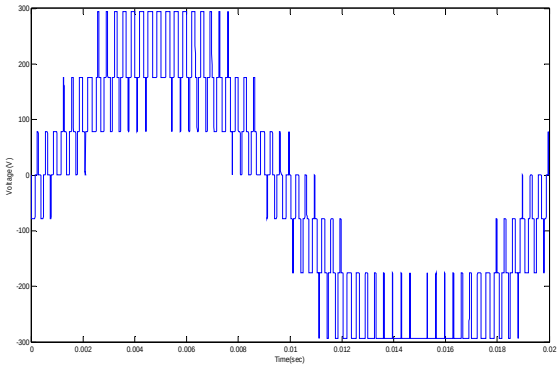

Figure 4: Output voltage of conventional Cascaded seven level inverter employing conventional PWM.

When UISCPWM technique is employed for conventional cascaded multilevel inverter, there exists considerable reduction in THD and improvement in fundamental voltage component throughout the working range. The generated carrier waves of frequency 4000 Hz are then modulated with reference sine wave of frequency 50Hz for pulse generation.

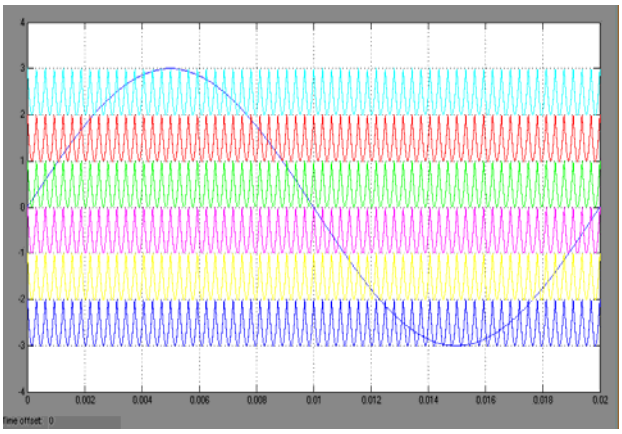

Figure 5: Carrier and Inverted Sine Waveforms for Unipolar ISCPWM Technique.

The obtained pulses are applied to the conventional cascaded multilevel inverter.Output voltage waveform of conventional cascaded seven level inverter employing unipolar ISPWM technique is shown in Fig.6.

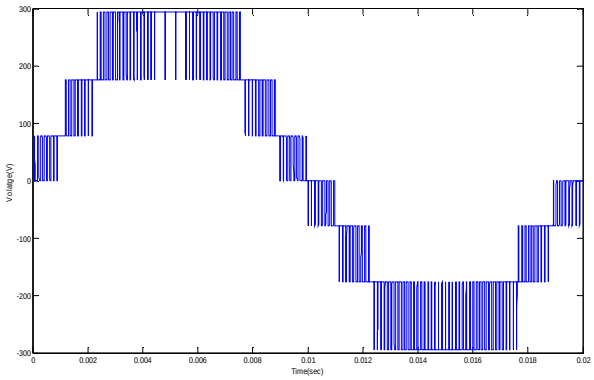

Figure 6: Output voltage of conventional cascaded seven level inverter employing Unipolar ISCPWM.

With the optimum frequency of 3950Hz, in conventional PWM method the obtained fundamental component and THD values are 265.6V and 30.99% respectively.

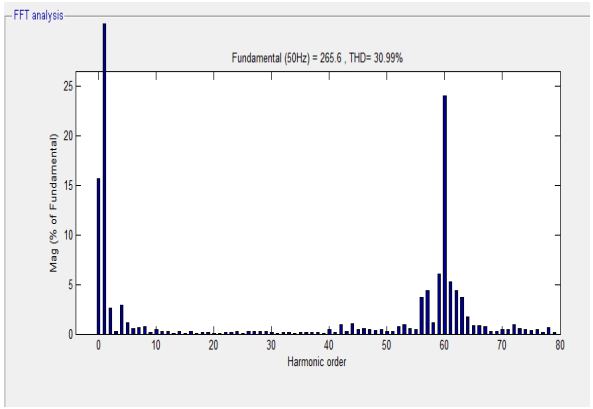

Figure 7: FFT Window for output voltage (conventional PWM).

With the proposed Unipolar ISCPWM technique, the obtained fundamental component and THD values are 278.9V and 21.82% respectively.

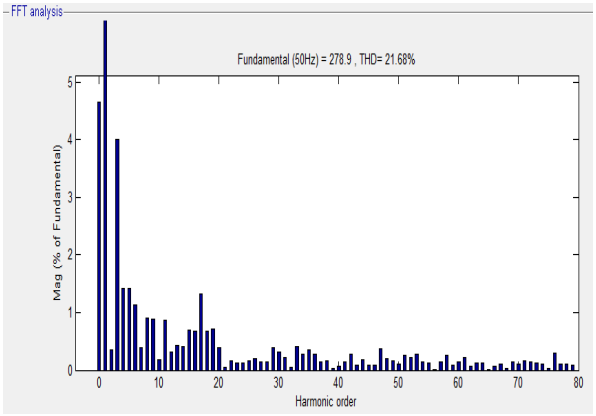

Figure 8: FFT Window for output voltage (ISPWM).

Table 1: Comparison of Unipolar ISPWM with conventional PWM technique for conventional Cascaded MLI:

PWM Technique	THD (%)	Fundamental output voltage(V)
Conventional PWM	30.97	266.6
Unipolar ISCPWM	21.82	278.9

Inferences made from above waveforms on implementing Unipolar ISPWM technique for conventional Cascaded MLI are:

- It has a better spectral quality and a higher fundamental component compared to the conventional PWM

- The Unipolar ISCPWM strategy enhances the fundamental output voltage and reduces THD.
- Harmonics of carrier frequencies or its multiples are not produced.

On implementing Unipolar ISPWM technique for conventional Cascaded MLI, THD is reduced considerably by a factor of around 9%. Hence Unipolar ISCPWM technique is extended for Asymmetric Cascaded MLI.

Asymmetric Cascaded MLI with Unipolar Iscpwm

PWM signal for the asymmetric cascaded multilevel inverter is generated by comparing inverted sine carrier wave of high switching frequency with that of reference sine wave.To produce a seven-level output, UISCPWM strategy uses six carriers. The generated pulses are then applied to asymmetric cascaded MLI. Output voltage waveform of single phase asymmetric cascaded seven level inverter employing UISPWM technique is shown in Fig.9

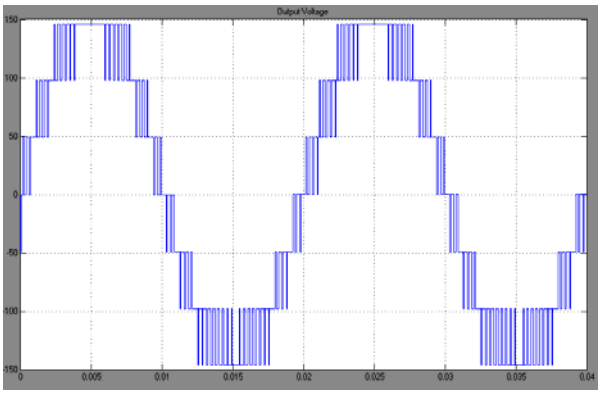

Figure 9: Output Voltage Waveform of single phase Asymmetric Cascaded Seven Level Inverter.

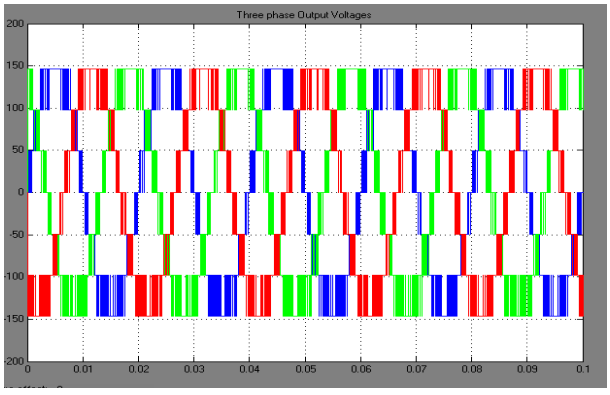

Figure 10: Output Voltage Waveform of three phase Asymmetric Cascaded Seven Level Inverter. (Unipolar ISPWM)

The proposed PWM strategy is also extended for three phase asymmetric cascaded MLI by introducing a phase displacement of 120 degrees between each phase.

Asymmetric Cascaded MLI with VFISCPWM

The proposed control strategy replaces the conventional fixed frequency carrier waveform by variable frequency inverted sine wave to have a better spectral quality and a higher fundamental voltage compared to the unipolar ISCPWM strategy. The reference carrier frequency was chosen as 4000Hz**.** Pulses for the asymmetric cascaded MLI are generated by modulating carrier waves with reference sine wave of frequency 50Hz.

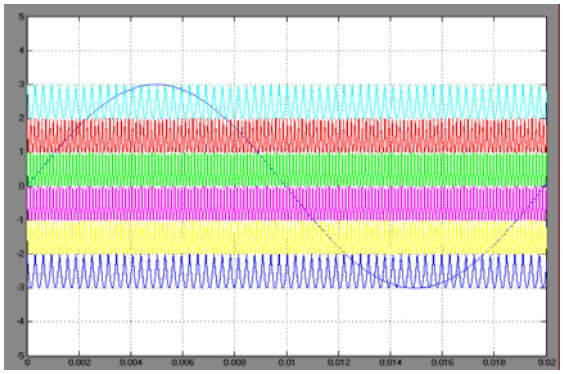

Figure 11: Carrier and Inverted Sine Waveforms for VFISCPWM Technique.

The obtained pulses from VFISPWM strategy are then applied to the asymmetric cascaded MLI. Output voltage waveform of cascaded seven level inverter employing VFISCPWM technique is shown in Fig12. The proposed PWM strategy is also extended for three phase asymmetric cascaded MLI by introducing a phase displacement of 120 degrees between each phase.

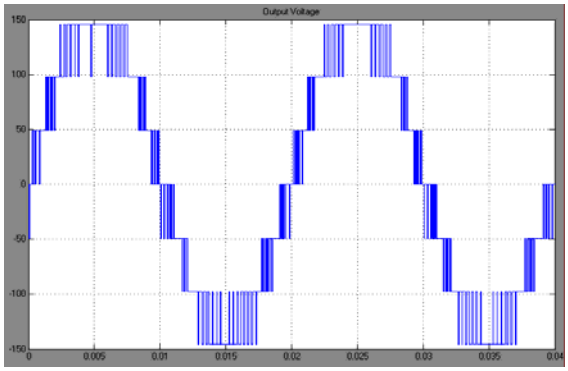

Figure 12: Output voltage waveform of single phase asymmetric cascaded MLI employing VFISCPWM.

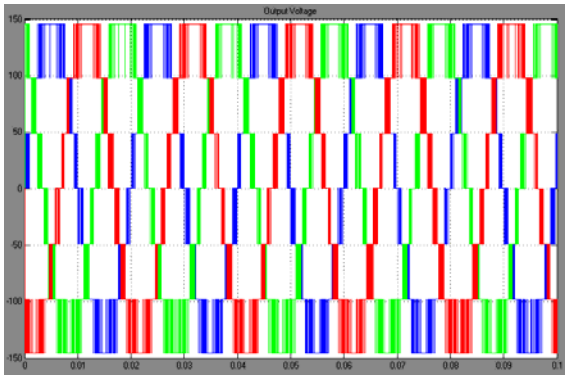

Figure 13: Output Voltage Waveform of three phase Asymmetric Cascaded Seven Level Inverter employing VFISPWM.

Inferences

On implementing VFISPWM technique for asymmetric cascaded MLI, THD is reduced when compared to UISCPWM strategy. The VFISPWM provides an enhanced fundamental voltage, THD and minimizes the switch utilization among the various levels in inverters. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The carrier frequencies are so selected that the number of switching in each band are equal. The proposed modulation technique for the proposed inverter topology maximizes the output voltage and gives a low THD of 5.80%. The FFT window for the output voltage waveform of asymmetric cascaded MLI employing UISCPWM is shown in Fig 14.

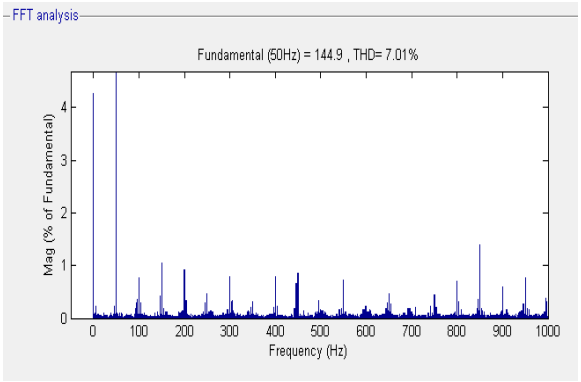

Figure 14: FFT Window for output voltage (Unipolar ISPWM).

The FFT window for the ouput voltage waveform of asymmetric cascaded MLI employing VFISPWM is shown in Fig.23

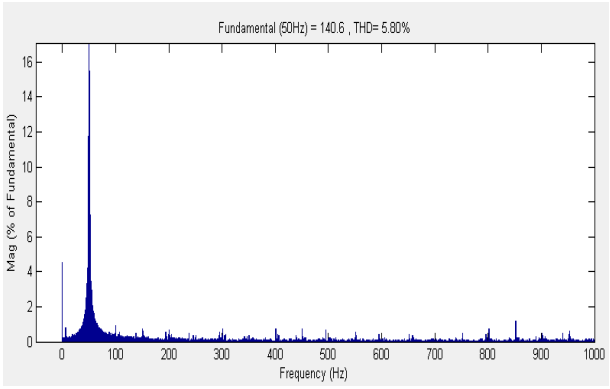

Figure 15: FFT Window for output voltage (VFISPWM).

Table 2: Comparison of VFISPWM with Unipolar ISPWM technique.

PWM Technique	**THD (%)**
Unipolar ISCPWM	7.01
VariableFrequency ISCPWM	5.80

Conclusion

The line voltage yields better spectral performance for VFISCPWM hence this technique reduces the need for output filter. Asymmetric cascaded multilevel inverter using two unequal dc sources for each phase requires minimum number of switching devices. An inverted sine wave carrier frequency modulation strategy gives maximum fundamental voltage for a given THD.By employing this new technique the fundamental voltage is improved throughout the working range and thereby resulting in enhanced fundamental voltage. Also the range of THD is reduced when compared to conventional PWM technique. Reduction in number of DC sources and switches reduces the complexity and cost of the circuit. By increasing the number of steps, waveform approaches the desired sinusoidal shape accompanied with reduction in THD. Further reduction in THD can be obtained by employing PI or PID controller. The proposed inverter topology along with proposed PWM strategy has a greater scope of application in fuel cells and electric vehicles.

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