International Journal of Electrical Engineering.
ISSN 0974-2158 Volume 4, Number 4 (2011), pp. 473-481

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Design and Development of Analog (Time) to Digital Converter using Differential Ring Oscillator and Counter

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Abstract

This paper presents a novel design and development of Analog (Time)-to-Digital converter using differential ring oscillator and counter. The basic structure is completely implemented using the fully digital technology. This proposed 12-bit ADC circuit is based on the CMOS differential ended ring oscillator and Counter for Analog or Time to Digital Converter (ADC or TDC). This circuit consists of start signal with 8-stage diode connected load differential ring oscillator, thermometer coded encoder logic circuits, and counter. Instead of VDD the upper common 8-stage differential ring oscillator is applied to the input signal variation (Analog signal) produces 4-bits and counterpart produces 8-bits (total: 4+8=12bits ADCs or TDCs).Then the whole circuit design is said to be 12-bit ADC otherwise it is 12-bit TDC. Finally edge triggered flip-flops/latches are used to latch the final 12-bit ADCs outputs. The proposed fully digital 12-bit ADC or TDC is suitable for sensor applications. The proposed circuit is designed and simulated using 0.12µm CMOS parameters.

Keywords: Time to Digital Converter, CMOS Differential Ended Ring Oscillators, and 4T-XOR gates, and positive (+ve) edge - triggered D-flip/flops and latches, counters, and thermometer code, encoder logic.

Introduction

For long time, the Analog-to-Digital Converters (ADCs) have been used widely in

digital equipments. Recently, the most ADC applications today can be classified into four broad market segments: a) data acquisition b) precision industrial measurement c) voice band and audio and d) "high speed" (implying sampling rates greater than about 5 Mbps). Application such as wireless communications and digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors continuously challenge analog designers to improve and develop new ADC and DAC. ADCs find many applications in the field of electronics. Examples of such applications include digital telephone transmission, cordless telephones, medical imaging, PLL's, clock generation in microprocessors, etc. Consequently, different applications may require different topologies. The conventional ADC usually requires a sample and hold circuit, Digital to Analog Converter (DACs), and comparator as main blocks. These blocks include analog devices, which are analog technology based. Thus, a new 12-bit TDC structure has the ability to be implemented in the digital technology are highly demanded. The CMOS ring gate delay line has been used for a CMOS time-to-digital converter. Then, Encoder Logic using 4TXOR-Gate, Edge Triggered D-Flip/Flops/Latches, counter register has been employed to digitize the Analog input. New ADC system called 12-bit ADC has been developed. In this paper, we present a 12-bit TDC or ADC structure compatible with the CMOS digital technology. The digital circuit includes a differential ended ring-delay line, Thermometer encoder and digital counter. The work is organized as follow.

The Basic CMOS Ring Oscillators

There are two types of Basic CMOS Ring oscillators

a. Single-Ended Ring Oscillators (SERO's)
b. Differential Ring Oscillators (DRO's).

The latter are much more important in digital circuit applications, since DRO's are less affected by supply and substrate noise. The circuit topology is shown in the figure.1 (a) and 1(b) [4].

Differential Topology

Single Ended Ring Oscillator structures are not widely used in state-of-the-art high-frequency communications systems. Differential architectures are preferred over the single – ended design because of their inherent advantages.

This includes better immunity to common-mode noise, improved spectral purity, and 50% duty cycle at the output.

Differential ring oscillators can be constructed with an even number of stages, unlike their single ended counterpart. The required extra phase shift (π) can be obtained by reversing one of the connections in the architecture introducing a DC phase inversion. Fig.1 (a) shows the N-stage differential ring oscillator [2, 5, and 6].

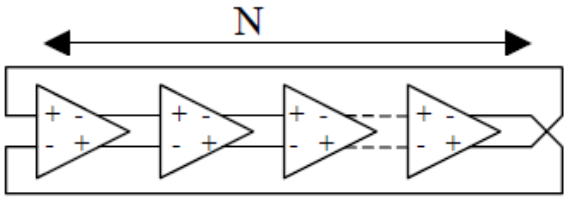

Figure 1(a): Differential ring oscillator block diagram.

The differential topology comprises a diode - connected load and a NMOS differential pair, Fig.1 (b) the delay in the cell is set by the charge in each node and the current through the load. The load can consist of a resistor or Diode for fixed frequency or PMOS devices, which makes the oscillator tuneable with a voltage. The Diode connected PMOS load is usually implemented as symmetric or cross-coupled.

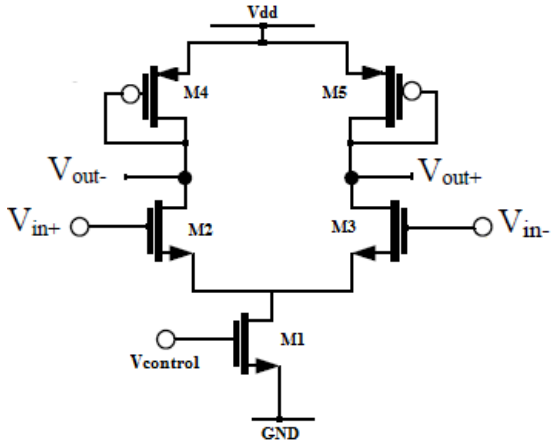

Figure 1(b): Implementation of one stage differential amplifier as a diode connected load.

XOR-Gates

The design of four Transistor XOR (4T) and Three Transistor XOR (3T) which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed [7-12]. In this paper XOR gates form the fundamental building block Design of Encoder Logic. Several designs were proposed to realize the XOR function using different logic styles. Two optimized designs are 1) 3T- XOR 2) 4T- XOR and here encoder is designed using the 4T-XOR gate.

T-XOR

The Design of a four Transistor XOR (4T) is also based on a modified version of a

CMOS inverter and a PMOS pass transistor. Wang, Fang and Feng in [11] proposed novel XOR architectures and simulation result of 4T-XOR gates are as shown in Fig.2 and Fig.3 respectively. That could operate without requiring complementary inputs which is a severe drawback of CMOS transmission gate logic based XOR gates [9]. The values of W/L ratios of the transistors have been shown in the Fig.2 besides the respective transistors. Considerable emphasis has been given in the present work on the design of four transistor XOR gates.

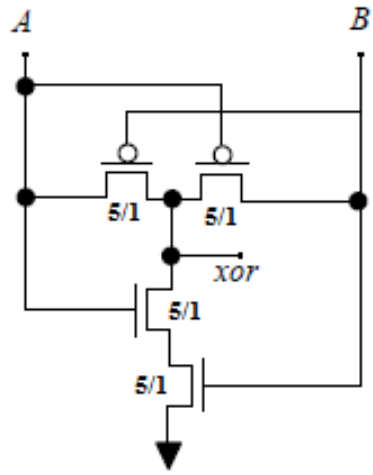

Figure 2: A 4T XOR Gate.

Figure 3: Simulation result of a 4T-XOR Gate.

Design of the Encoder Logic diagram (binary) is based on the design of the XOR gate. 4T-XOR gates are used for the proposed design of Encoder Logic circuit, which produces 4-bits binary outputs (S3, S2, S1 and S0) and s3 is taken directly from c7 for proposed 12-bit ADC's. The design of a four (4T) transistor XOR gate as shown in Fig.2.

Binary Asynchronous/Ripple Counter

Fig.4 shows 8-bit asynchronous counter using D flip-flops. As shown in Fig.4 the differential stage output is connected to the clock input of first stage flip-flop. The clock input of the second stage flip-flop is triggered by the QA output of the first stage. Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse and a transition of the QnA output of the first stage can never occur at exactly the same time. Therefore, the two flip-flops are never simultaneously triggered, which results in Asynchronous counter operation. The simulation result of the 8-bit asynchronous binary counter are as shown in Fig.5.

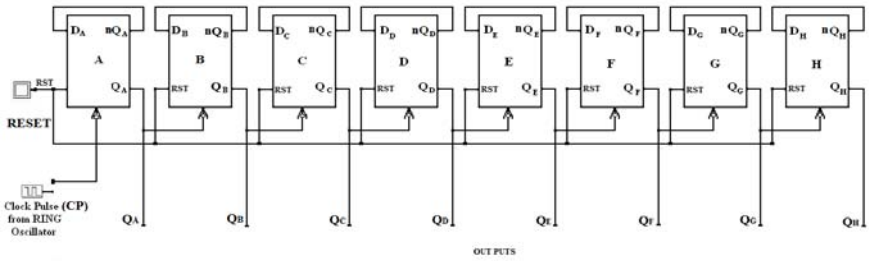

Figure 4: A 8-bit Asynchronous binary counter.

Figure 5: The simulation result of the 8-bit asynchronous binary counter.

Edge Triggered D-Flip-Flops

The Edge-triggered flip-flop that synchronizes the state changes during a clock pulse transition is the Edge-triggered flip-flop. Here inverted form of start signal is given as input to the latch circuit to latch the 12-bit TDC and finally taking a particular digital output from out of 12-bits binary outputs (D0-D11). Some edge-triggered flip-flops cause a transition on the positive edge of the clock pulse is called Positive-Edge-Triggered flip-flops/latches. The logic diagram of a D-type positive-edge-triggered flip-flop is shown in Fig.6.

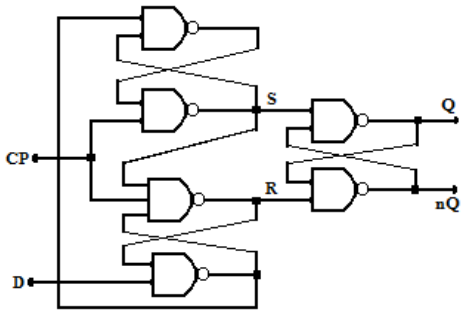

Figure 6: D-type Positive-Edge Triggered Flip-Flop.

Proposed 12-BIT ADC Architecture

Generally, the comparator has been used in the conventional Analog to Digital converters to decide about the conversion. In this paper, a new approach of ADC structure is suggested which is implemented in the digital CMOS technology. The general schematic of ADC and TDC (12-bit) is shown in fig.7. The upper common 8-stage differential ring oscillators are connected to the input signal variation (analog signal) instead of connecting VDD signal and then lower common 8-stage is connected to ground signal (GND), then whole circuit design is said to be 12-bit ADC circuit. Otherwise it becomes 12-bit TDC circuit. The first stage of differential ring oscillator produces an output C0, second stage produces C1, similarly all stages produces outputs (C0, C1, C2, C3, C4, C5, C6, and C7) and then shifted to next stage input. DRO's output C7 is considered as Clock Signals to the next reset with counter circuit. Here Asynchronous 8-bit counter or simply Ripple counter (D or T-Flip-Flops) are used to generate 8-bit Digital outputs, hence DRO's part produces 4-bit and counterpart produces 8-bit,Finally (4+8)=12-bit TDC design is obtained. Finally latch circuits are used to Latch all final outputs (D0-D11). The Encoder block is a combinational logic circuit and it is designed and implemented with XOR-gates and later it generates binary outputs (s2, s1, s0) are as shown in fig.8. S3 is obtained directly from C7. Finally 4-bit binary (S0-S3) is obtained.

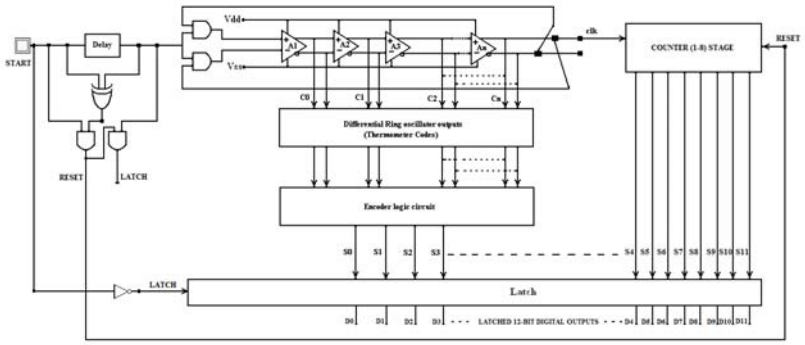

Figure 7: Proposed 12-bit ADC architecture.

$S3 = C7$

$S2 = C3 \oplus C7$

$S1 = C1 \oplus C3 \oplus C5 \oplus C7$

$S0 = C0 \oplus C1 \oplus C2 \oplus C3 \oplus C4 \oplus C5 \oplus C6 \oplus C7$

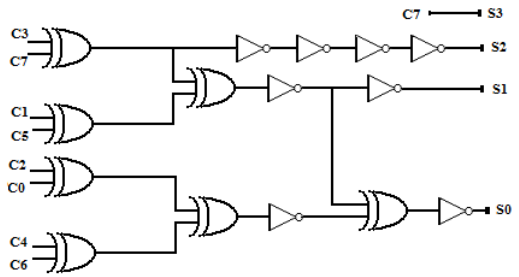

Figure 8: Encoder Logic diagram.

Table 1: Thermometer code to Binary Code conversion.

DRO's Outputs (Thermometer code)								4-Bit Digital Outputs				Decimal
C7	C6	C5	C4	C3	C2	C1	C0	S3	S2	S1	S0	D
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	1	1
0	0	0	0	0	0	1	1	0	0	1	0	2
0	0	0	0	0	1	1	1	0	0	1	1	3
0	0	0	0	1	1	1	1	0	1	0	0	4
0	0	0	1	1	1	1	1	0	1	0	1	5
0	0	1	1	1	1	1	1	0	1	1	0	6
0	1	1	1	1	1	1	1	0	1	1	1	7
1	1	1	1	1	1	1	1	1	0	0	0	8
1	1	1	1	1	1	1	0	1	0	0	1	9
1	1	1	1	1	1	0	0	1	0	1	0	10
1	1	1	1	1	0	0	0	1	0	1	1	11
1	1	1	1	0	0	0	0	1	1	0	0	12
1	1	1	0	0	0	0	0	1	1	0	1	13
1	1	0	0	0	0	0	0	1	1	1	0	14
1	0	0	0	0	0	0	0	1	1	1	1	15

Layout and Simulation Results

To illustrate the proposed TDC (12-bit) function, the circuit shown in fig.7 is designed and simulated by using MICROWIND-2, the complete Layout and simulation results are shown in fig.9 and fig.10 respectively which consists of Differential Ring Oscillators (DRO's), Reset circuitry with Counter (D-Flip-Flops),

Encoder logic circuits, and Edge triggered Flip-Flops/latch circuits. The proposed 12-bit TDCs before latch produces 12-bit outputs in the binary form likes S0, S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11.and all of these are latched by using Latch circuit to get proposed 12-bit ADCs (TDCs) in digital form (D0, D1, D2, D3, D5, D6, D7, D8, D9, D10, and D11). The complete Layout and simulation results are as shown in fig.9 and fig.10 respectively.

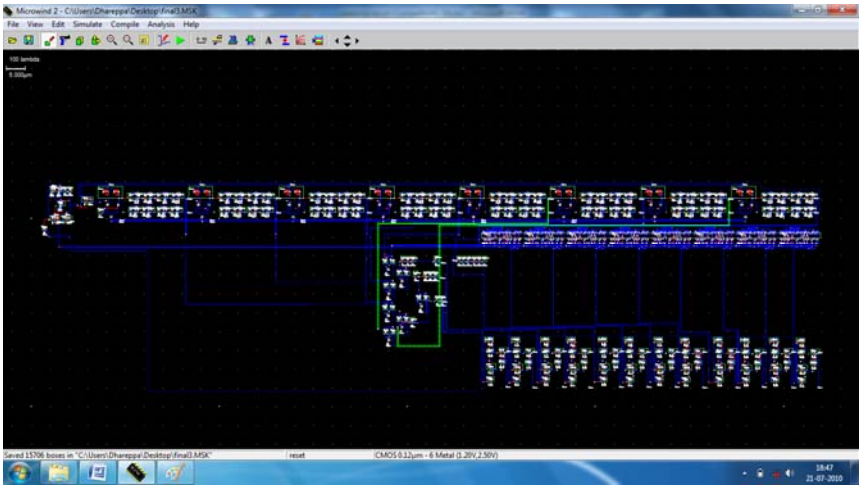

Figure 9: Layout of The Proposed TDC (12-bit) Circuit.

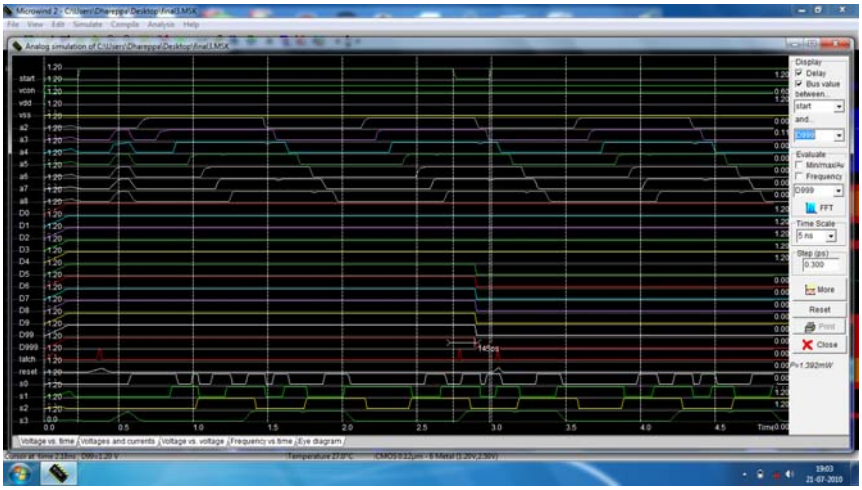

Figure 10: Simulation Results of The Proposed TDC (12-bit) Circuit.

Conclusion

A new ADCs and TDCs circuit has been proposed, which is completely digital. Design and Development of Analog to Digital Converter using Differential Ring Oscillator and Counter is implemented in Microwind-2 and Dsch-2 for desired

specifications. Specifications are derived specifically for sensor application. And other applications include digital telephone transmission, cordless telephones, medical imaging, PLLs, Frequency modulator, Demodulator, and clock generation in microprocessor, system synchronization (deskewing), oversampling A/D converters etc. all of them requiring high performance parameters.

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