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Implementation of Microcontroller based Driver Circuit for Plasma Display Panel.

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Abstract

The model of the new zero-voltage and zero current switching energy recovery display driver for a Plasma Display Panel is proposed. This operation helps to achieve the zero-voltage turn on of all main power switches and zero-current turn-off of all auxiliary power switches, reduce the EMI noise, current stress in Mode 2 and Mode 3 operation, and improve the energy recovery capability. This paper presents the simulation and implementation of microcontroller based driver circuit for plasma display panel. Moreover, it has the simpler structure, fewer power devices, and lower cost of production than the Weber's driver. The experimental results concur with simulation results.

Keywords: Energy recovery, Plasma Display Panel, Zero-voltage switching,

Introduction

Electronic display devices play an important role as an information display for a man-to-machine interface. With the rapid progress in the information industry, there has been a continuous increase in the demand for new electronic display devices with a large size, high resolution, and high information capacity. In order to substitute for a conventional cathode ray tube (CRT), various flat panel displays (FPDs) using a liquid crystal technology, electroluminescence, or gas discharge have been newly developed and commercialized. Thus, nowadays, it is possible to select the display device most suitable to each purpose. Among various hitherto developed FPDs, the Plasma Display Panel (PDP), which uses a gas discharge was first commercialized in 1993, has been well known as a most promising candidate for a large area wall hanging color television due to its large screen size, wide viewing angle, thinness, long life time, and high contrast. Therefore, it can be widely used as a home theater, commercial advertisement, billboard, supervisory monitor, entertainment purpose.

To obtain a high frequency square wave voltage, a special driver needs to be designed; to execute this several approaches have already been proposed. Among them, Weber's driver [1] proposed features the low conduction loss and high performance. However, it has several serious problems such as a hard switching operation of all auxiliary switches and complex configuration, resulting in a high cost. Especially, inevitable parasitic components prevent the Plasma Display Panel from being fully charged or discharged, which also cases the hard switching of all main inverter switches, EMI noises, poor energy-recovery capability, wall-charge loss, and increased sustaining voltage. Hsu's driver [2-4] proposed is very simple and able to fully charge/discharge the plasma display panel with the aid of the current source built in the inductor. However, in order to sustain the plasma display panel at the input sustaining voltage or 0 V, a very large inductor current with the value of the gas discharge current (i.e., 120 A for 42-in plasma display panel) should consistently flow through power switches and diodes, resulting in the excessive conduction loss and serious heat generation. Therefore, Hsu's driver [2-4] is unreasonable to be employed in the commercial scale Plasma Display Panel TV. To overcome all these drawbacks, a new zero-voltage and zero current switching energy recovery display driver [5] for a Plasma Display Panel is proposed. The present work deals with implementation of embedded controlled driver circuit for plasma display panel. The details of simulation, control circuit and hardware are presented in this paper.

Operating Principle

Fig.1 shows the circuit diagram of the proposed driver and Fig.2 its key waveforms. One cycle period of the proposed driver is divided into two half cycles, t_0~t_5 and t_5~t_{10}. Because the operation principles of two half cycles are symmetric, only the first half cycle is explained. Before t_0, the voltage across is maintained at 0 V with M_1 and M_4 conducting. The auxiliary capacitors C_x and C_y are kept on being charged with constant voltage

$$V_c=0.5V_s(2t'_4-t_4-t_3+t_2+t_1-2t_0)/(t'_4-2t_4+2t_3-2t_2+2t_1-t_0)\leq V_s.$$

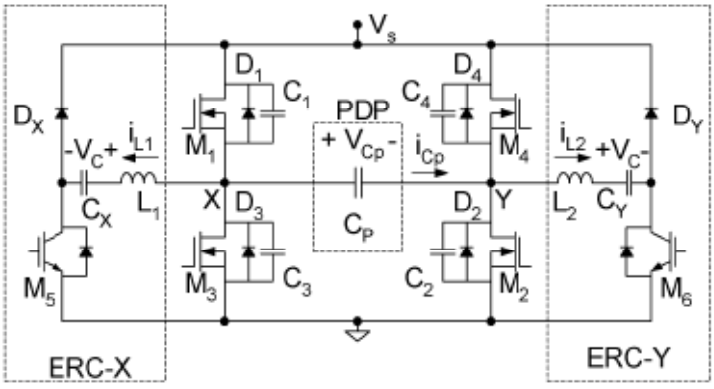

Figure 1: Proposed Circuit.

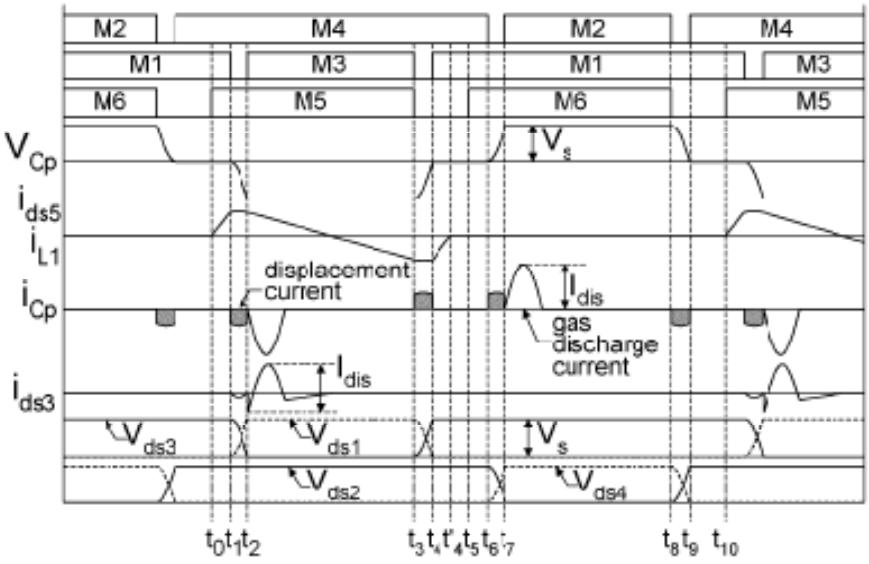

Figure 2: key waveforms.

Methods

Modes of operation

Mode 1 ($t_0 - t_1$)

When M_5 is turned on at t_0, mode 1 begins. As shown in Fig.3, the voltage across plasma display panel is still maintained at 0 V and V_s-V_c is applied to $L_1$with M_1, M_4, and M_5 conducting. Thus, increases linearly with the slope of $(V_s-V_c)/L_1$as i_{L1} (t) = $(V_s - V_c)(t-t_0)/L_1$.

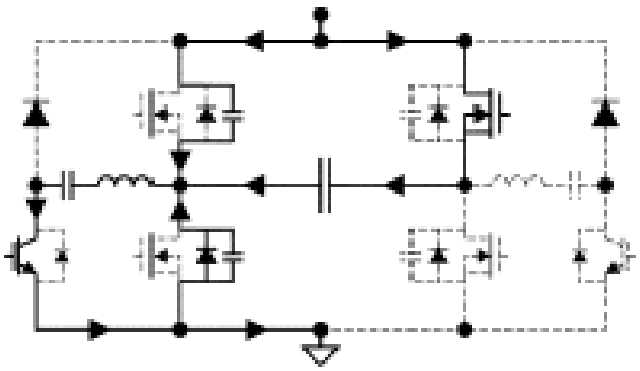

Figure 3: Mode 1.

Mode 2 (t_1 - t_2)

When $M_1$is turned off at t_1, mode 2 begins as shown in Fig.4. With the initial conditions of $i_{L1}(t_1) = i_{L1} = (V_s - V_c)(t_1 - t_0)/L_1$ and $V_{Cp}(t_1) = 0$ V, i_{L1} starts to charge

C_p and C_1 and discharge C_3 as follows:

$$Vcp(t) = -\frac{IL1}{2Coss+Cp}(t - t1)$$

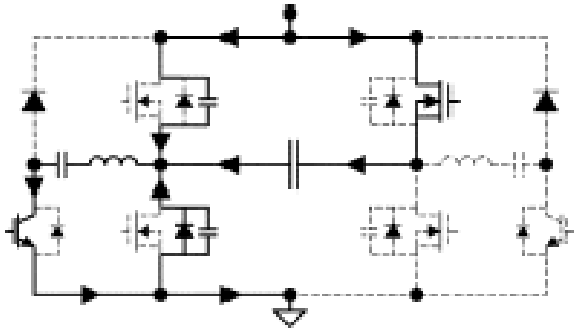

Figure 4: Mode 2.

Where it is assumed that C_1, C_2, C_3 and C_4 are equal to C_{oss} and L_1 acts as a current source with the value of i_{L1}. With this arrangement, the abrupt charging operation of is avoided and the voltages across C_p and C_3 are decreased toward $-V_s$ and 0 V, respectively.

Mode 3 (t_2 ~ t_3)

When V_{Cp} and V_{ds3} are clamped at $-V_s$ and 0 V at t_2, respectively, the gas discharge takes place and mode 3 begins as shown in Fig 5. Since the voltage across M_3 is 0 V at t_2, M_3 can be turned on under the ZVS. Moreover, since the inductor current i_{L1} compensates the large portion of the gas discharge current during this period, the discharge current flowing through M_3 can be considerably reduced. At the same time, since V_C is applied to L_1 with M_3 conducting, the inductor current i_{L1}decreases linearly with the slope of $-V_C/L_1$ as $i_{L1}(t) = i_{L1} - V_C(t - t_2) / L_1$and subsequently, the direction of the current is reversed.

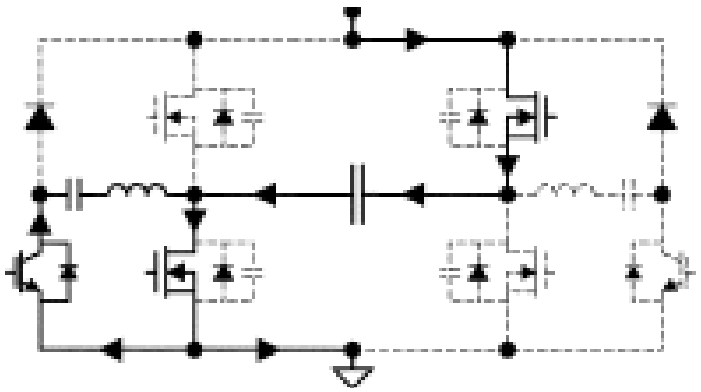

Figure 5: Mode 3

Mode 4 ($t_3 \sim t_4$)

When M_3 and M_5 are turned off at t_3, mode 4 begins as shown in Fig 6. With the initial conditions of $i_{L1}(t_3) = i_{L1'} = i_{L1} - V_C(t_3 - t_2) / L_1$and $V_{Cp}(t_3) = - V_s$, i_{L1} starts to discharge C_p and C_1 , and charge C_3 as follows:

$$Vcp(t) = -\frac{IL1}{2Coss+Cp}\ (t - t1)$$

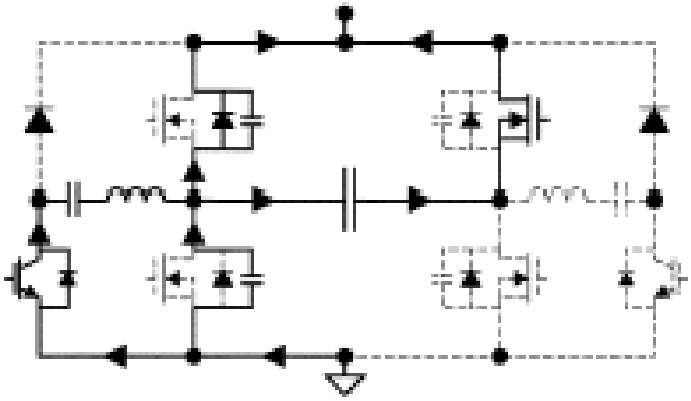

Figure 6: Mode 4

With this arrangement, the abrupt discharging operation of C_p is avoided and the voltages across C_p and C_1 are increased and decreased toward 0 V, respectively. Moreover, since the current i_{L1} is flowing through the anti-parallel diode of M_5, M_5 can be turned off under the zero-current switching (ZCS) at t_3.

Mode 5 ($t_4 \sim t_5$)

When V_{Cp} and V_{ds1} are clamped at 0 V at t_4, mode 4 begins. Since the voltage across M_1 is 0 V at t_4, M_1 can be turned on under the ZVS. The residual energy of the inductor L_1 is fed back to the input power source.

The circuit operation of $t_5 \sim t_{10}$ is similar to that of $t_0 \sim t_5$. Subsequently, the operation from t_0 to t_{10} is repeated.

Simulation Results

The simulation circuit model of Driver circuit for Plasma display system is given in Figure7. Scope 1 is used for displaying these voltages. The simulated waveform is shown in Figure 8.

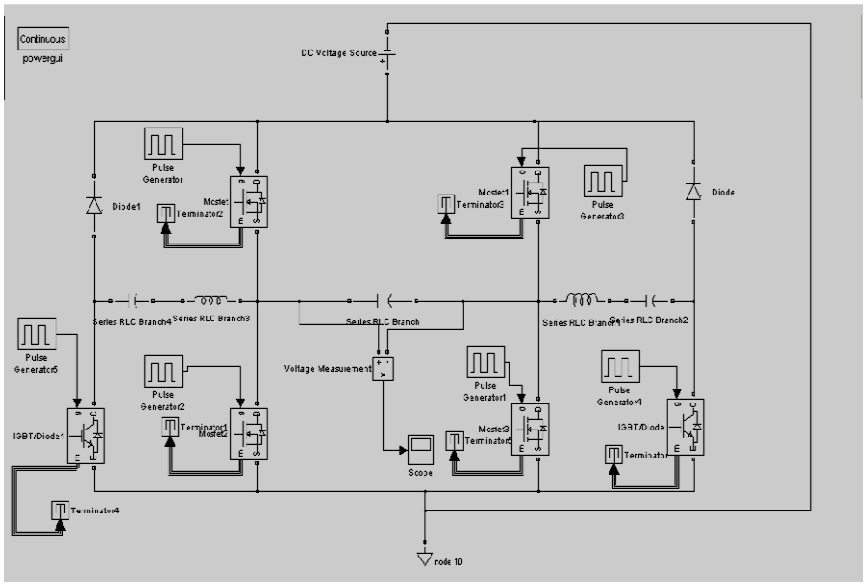

Figure 7: Driver Circuit for Plasma display panel.

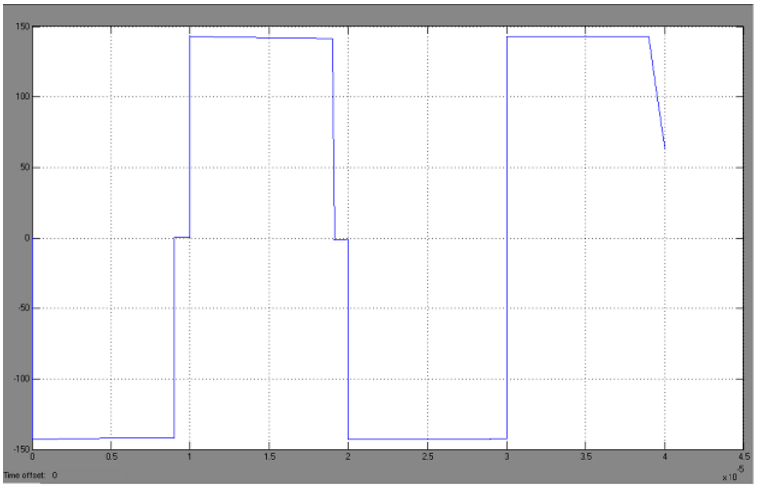

Figure 8: Simulation Result.

Experimental Results

After the simulation studies, a microcontroller based driver circuit for plasma display panel is fabricated and tested. The top view of the hardware is depicted in Figure 9. The oscillogram of output voltage is given in Figure 10. The Atmel microcontroller 89C51 is used to generate the pulses. Port 1 of the microcontroller is used for generating the gate pulses. Timer 0 is used for producing the delay required for the duration TON and TOFF. The microcontroller operates at a clock frequency of 12 MHZ. The pulses produced by the microcontroller are amplified using the driver IC IR 2110.

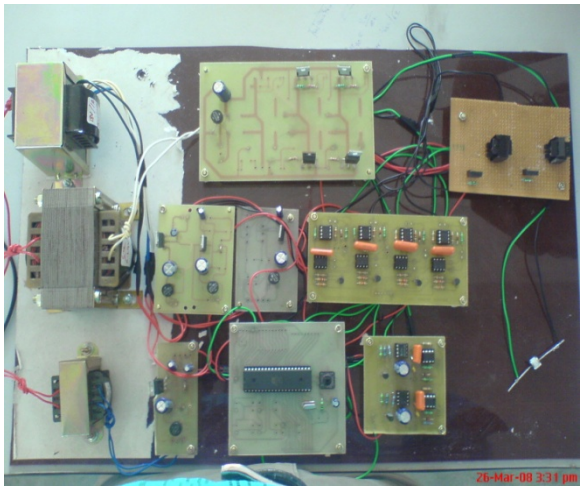

Figure 9: Prototype of Driver circuit for PDP.

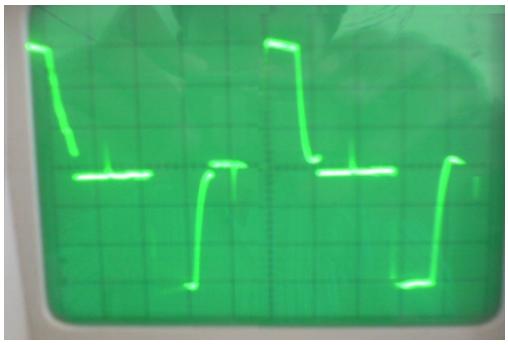

Figure 10: Output voltage across the load.

Conclusions

Microcontroller based driver circuit for plasma display panel is simulated using Matlab Simulink and the hardware is implemented on prototype board and it has several desirable merits such as an improved EMI, low switching losses, and reduced burden on the cooling system.. A Microcontroller based gating circuit generates the pulses required by the inverter. The driver circuit for plasma display panel is successfully fabricated and tested. The applied research demonstrated that simulation and experimental results shown in Figures 2 and 10 are consistent. The hardware system used in the present work has obvious advantage of using single phase supply.

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