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Multiband Hysteresis Modulation of Adjacent Possible Switching Diode Clamped Multilevel Inverter

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Abstract

This paper presents Multiband Hysteresis Modulation of Adjacent possible switching diode clamped multilevel inverter (ADCMI). In ADCMI the adjacent possible switching technique is used to increase the number of levels more than in a conventional DCMI. ADCMI is focused on minimizing the number of power capacitors and semiconductors for a given number of levels. The MB hysteresis modulation scheme for the multilevel converters uses symmetrical hysteresis bands to control the switching so that the inner band causes switching between adjacent levels, while the outer band causes an additional switching level change whenever necessary. The multiband hysteresis algorithm is robust even under unequal capacitor voltages. The effectiveness of the system is verified through simulation using MATLAB/Simulink.

Index Terms: Adjacent possible switching DCMI (ADCMI); Hysteresis Bands; Multiband Hysteresis Modulation; current control

Introduction

Diode Clamped Multilevel Inverter

During the last 10 years, there has been steady growth in multilevel converter topology as they can suit for the high voltage and high power applications. Multilevel VSC are the attractive technology for the medium voltage application, which includes power quality and power conditioning applications in the distribution system. The most well-known multilevel topologies are diode clamped multilevel voltage source converter (DC-VSC), flying capacitor multilevel voltage source converter (FC-VSC) and cascaded H-bridge multilevel voltage source converter (CHVSC)[1-2]. These topologies use different solutions to expand the output voltage range up to several levels. These multilevel topologies can generate multilevel output voltages with low harmonics. Fig. 1 depicts one leg circuit diagram of a five-level DCMI. This topology uses clamping diodes to limit dynamic and static over voltage for switching devices. The clamping diodes are connected to taps of dc bus capacitor .The DCMI generates different voltage levels for output voltage in the ranging between positive and negative of V_{dc}. This topology consists of 2(N -1) switching devices, (N -1) capacitors and 2(N -2) clamping diodes for each phase of N - level inverter. In adjacent possible switching diode clamped multilevel inverter, the adjacent possible switching technique is used to increases the number of levels more than in a conventional DCMI [3].

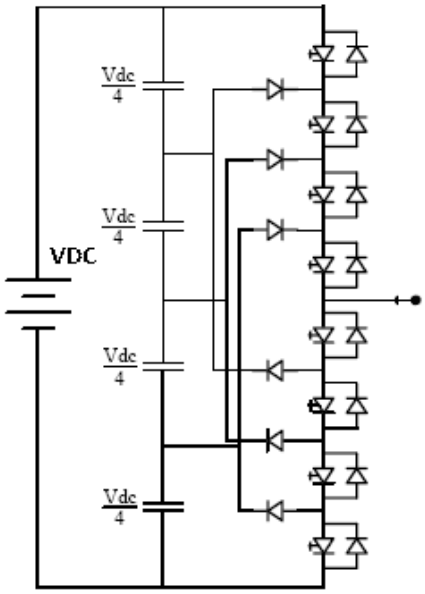

Figure 1: Diode Clamped Multilevel Inverter

Hysteresis Modulation

The hysteresis modulation for power electronic converters are preferred for applications, where performance requirements are more demanding such as to achieve

good dynamic response, unconditional stability, and wide command-tracking bandwidth [4], [5]. In this approach, the controlled system variable is compared against hysteresis band(s) to create the switching commands for the converter. This control has been widely used to control the conventional two-level converter, showing its robustness and simplicity in a lot of applications [6]–[9]. A brief description of the standard two-level hysteresis control for output current regulation is presented in the following. The objective of standard two-level hysteresis current control is to switch the converter transistors in such a manner that the converter load current tracks a reference within a specified hysteresis band.

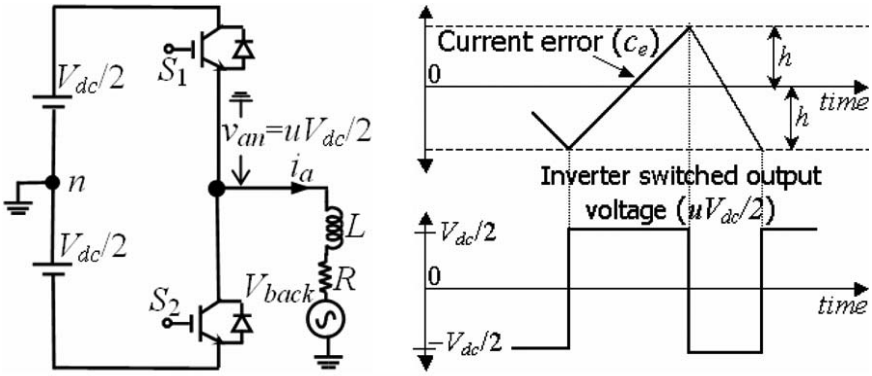

Figure 2: (a) Two-level half-bridge inverter. (b) Two-level hysteresis control.

Consider a single-phase half-bridge inverter, as shown in Fig. 2(a) for two-level hysteresis current control. In Fig. 2, two dc sources of magnitudes $V_{dc}/2$ are considered at the dc link of inverter and their common point (n, neutral point) is grounded. The net controllable output voltage of the inverter is $uV_{dc}/2$, where u is defined as the control input and represents the switching logic of inverter. It assumes the values +1 and −1 for the two-level inverter of Fig. 2(a). The inverter output voltage Van can be represented as follows:

$$V_{an} = u\frac{V_{dc}}{2} = Ri_a + L\frac{di_a}{dt} + V_{back} \tag{1}$$

where i_a is the load current, V_{back} is the back EMF , and L & R are the load inductance and resistance, respectively [see Fig. 2(a)]. As V_{back} increases or as larger reference current slopes are required, larger average values of Van need to be used. Since the voltage across the load resistance is often small, this value can often be neglected. The current error ($C_e = i_a - i_{ref}$) can be reduced by increasing or decreasing Van, depending on the polarity of C_e . Fig. 2(b) represents the implementation logic for this correct voltage-level selection for a two-level inverter using hysteresis control. It can be seen that as the measured current (i_a) becomes greater than its reference (i_{ref}) by the hysteresis band "h," the inverter output voltage ($uV_{dc}/2$) is switched to its lowest level

($-V_{dc}/2$, u = −1) in order to decrease the current according to equation (1). Likewise, when ia becomes less than i_{ref} by "h", $uV_{dc}/2$ is switched to its highest level ($V_{dc}/2$, u = +1) in order to increase the current. For the inverter of Fig. 2(a), u assumes the value +1 for the switching logic S1 = 1, S2 = 0 and −1 for S1 = 0 and S2 = 1.

This paper addresses the performance and simulation of Adjacent possible switching DCMI employing Multiband Hysteresis Modulation for current control.

Adjacent Possible Switching DCMI

Adjacent possible switching diode clamped multilevel inverter (ADCMI) is shown in Fi.g.3. In ADCMI scheme, the adjacent possible switching technique is used to increase the number of levels more than in a conventional DCMI. The switches are switched such that there is a prominent decrease in THD than in a conventional DCMI. The switching strategy for the 15-level adjacent possible switching DCMI topology is given in table I.

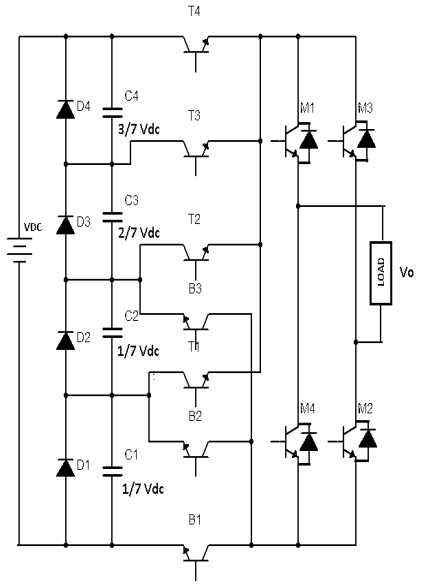

Figure 3: Adjacent possible switching diode clamped multilevel inverter

The output voltage level across C1, C2, C3 and C4 are (1/7) V_{dc}, (1/7) V_{dc}, (2/7) V_{dc} and (3/7) Vdc respectively. For example, to obtain an output voltage level of (1/7) V_{dc} turn on switches T1 and B1 or T2 and B2. To obtain an output voltage level of (3/7) V_{dc}, turn on switches T3 and B2. To obtain an output voltage level of (5/7) Vdc turn on switches T4 and B3 and so on. Thus by switching ON the adjacent possible switches, required output levels can be achieved. By using conventional H-bridge with main switches M1, M2 and M3, M4 at the output of this adjacent possible switching DCMI, multiple levels in both the positive and negative cycle is obtained. The switching pulses are generated with reference to the sine wave form. So its output frequency is varied with respect to the frequency of reference sine waveform.

Table 1: Switching Pattern. a. Multilevel Inverter, b. Main Bridge.

MLI[a]							MB[b]		V_O
T1	T2	T3	T4	B1	B2	B3	M1 & M2	M3 & M4	V_{dc}
1	0	0	0	1	0	0	1	0	1/7
0	1	0	0	1	0	0	1	0	2/7
0	0	1	0	0	1	0	1	0	3/7
0	0	1	0	1	0	0	1	0	4/7
0	0	0	1	0	0	1	1	0	5/7
0	0	0	1	0	1	0	1	0	6/7
0	0	0	1	1	0	0	1	0	7/7
1	0	0	0	1	0	0	0	1	-1/7
0	1	0	0	1	0	0	0	1	-2/7
0	0	1	0	0	1	0	0	1	-3/7
0	0	1	0	1	0	0	0	1	-4/7
0	0	0	1	0	0	1	0	1	-5/7
0	0	0	1	0	1	0	0	1	-6/7
0	0	0	1	1	0	0	0	1	-7/7
1	0	0	0	1	0	0	1	0	1/7
0	1	0	0	1	0	0	1	0	2/7
0	0	1	0	0	1	0	1	0	3/7
0	0	1	0	1	0	0	1	0	4/7
0	0	0	1	0	0	1	1	0	5/7
0	0	0	1	0	1	0	1	0	6/7
0	0	0	1	1	0	0	1	0	7/7
1	0	0	0	1	0	0	0	1	-1/7
0	1	0	0	1	0	0	0	1	-2/7
0	0	1	0	0	1	0	0	1	-3/7
0	0	1	0	1	0	0	0	1	-4/7
0	0	0	1	0	0	1	0	1	-5/7
0	0	0	1	0	1	0	0	1	-6/7
0	0	0	1	1	0	0	0	1	-7/7

The conventional topology consists of 2(N-1) switching devices, (N-1) capacitors and 2(N-2) clamping diodes for each phase of N- level inverter. But the new topology achieves more number of levels with reduced number of capacitors and switching devices. The number of capacitors employed should be even. The number of levels obtained per leg (m) is given by the equation (2).

$$\text{No of levels/leg (m)} = \left(\sum_{n=2,4,6}^{c}\left(\frac{n}{2}+2\right)+n_{(n-2)}\right)+1 \qquad (2)$$

Where C is the total number of capacitors and n_0 =0V

Table 2: Comparison of DCMI and ADCMI.

Levels(m) Per Leg	Capacitors		Switches	
	DCMI (m-1)	ADCMI n	DCMI 2(m-1)	ADCMI 2n
4	3	2	6	4
8	7	4	14	8
13	12	6	24	12
19	18	8	36	16
26	25	10	50	20

The voltage division among the capacitors to employ adjacent possible switching is given in Table III.

Table 3: Voltage division among the capacitors for ADCMI

Voltage Division (E)	No of capacitors	No of levels / Leg
12	2	4
3 2 1 1	4	8
4 3 2 1 1 1	6	13
5 4 3 2 1 1 1 1	8	19
6 5 4 3 2 1 1 1 1 1	10	26

Multiband Hysteresis Modulation

The process of MB hysteresis modulation, first proposed in [10] and later used in [11], [12], [13], [14], is shown in Fig. 4 in the form of current regulation. The MB hysteresis modulation scheme for the multilevel converters uses symmetrical hysteresis bands to control the switching so that the inner band causes switching between adjacent levels, while the outer band causes an additional switching level change whenever necessary.

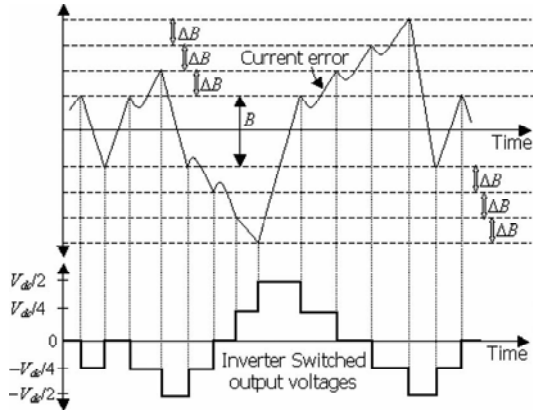

Figure 4: MB Five-level hysteresis current control.

Whenever the current error crosses the inner boundary B, the inverter output is decreased or increased by one level (depending on which hysteresis boundary has just been crossed). Generally, this voltage change will cause the current error to reverse its direction without reaching the next outer band. However, if the error does not reverse, it will continue through the boundary of B to the next outer boundary (placed at ΔB out of B). At this point, next higher or lower level voltage will be switched. This process continues until the current error direction reverses. It is important to note that if the voltage level applied at a boundary crossing of the current error is insufficient to force the error back, no next voltage level is applied as the error again crosses this boundary next time after the previous voltage level change with the same slope. The error in that case is allowed to go until the next voltage level change at next higher or lower boundary crossing of the error to force it back as is evident from Fig. 4.

An advantage of this MB hysteresis control is that the (n − 1) bands used here for an n-level inverter center about the zero error axis. In this case, the average value of the current error approaches zero even when current ripple periods are considered [10]. Therefore, no dc-tracking error is introduced into the output current (no analog offset compensation circuitry required). Also, it gives relatively better performance and the switching frequency depends on the hysteresis band sizes.

Simulation Results

To illustrate the principle of operation of Adjacent possible switching DCMI employing MB Hysteresis Modulation scheme, simulation studies are performed using MATLAB/Simulink. The SIMULINK model for the power circuit of ADCMI employing Multi band hysteresis modulation is shown in Fig.5.

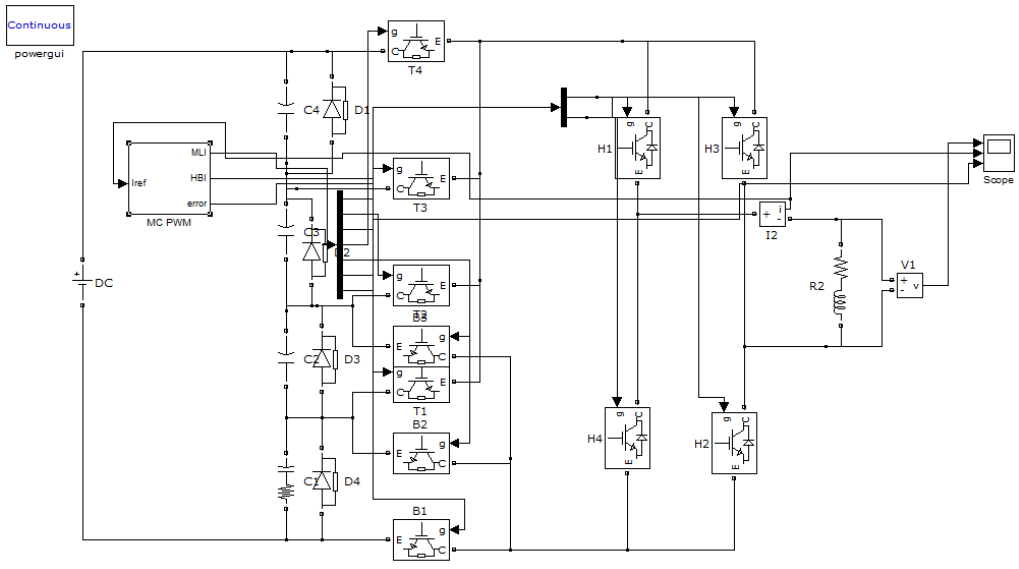

Figure 5: Simulation Circuit of ADCMI with Hysteresis Modulation

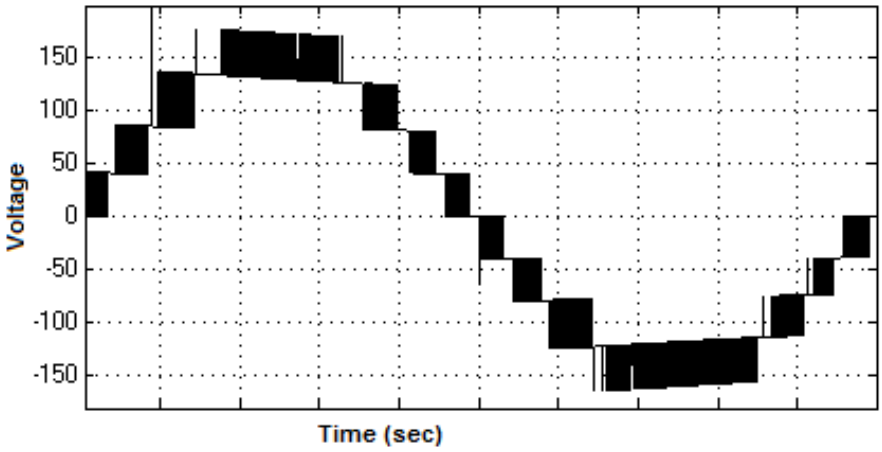

Figure 6a: Output Voltage Waveforms (X-axis: 1Unit=0.02s; Y-axis: 1Unit=50V).

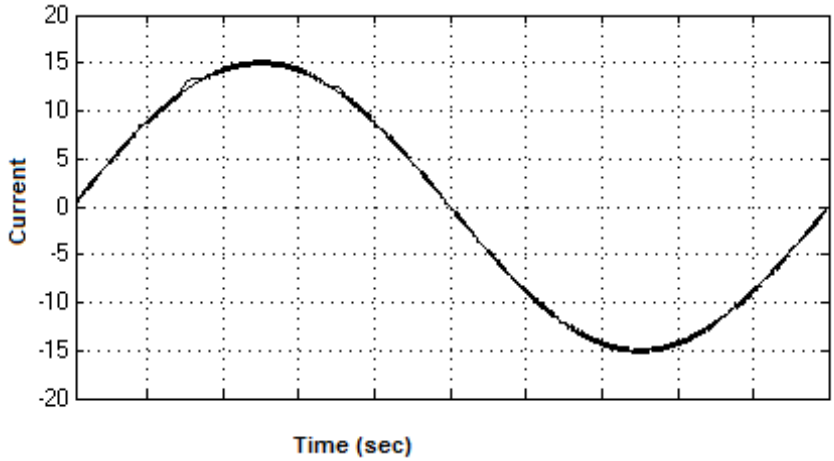

Figure 6b: Output Current Waveforms (X-axis: 1Unit=0.02s; Y-axis: 1Unit=5A).

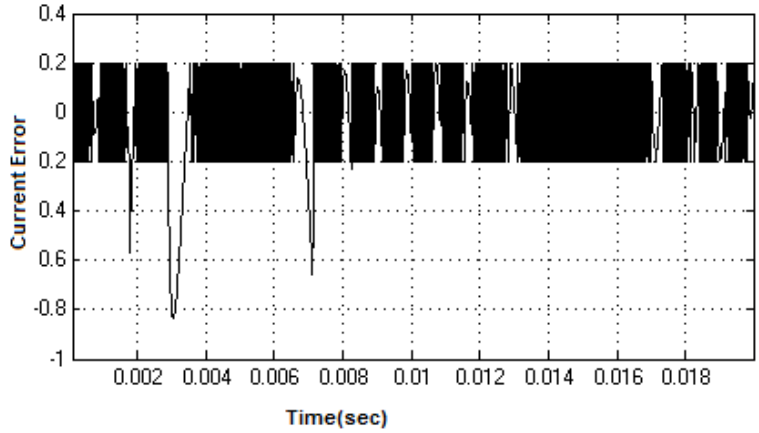

Figure 6c: Current Error (X-axis: 1Unit=0.02s; Y-axis: 1Unit=0.2A).

The output voltage and output current for a current reference of I_{ref}=15A is shown in figure 6a and 6b respectively. The figure 6c represents the current error. It is observed that ΔE=0.4A. It is evident that the controller is able to keep the current error in the defined hysteresis band.

Conclusion

A Multi Band hysteresis modulation technique for adjacent possible switching DCMI was presented in this paper. Compared to conventional DCMI, with reduced number of switches and capacitors, more number of levels was achieved with this ADCMI. Further, Multi Band hysteresis modulation for current control is adopted which uses symmetrical hysteresis bands to control the switching. From the simulation results it is evident that the controller is able to keep the current error in the defined hysteresis band. Also, no dc-tracking error is introduced into the output current. It was also shown to be valid for any number of phases or levels. Analyses and simulations demonstrated the superiority of the proposed system.

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