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Dynamic Modeling and Simulation of Unified Power Quality Conditioner

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Abstract

The main objective of this paper is to operate the UPQC in such a way that it tightly regulates the bus voltage of critical loads against unbalance, harmonics, voltage sag/swell and other disturbances occurring in a distribution system. The series component of the UPQC inserts voltage so as to maintain the voltage at the load terminals balanced and free of distortion. Simultaneously, the shunt component of UPQC injects current into the AC system such that the currents entering the bus to which the UPQC is connected are balanced sinusoids. Both these objectives must be met irrespective of unbalance in either source or load sides.

Keywords: Unified Power Quality Conditioner (UPQC), Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR), Pulse Width Modulation(PWM), Active Power Filter(APF)

Introduction

Power electronic based power processing offers higher efficiency, compact Size and better controllability. But on the flip side, due to switching actions, these systems behave as non- linear loads. Therefore, whenever, these systems are connected to the Utility, they draw non- sinusoidal or lagging current from the source. As a result these systems pose themselves as load sharing poor displacement as well as distortion factors. Hence they draw considerable reactive volt-amperes from the utility and inject harmonics in the power networks.

Until now, to filter these harmonics and to compensate reactive power at factory level, only capacitor and passive filters were used. More recently, new PWM based converters for motor control are able to provide almost unity power factor operations. This situation leads to two observations: on one hand, there is electronic equipment which generates harmonics and, on the other hand, there is unity power factor motor drive system which doesn't need power factor correction capacitor. Also, we cannot depend on this capacitor to filter out those harmonics. Loads, such as, diode bridge rectifier or a thyristor bridge feeding a highly inductive load, presenting themselves as current source at point of common coupling (PCC), can be effectively compensated by connecting an APF in shunt with the load. On the other hand, there are loads, such as Diode Bridge having a high dc link capacitive filter. These types of loads are gaining more and more importance mainly in forms of AC to DC power supplies and front end AC to DC converters for AC motor drives. For these types of loads APF has to be connected in series with the load. The voltage injected in series with the load by series APF is made to follow a control law such that the sum of this injected voltage and the input voltage is sinusoidal. Thus, if utility voltages are non-sinusoidal or unbalanced, due to the presence of other clients on the same grid, proper selection of magnitude and phase for the injected voltages will make the voltages at load end to be balanced and sinusoidal.

The shunt APF acts as a current source and inject a compensating harmonic current in order to have sinusoidal, in-phase input current and the series APF acts as a voltage source and inject a compensating voltage in order to have sinusoidal load voltage.

Its main purpose is to compensate for supply voltage and load current imperfections, such as sags, swells, interruptions, imbalance, flicker, voltage imbalance, harmonics, reactive currents, and current unbalance. This combination of series and shunt APF is called as Unified Power Quality Conditioner (UPQC). In most of the articles control techniques suggested are complex requiring different kinds of transformations. The control technique presented here is very simple and does not require any transformation.

Load Compensation using Unified Power Quality Onditioner

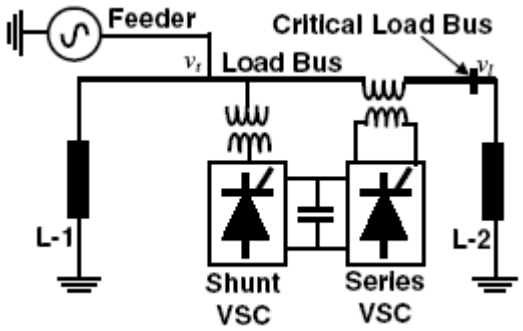


Figure 1: Single-line diagram of a UPQC

Compensated distribution system

The UPQC connection in this figure is called the left-shunt structure as the shunt VSC is connected on the left hand side of the series VSC. It is also possible to have a UPQC with a right- shunt structure. The main purpose of a UPQC is to compensate for voltage flicker/imbalance, reactive power, negative-sequence current and harmonics present in a distribution system. In other words, the UPQC has the capability of improving the power quality at the point of installation on power distribution systems. A UPQC modeled using a state-space averaging technique to analyze its behavior. The enhancement of shunt active filter performance is achieved by applying a moving time window method. A UPQC control system is used for simultaneous voltage regulation and current compensation in the presence of unbalance and harmonics in both load currents and source voltages.

With respect to the circuit of Fig.1, load L-2is a critical load that requires a balance voltage of specified magnitude. The load L-1 can be unbalanced and may draw harmonic current. The main purpose of the UPQC is to regulate the critical load bus voltage v_l. This is achieved through the series VSC. The primary goal of the shunt VSC is to supply real power to the dc capacitor. Additionally, the shunt VSC also eliminates the unbalance and harmonics from the bus voltage on the left-hand side of the UPQC. This voltage is denoted by v_t and will be termed as the terminal voltage.

The operation of UPQC that combines the operations a Distribution Static Compensator (DSTATCOM) and Dynamic Voltage Restorer (DVR).The series component of the UPQC inserts voltage so as to maintain the voltage at the load terminals balanced and free of distortion. Simultaneously, the shunt component of UPQC injects current into the AC system such that the currents entering the bus to which the UPQC is connected are balanced sinusoids. Both these objectives must be met irrespective of unbalance in either source or load sides.

For the proposed UPQC the reference compensator currents are generated using instantaneous symmetrical components theory to achieve the load current compensation and reactive power compensation. The reference compensator voltages are generated such that load voltages are balanced sinusoidal.

A Hysteresis switching controller scheme is proposed that tracks a reference for the proposed UPQC configuration.

Load Compensation using D-Statcom

The schematic diagram of a distribution system compensated by an ideal shunt compensator (DSTATCOM) is shown in fig-2.In this it is assumed that the DSTATCOM is operating in current control mode. Therefore its ideal behaviour is represented by the current source i_f. It is assumed that the load –2 is reactive, non-linear and unbalanced. In the absence of the compensator, the current i_s flowing through the feeder will also be unbalanced and distorted and, as a consequence, so will be Bus –1 voltage.

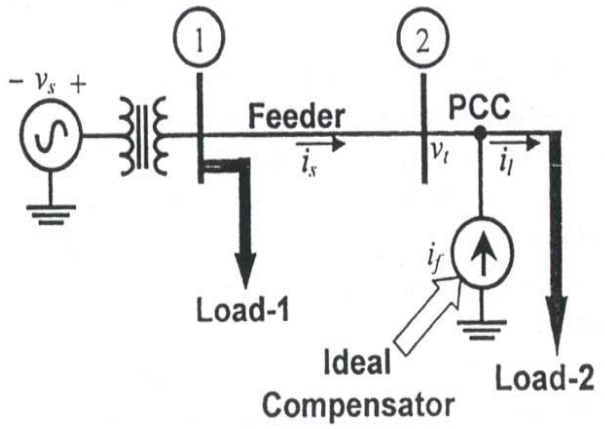


Figure 2: DSTATCOM as load compensator

To alleviate this problem, the compensator must inject current such that the current i_S becomes fundamental and positive sequence. In addition, the compensator can also force the current i_S to be in phase with the Bus –2 voltage. This fashion of operating the DSTATCOM is also called load compensation since in this connection the DSTATCOM is compensating the load current. From the utility point of view, it will look as if the compensated load is drawing a unity power factor, fundamental and strictly positive sequence current. The point at which the compensator is connected is called the utility customer point of common coupling(PCC)

Denoting the load current by I_l the KCL at the PCC yields

$$i_S=i_l-i_f$$

The desired performance from the compensator is that it generates a current i_f such that it cancels the reactive component, harmonic component and unbalance of the load current.

Neutral Clamped Three Phase Voltage Source Inverter

Neutral clamped topology is used in this project because it allows the injection of three independent currents including any dc current that the load may draw. This topology contains two dc storage capacitors as shown in figure 3.In this circuit the junction (n') of the two capacitors is connected to the neutral of the load. This neutral clamped topology allows a path for the zero sequence current and therefore the three injected currents can be independently controlled. Note that in this configuration there is no transformer and each leg of the VSI is connected to the point of common coupling through an interface reactor.

The inductance L_f and the resistance R_f in fig3 represent the interface reactor. Another important component of the topology of fig.3.is chopper circuit that is

represented by the switches S_{ch1} and S_{ch2}, the inductance L_p, resistance R_p.The purpose of this circuit is to balance the voltages in the two capacitors.

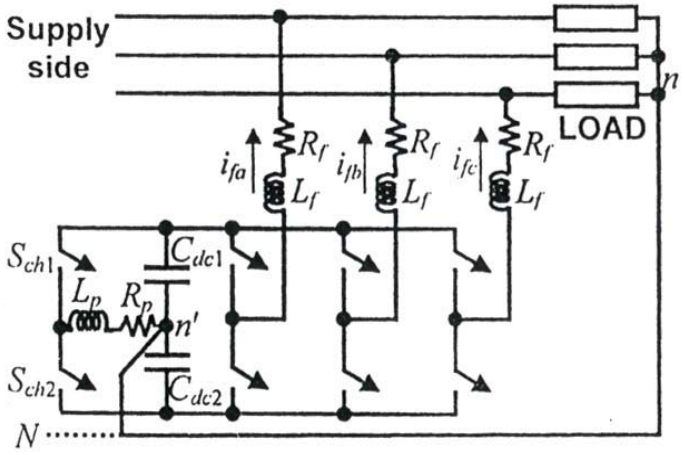


Figure 3: Neutral clamped three phase voltage source inverter

Let us define the voltages across C_{dc1} and C_{dc2} by V_{dc1} and V_{dc2} respectively. Normally the switches S_{ch1} and S_{ch2} are kept open and the V_{dc1} and V_{dc2} are equal. Now suppose the voltage V_{dc1} drops and V_{dc2} rises. The switch S_{ch2} is then closed such that a current is built up in the inductor L_p, once the current reaches a certain level the switch S_{ch1} is opened. The inductor current then discharges through the diode D_{ch1} to bring up the voltage V_{dc1} to the desired level. Similarly, the charge can be transferred from the capacitor C_{dc1} to the capacitor C_{dc2} by closing the switch S_{ch1} to build current in L_p and then charging C_{dc2} through the diode D_{ch2} by opening the switch S_{sh1}. The feedback control of this chopper circuit is essential for the success of the scheme.

Computation of Reference Current

It is assumed that source voltages are balanced and are given by

$$v_{sa} = \sin \omega t$$

$$v_{sb} = \sin(\omega t - 120^{o})$$

$$v = \sin(wt + {}^{o})$$

The objective of compensation is to provide balanced supply current such that its zero sequence component is zero. We therefore have,

$$I_{sa} + i_{sb} + i_{sc} = 0$$

When the power factor angle is assumed to be zero, implies that the instantaneous reactive power supplied by the source is zero. On the other hand, when this angle is non-zero, the source supplies a reactive power that is equal to times the instantaneous power.

The instantaneous power in a balanced three-phase circuit is constant while for an unbalanced circuit it has a double frequency component in addition to a dc value. In addition, the presence of harmonics adds to the oscillating component of the instantaneous power.The objective of the compensator is to supply the oscillating component such that the source supplies the average value of the load power. Therefore,

$$v_{sa}\, i_{sa} + v_{sb}\, i_{sb} + v_{sc}\, i_{sc} = p_{lav}$$

Reference compensator currents are calculated using instantaneous symmetrical component theory.

Modeling of Shunt Active Filter

The equivalent circuit of the compensated system given in fig3. We define three loops with loop currents if_a, if_b and if_c,

$$dif_a/dt = (-R_f/L_f)\, if_a - (v_{sa}/L_f) + \{S_1\, vc_1/L_f - S_4\, vc_2/L_f\}$$
$$dif_b/dt = (-R_f/L_f)\, if_b - (v_{sb}/L_f) + \{S_3\, vc_1/L_f - S_6\, vc_2/L_f\}$$
$$dif_c/dt = (-R_f/L_f)\, if_c - (v_{sc}/L_f) + \{S_5\, vc_1/L_f - S_2\, vc_2/L_f\}$$
$$C\, dvc_1/dt = -(S_1 if_a + S_3\, if_b + S_5 if_c)$$
$$C\, dvc_2/dt = (S_4 if_a + S_6\, if_b + S_2 if_c)$$

Then defining a state vector of the state space equation is given as

$$d/dt\begin{bmatrix} ifa \\ ifb \\ ifc \\ vc_1 \\ vc_2 \end{bmatrix} = \begin{pmatrix} \frac{-R_f}{L_f} & 0 & 0 & \frac{Sa}{L_f} & -\frac{\dot{S}a}{L_f} \\ 0 & \frac{-R_f}{L_f} & 0 & \frac{S_b}{L_f} & -\frac{\dot{S}_b}{L_f} \\ 0 & 0 & \frac{-R_f}{L_f} & \frac{S_c}{L_f} & -\frac{\dot{S}_c}{L_f} \\ -\frac{S_a}{C} & -\frac{S_b}{C} & -\frac{S_c}{C} & 0 & 0 \\ \frac{\dot{S}_a}{C} & \frac{\dot{S}_b}{C} & \frac{\dot{S}_c}{C} & 0 & 0 \end{pmatrix} \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \\ vc_1 \\ vc_2 \end{bmatrix} + \begin{pmatrix} -\frac{1}{L_f} & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & -\frac{1}{L_f} \end{pmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}$$

Switching Control of VSI

If a dynamic offset level is added to both limits of the Hysteresis-band, it is possible to control the capacitor voltage difference and to keep it within an acceptable tolerance margin. Normally 10% of the load current is taken as Hysteresis-band width.

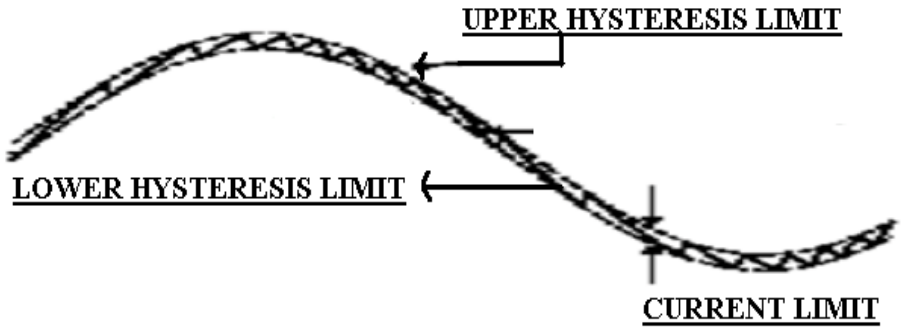


Figure 4: Hysteresis-band width control.

For Phase a:

If $i_{fa} < (i_{fa}^* - hb)$ then upper switch is OFF & lower switch is ON.
If $i_{fa} > (i_{fa}^* + hb)$ then upper switch is ON & lower switch is OFF.

For Phase b:

If $i_{fb} < (i_{fb}^* - hb)$ then upper switch is OFF & lower switch is ON
If $i_{fb} > (i_{fb}^* + hb)$ then upper switch is ON & lower switch is OFF

For Phase c:

If $i_{fa} < (i_{fa}^* - hb)$ then upper switch is OFF & lower switch is ON
If $i_{fa} > (i_{fa}^* + hb)$ then upper switch is ON & lower switch is OFF

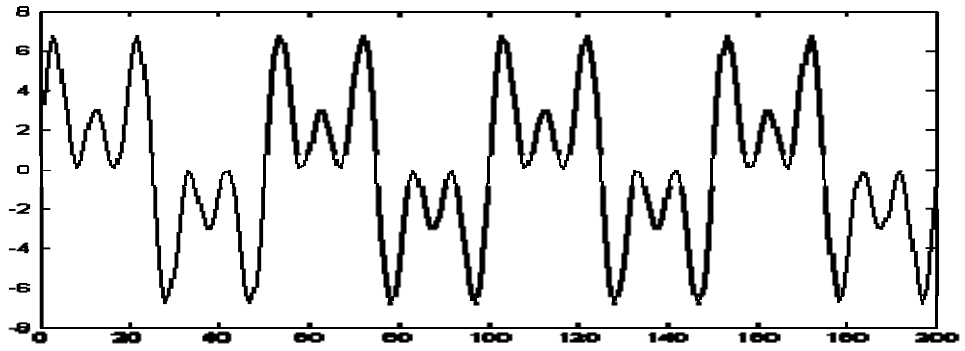
Where 'hb' is the width of the hysteresis band around the reference current

PWM Generation

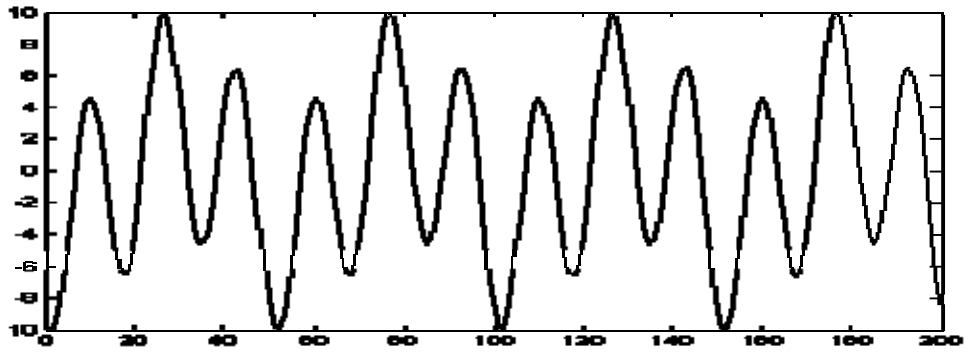
By writing suitable program in DSP, we get the corresponding PWM pulses with respect to the fuzzy logic controller output. From the pulses, we can trigger the inverter circuits, and the current is injected to the source. According to the PWM pulses from the DSP processor, the inverter circuit produces the current to be injected to the source. This injected current just opposes the input supply harmonic current flows from source to load, that is, the amount of current injection is equal to the harmonic current exists on the power system. From that way, we can eliminate the harmonics on the power system and also make the current as pure sinusoidal.

Results

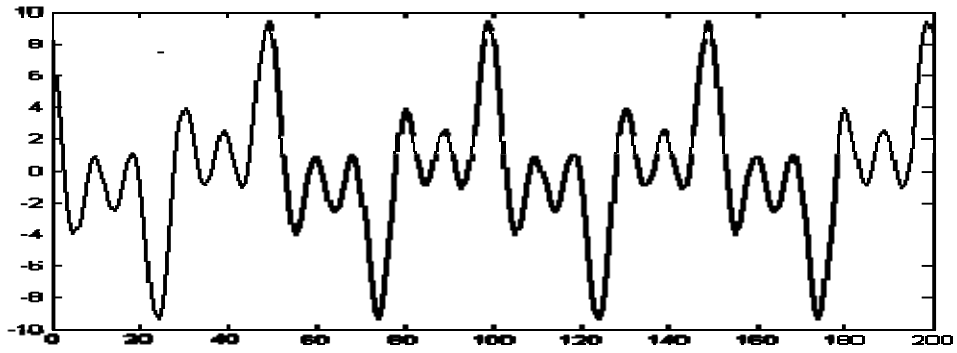
The Source current in phase-a, b, and c before compensation is shown in Fig.-5. The Source current in phase-a, b, and c after compensation is shown in figure-6. From the results presented here it is clearly known that the UPQC is working efficiently in achieving the Source current compensation.



Source current in phase ‘a’ before compensation

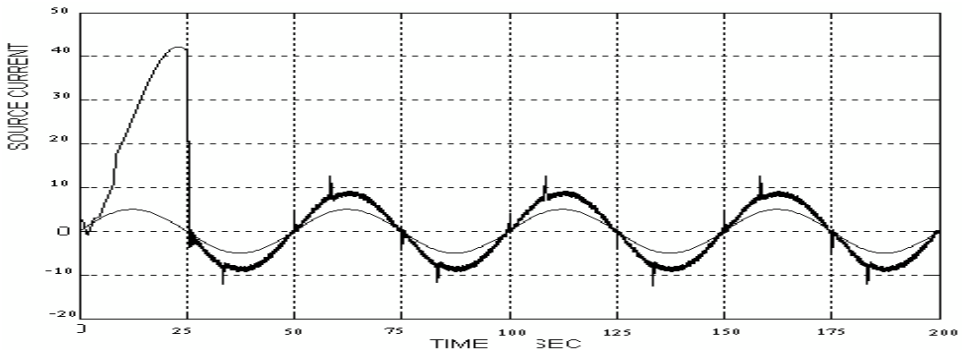


Source current in phase ‘b’ before compensation

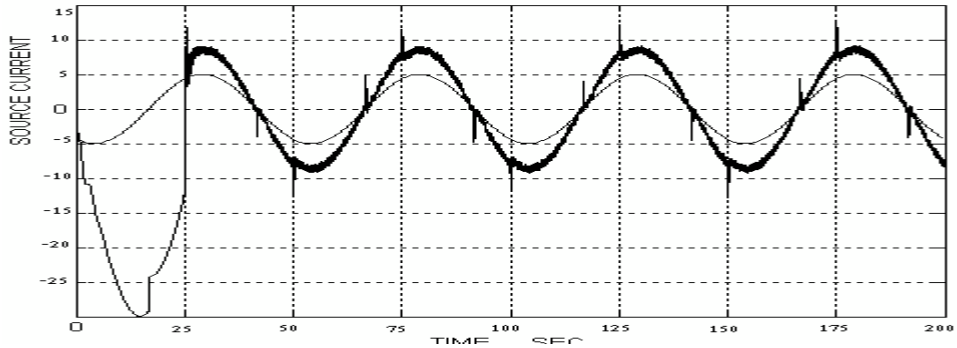


Source current in phase ‘c’ before compensation

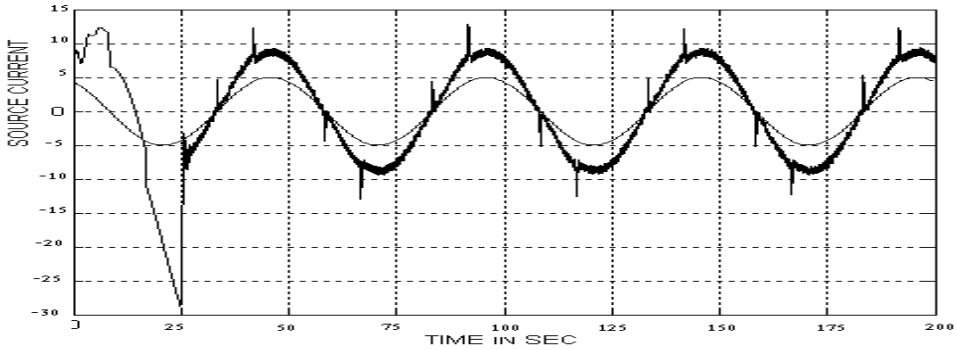
Figure 5: Source currents before compensation



Source current in phase ‘a’ after compensation



Source current in phase ‘b’ after compensation



Source current in phase ‘c’after compensation

Figure 6: Source currents after compensation

Schematic Diagram of the DVR with Capacitor Filter

In this, three H-bridge inverters that are connected through a common dc storage capacitor realize the DVR. The voltage across this capacitor is denoted by V_{dc}. The outputs of the inverters are connected to three single-phase transformers that are connected in series with the three phases of the distribution feeder. The DVR injects

the voltage in the phases a, b and c respectively of the feeder. An ac filter capacitor C_k is also connected across each of the secondary windings of the three transformers to bypass the harmonics generated by inverter switching.

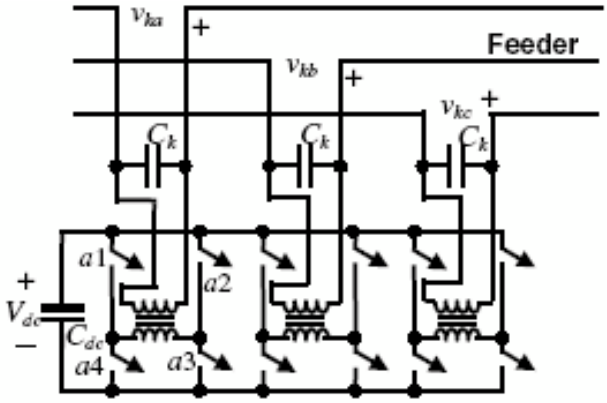


Figure 7: The schematic diagram of the DVR

Computation of Reference Voltage

The source is connected to the DVR by a feeder with an impedance of R+jX. Using KVL at PCC we get

$$v_t + v_f = v_l$$

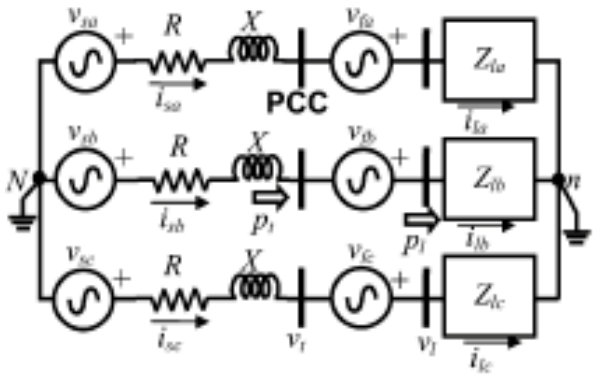


Figure 8: Schematic diagram of a series- compensated distribution system.

The main aim of the DVR is to make the load voltage a strictly positive sequence. Furthermore, the DVR must not supply or absorb any real power. To force v_l to be positive sequence v_f must cancel the zero-and negative-sequence components of v_t. Here the DVR must operate in zero power mode,

$$p_{lav} = p_{tav} = v_{ta}i_{sa} + v_{tb}i_{sb} + v_{tc}i_{sc}$$

Therefore,

$$v_{fo}^* = -v_{to}\ ,\ v_{f1}^* = \lceil v_l \lceil \setminus -v_{t1},\ v_{f2}^* = -v_{t2}$$

An inverse symmetrical component transformation of above equation produces the reference phasor voltages of the DVR. The instantaneous phase voltages then can be obtained from the phasor voltages.

Modeling of Series Active Filter

The basic purpose of the DVR is to inject a set of three phase voltages such that the voltage v_l at the critical load terminal is balanced with a pre- specified magnitude and phase angle. Let this voltage be denoted by v_l then applying KVL, the DVR reference voltage v_k is given by

$$v_k = v_l - v_t$$

Once the reference voltage is generated it is tracked in a Hysteresis band state feedback control Consider the DVR single-phase equivalent circuit shown in Fig 9. In this figure the inverter output voltage is represented by the dc voltage (v_{dc}) times the switching function u(= ± 1).Also the transformer leakage inductance is denoted by L_d and R_d represents the switching losses.

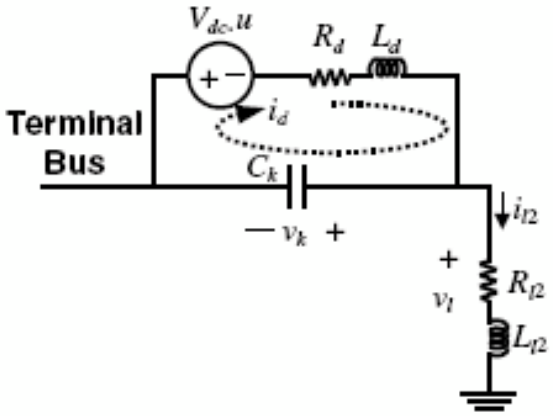


Figure 9: DVR single-phase equivalent circuit

Defining the system state vector as $x^T = [v_k \quad i_d]$ the state space equation of the system is

$$\dot{x} = Ax + Bu_c + Di_{l2}$$

Where u_C is the continuous-time equivalent of *u* and

$$A = \begin{bmatrix} 0 & 1/C_k \\ -1/L_d & -R_d/L_d \end{bmatrix},\quad B = \begin{bmatrix} 0 \\ -V_{dc}/L_d \end{bmatrix},\quad D = \begin{bmatrix} -1/C_k \\ 0 \end{bmatrix}$$

In the state feedback control, u_C is given by

$$u_c = -K(x - x_{ref})$$

Where k is the feedback gain matrix and x_{ref} contains the references of the state vector. The inverter switching logic is then

If u_C >h, then u=+1,

If u_C <h, then u=-1,

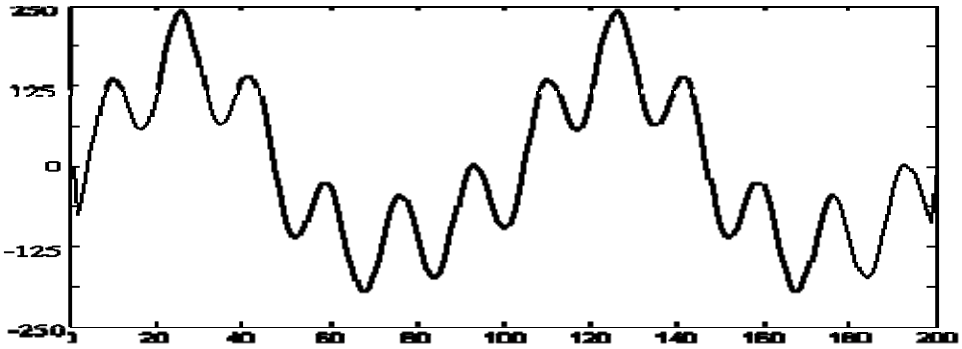
Where h is a small positive constant that defines the Hysteresis band. For example, consider the DVR circuit of Fig. For phase-a, the switching action is given by

If u=1then turn on the pair, a1-a3

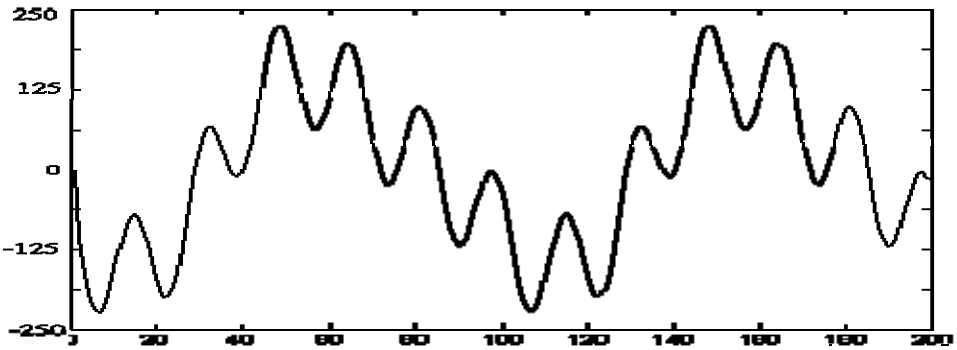
Else if u=-1 1then turn on the pair, a2-a4

Where the switches of one leg are complementary. Similar switching action is also employed for the other two phases.

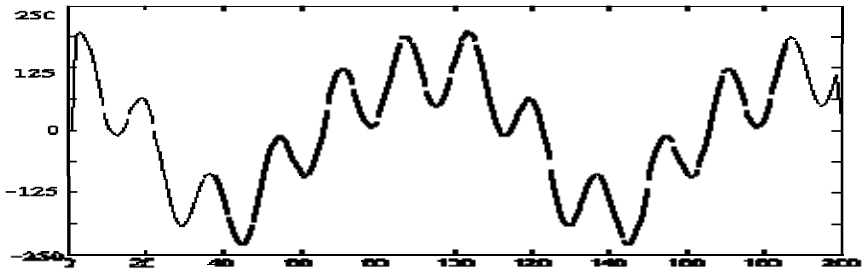
Results



Load voltage in phase ‘a’ before compensation

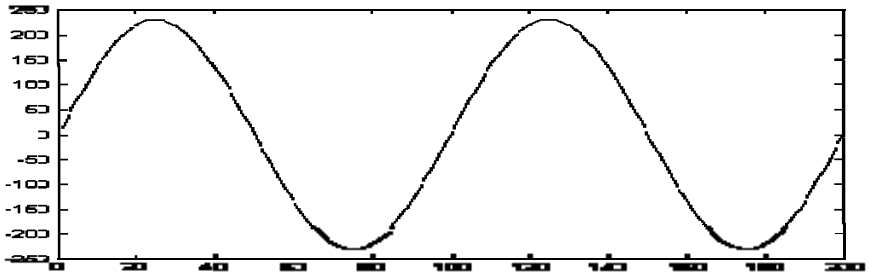


Load voltage in phase ‘b’ before compensation

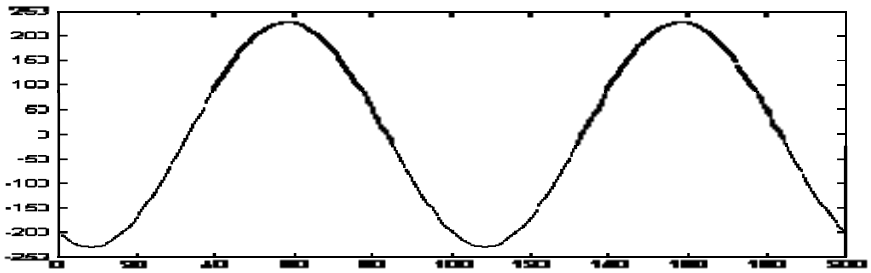


Load voltage in phase ‘c’ before compensation

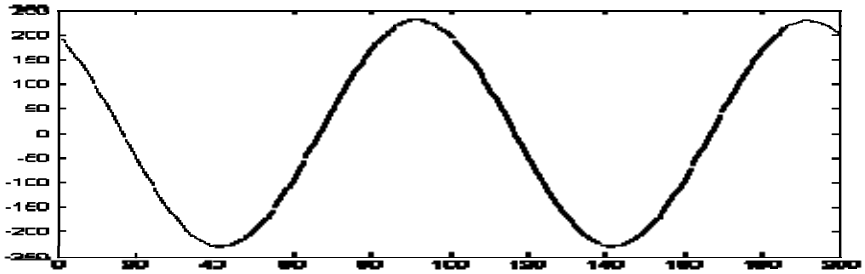
Figure 10: Load voltages before compensation



Load voltage in phase ‘a’ after compensation



Load voltage in phase ‘b’ after compensation



Load voltage in phase ‘c’ after compensation

Figure 11: Load voltages after compensation

The Load voltage in phase-a, b, and c before compensation is shown in fig-10. The Load voltage in phase-a, b, and c after compensation using DVR is shown in fig-11. From the results presented here it is clearly known that the UPQC is working efficiently in achieving the Load voltage compensation.

Conclusion

An operating principle of a unified power quality conditioner (UPQC) is discussed in this paper. The UPQC is connected to a bus that has critical as well as unbalanced and harmonic polluting loads. It has been shown that, the UPQC can tightly regulate the voltage of the critical load and, at the same time, correct the bus voltage from harmonics and unbalance. Extensive simulation results are given to illustrate the operating principle of the UPQC.

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