International Journal of Electrical Engineering.
ISSN 0974-2158 Volume 5, Number 1 (2012), pp. 49-60

http://www.irphouse.com

Performance Evaluation of a Cascaded Multilevel Inverter with a Single DC Source using ISCPWM

[1]M. Balachandran, [2]P. Senthilkumar, and [3]N.P. Subramaniam

[1, 2] Research Scholar, PRIST University, Thanjavur, India.
[3]Assit. Prof, Department of EEE,
Pondicherry Engineering College, Puducherry, India.
E-mail: [1]balachandran_pm@yahoo.com

Abstract

Multilevel inverter (MLI) has been accepted to be very popular particularly in high power applications. The different topologies of MLI are flying capacitor, diode-clamped, and cascaded H-bridge inverter [1].This paper proposes on cascaded MLI using only a single battery and capacitor as the dc sources in order to generate a fifteen-level output. In this effort the scheme is proposed that allows the use of a single battery as the first dc source with the remaining n-1 dc sources being capacitors. The anticipated topology reduces the number of dc sources and switching elements. Different modulation techniques can be used for the MLI [2], but this paper highlighting on a unipolar Inverted Sine Carrier Pulse-Width Modulation (ISCPWM) method reduces the number of carriers with reduction in switching losses and, Total Harmonic Distortion (THD). The performance evaluation of the proposed PWM method for three-phase multilevel inverter is done using MATLAB/SIMULINK and switching loss is determined and minimized total harmonic distortion.

Keywords: ISCPWM, Multilevel inverter, Switching loss & THD.

Introduction

A most important issue with multilevel inverter is eliminating the harmonics from the output voltage. Multilevel inverter approach is a practical solution for reducing harmonics. Different topologies have been reported in the literatures. The cascaded multilevel inverter with separate dc sources can robust many of the needs of all electric vehicles because it can use on panel batteries to generate a nearly sinusoidal voltage waveform to drive the main vehicle traction motor. Normally, each phase of a

cascaded multilevel inverter requires "n" dc sources for 2n+1 level. For many applications, multiple dc sources are required demanding long cables and this could lead to voltage unbalance among the dc sources. To reduce the number of dc sources required for the cascaded multilevel inverter for distributed power generation, this paper focuses on a hybrid cascade MLI(HCMLI) that uses only one dc source while the other dc source is replaced by a capacitor to generate seven level equal step multilevel output [3]. This structure is favorable for high power applications since it provides higher voltage at higher modulation frequencies with a low switching (carrier) frequency. It means low switching loss for the same total harmonic distortion (THD). It also improves the reliability by reducing the number of dc sources.

Performance of the multilevel inverter (such as switching loss and THD) is mainly decided by the modulation strategies. For the cascaded multilevel inverter there are several well known sinusoidal pulse width modulation strategies [4].Compared to the conventional triangular carrier based PWM, the inverted sine carrier PWM has a better spectral quality and a higher fundamental output voltage without any pulse dropping.

Hybrid H-Bridge Multilevel Inverter

The topology of the proposed hybrid multilevel inverter is shown in Fig. 1. The proposed hybrid cascaded multilevel inverter includes a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. It can use only a single DC power source to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors. Traditionally, each H-bridge requires a DC power source [5-7]. Inverted sine carrier PWM (ISCPWM) technique is used to produce a fifteen level phase voltage.

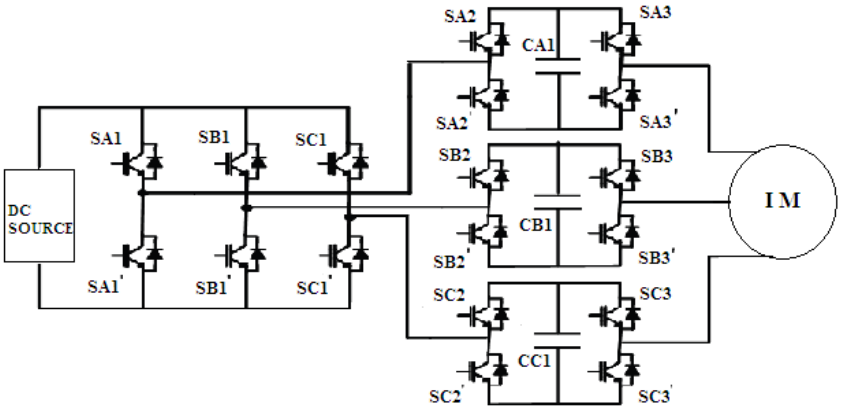


Figure 1: Topology of a three-phase cascaded H-bridge inverter

The topology presented in this paper employs a single dc source per phase to generate an equal step seven level output. The proposed inverter consists of two H-

bridges per phase as shown in Fig.2. The main H - bridge (H_1) is connected to a dc source of value V_{dc} and the second bridge (H_2) is connected to a capacitor whose value is maintained at $0.5V_{dc}$. By appropriately opening and closing the switches of H1, the output voltage v_1 can be made equal to $-V_{dc}$, 0, or $+V_{dc}$ similarly the output voltage of H2 can be made equal to $–0.5V_{dc}$, 0, or $0.5V_{dc}$ and the cascaded output is shown in Fig.3. Therefore, the output voltage of the converter can have seven possible values $1.5V_{dc}$, V_{dc}, $0.5V_{dc}$, 0, $-0.5V_{dc}$, $-V_{dc}$ and $-1.5V_{dc}$.

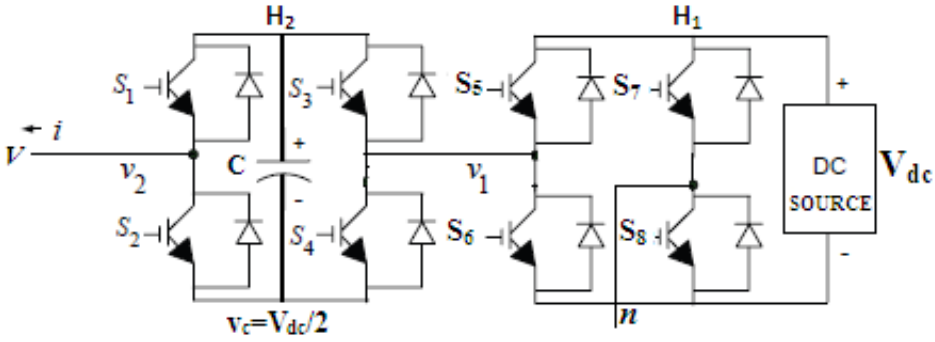


Figure 2: Topology of a hybrid multilevel inverter for one leg

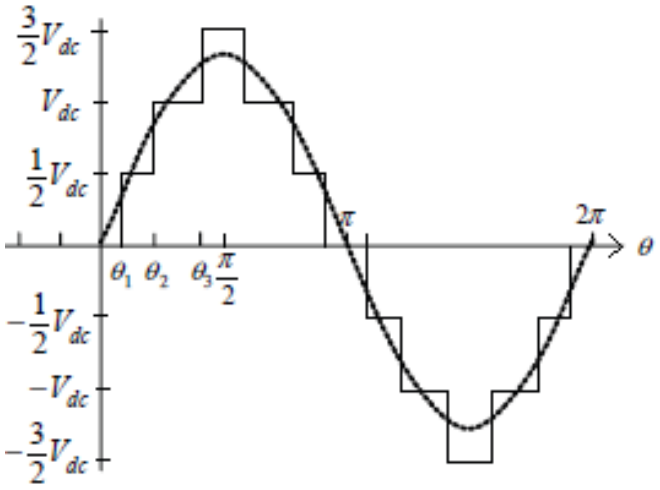


Figure 3: Output voltage waveform of seven level inverter

The DC source for the first H-bridge (H_1) is a dc source with an output voltage of V_{dc}, while the dc source for the second H-bridge (H_2) is a capacitor voltage to be held at $V_{dc}/2$. The output voltage of the first H-bridge is denote by v_1 and the output of the second H-bridge is denote by v_2 so that the output of this two dc sources cascaded H-bridge multilevel inverter is $v = v_1+v_2$. By opening and closing the switches of H_1

suitably, the output voltage v_1 can be made equal to V_{dc}, 0, or else $-V_{dc}$ when the output voltage of H_2 can be made equal to $V_{dc}/2$, 0, or else $-V_{dc}/2$ by opening and closing its switches suitably. Therefore, the output voltage of the inverter may have the values $3V_{dc}/2$, V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$, $-3V_{dc}/2$, which are seven levels. Table I shows a waveform can be generated using the topology of Fig.2 By selecting the nominal value of the capacitor voltage to be one half that of the dc source, the nominal values of the levels are equally spaced. On the other hand, this is not required. The criterion necessary for this capacitor regulating scheme is that (a) the desired capacitor voltage is less than the dc source voltage, (b) the capacitor value is selected large enough so that the variation of its voltage just about its nominal value is small, and (c) the capacitor charging cycle is greater than the capacitor discharge cycle.

Table I: Output Voltages For Seven Level Hybrid Inverter

Angle θ	v_1	v_2	$v = v_1 + v_2$
$0 \le \theta \le \theta_1$	0	0	0
$\theta_1 \le \theta \le \theta_2$	0	$V_{dc}/2$	$V_{dc}/2$
	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$
$\theta_2 \le \theta \le \theta_3$	V_{dc}	0	V_{dc}
$\theta_3 \le \theta \le \pi/2$	V_{dc}	$V_{dc}/2$	$3V_{dc}/2$

The anticipated unipolar control strategy replaces the triangular based carrier waveform by inverted sine wave. The inverted sine pulse width modulation has a enhanced spectral quality and a higher fundamental voltage compared to the triangular based PWM. The application of unipolar PWM to inverted sine carrier results in the reduction of carrier frequencies or its multiples and considerable reduction in switching losses. The advantage of inverted sine and unipolar PWM are combined to get better the performance of the hybrid multilevel inverter. The inverted sine carrier PWM (Inverted SCPWM) technique uses the sine wave as reference signal at the same time as the carrier signal is an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. The pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.

Switching Angles of Switches

Table II shows a waveform can be generated using the topology of Fig. 2. The switching angles of the waveform will be adjusted to get the lowest output voltage THD. If the nominal capacitor voltage is selected as $V_{dc}/2$, then one can calculate the switching angles θ_1, θ_2, and θ_3. The Fourier series expansion of the (staircase) output voltage waveform of the multilevel inverter as shown in Fig. 2 is

$$v(\omega t) = 2\frac{V_{dc}}{\pi} \times \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{\mathrm{n}}(\cos(\mathrm{n}\theta_1) + \cos(\mathrm{n}\theta_2) + \cos(n\theta_3))\sin(\mathrm{n}\omega\mathrm{t}) \ldots\ldots \quad (1)$$

Table II: Switching States Of Seven Level Hybrid Multi level inverter.

Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$3V_{dc}/2$	off	on	on	on	off	on	on	off
V_{dc}	off	on	on	on	off	on	on	on
$V_{dc}/2$	off	on	on	on	off	on	off	on
$0V_{dc}$	off	off	off	off	off	off	off	off
$-V_{dc}/2$	on	on	off	on	off	on	off	on
$-V_{dc}$	on	on	off	on	on	on	off	on
$-3V_{dc}/2$	on	on	off	on	on	off	off	on

The given preferred fundamental voltage v_1, one wants to decide the switching angles θ_1, θ_2, and θ_3 so that eq.(1) becomes $v(\omega t) = v_1\sin(\omega t)$. For three-phase systems, the triplen harmonics in each phase no need to be canceled as they automatically terminate in the line-to-line voltages. In this where there are three dc sources (one battery and two capacitor sources), the need is to cancel the 5th and 7th order harmonics as they tend to dominate the total harmonic distortion. The mathematical statements of these conditions are

$$2\frac{V_{dc}}{\pi}(\cos(\mathrm{n}\theta_1) + \cos(\mathrm{n}\theta_2) + \cos(n\theta_3)) = \mathrm{v}_1 \ldots\ldots (2)$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \ldots\ldots (3)$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \ldots\ldots (4)$$

This is a method of three transcendental equations in the three unknown θ_1, θ_2, and θ_3.

Fifteen Level H-Bridge Inverter

Fig. 4. Shows the topology of a fifteen level H-Bridge cascaded multilevel inverter with three H-bridges. The output waveform is shown in Fig. 5. The dc source for the first H-bridge (H_1) is a dc source with an output voltage of V_{dc}, the dc source for the second H-bridge (H_2) is a capacitor voltage to be held at $V_{dc}/2$, and the dc source for the third H-bridge (H_3) is a second capacitor voltage held at $V_{dc}/4$. As in the seven level H-Bridge inverter, the capacitor voltages are selected in this way so that the difference between levels is the same. The output voltages of each of the H-bridges are denote v_1, v_2, and v_3 respectively, so the output voltage of the fifteen level inverter

is given by $v = v_1 + v_2 + v_3$. Table III shows a waveform can be generated using the topology of Fig.4

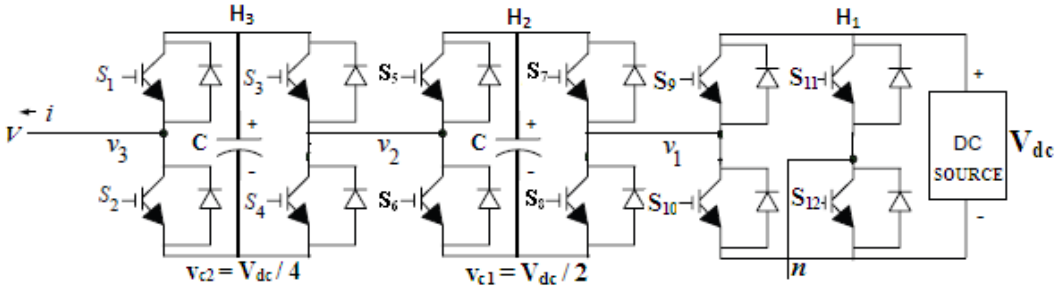


Figure 4: Topology of a fifteen level H-Bridge cascaded multilevel inverter for one leg

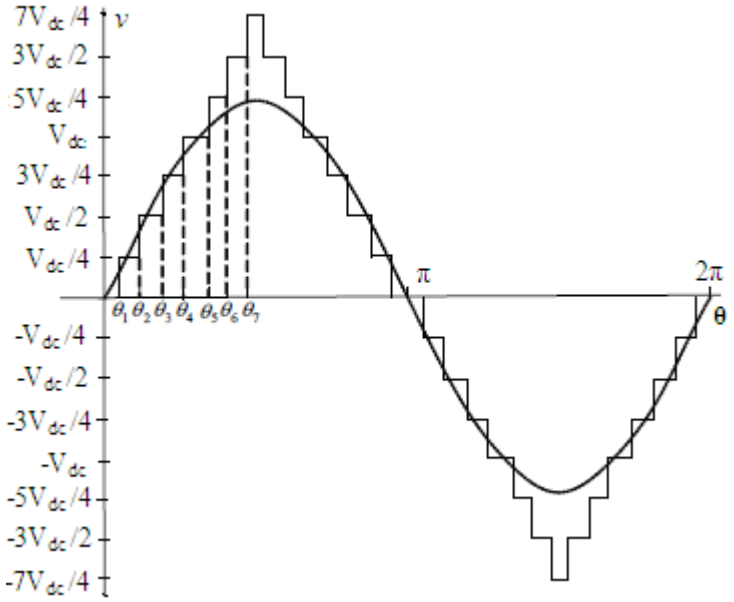


Figure 5: Output voltage waveform of fifteen level inverter

Table III: Output Voltages For Fifteen Level Hybrid Inverter

Angle θ	v_1	v_2	v_3	$v = v_1+v_3$
$0 \le \theta \le \theta_1$	0	0	0	0
$\theta_1 \le \theta \le \theta_2$	0	0	$V_{dc}/4$	$V_{dc}/4$
	0	$V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/4$
	V_{dc}	$-V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/4$
$\theta_2 \le \theta \le \theta_3$	0	$V_{dc}/2$	0	$V_{dc}/2$
	V_{dc}	$-V_{dc}/2$	0	$V_{dc}/2$

$\theta_3 \leq \theta \leq \theta_4$	0	$V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
	V_{dc}	0	$-V_{dc}/4$	$3V_{dc}/4$
	V_{dc}	$-V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
$\theta_4 \leq \theta \leq \theta_5$	V_{dc}	0	0	V_{dc}
$\theta_5 \leq \theta \leq \theta_6$	V_{dc}	0	$V_{dc}/4$	$5V_{dc}/4$
	V_{dc}	$V_{dc}/2$	$-V_{dc}/4$	$5V_{dc}/4$
$\theta_6 \leq \theta \leq \theta_7$	V_{dc}	$V_{dc}/2$	0	$6V_{dc}/4$
$\theta_7 \leq \theta \leq \pi/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	$7V_{dc}/4$

Harmonics

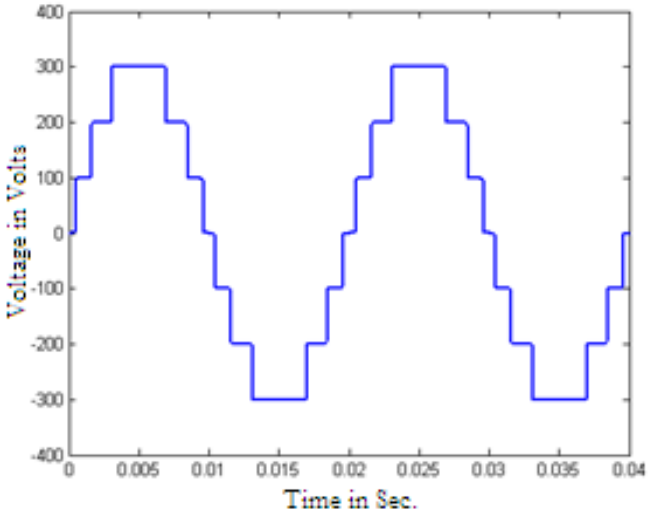
The switching angles of the waveform will be adjusted to obtain the lowest output voltage THD. Harmonics are disagreeable current or voltage [8-9]. They exist at some fraction or multiple of the fundamental frequency. The harmonics causes in three ways are a) the application of a non sinusoidal driving voltage to a circuit containing linear impedance. b) The application of a sinusoidal driving voltage to a circuit containing non linear impedance. c) The application of a non sinusoidal driving voltage to a circuit containing non linear impedance. The harmonics orders and magnitude are depends up on the type of inverter and the control techniques for example in single phase VSI, the output voltage waveform typically consists only of odd harmonics. The even harmonics are not present due to the half wave symmetry of the output voltage harmonics. For three phase VSI, in addition to the even harmonic triplen (third and multiple of third harmonics) are also not present. The harmonic spectra depend on the switching frequency and the control method.

PWM for harmonic reduction

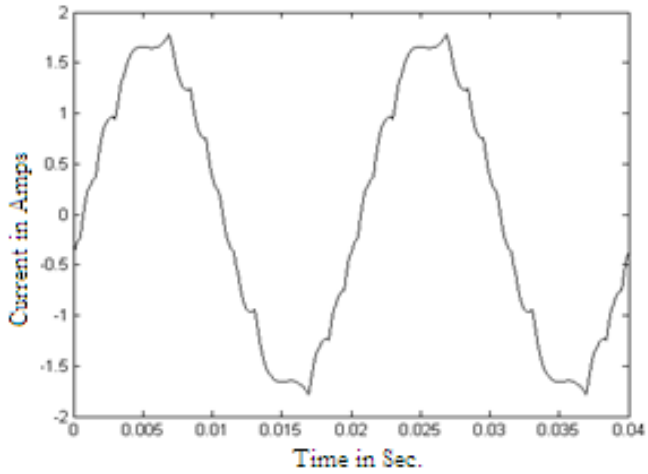
PWM method is broadly used for eliminating destructive low-order harmonics in input and output voltage. In PWM control technique, the inverter switches are turned ON and OFF several times during a half cycle and output voltage is controlled by varying the pulse width. At present, available PWM schemes can be broadly classified as carrier modulated sinusoidal PWM (SPWM) and pre calculated programmed PWM schemes. The inverters of the pulses are varied by changing the amplitude of the sinusoidal wave form. In this process the lower order harmonics are eliminated. As the switching for increases more harmonics can be eliminated.

Simulation Results and Analysis

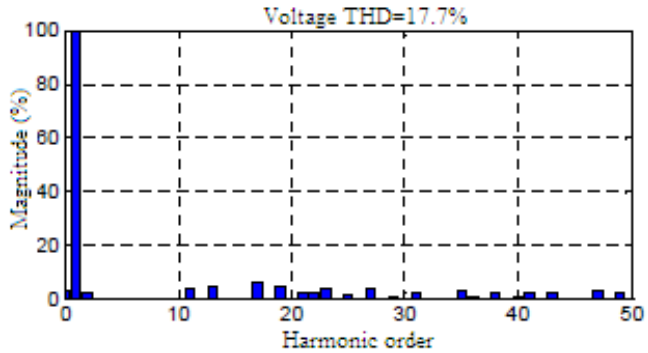
Fig. 6(a) illustrates the phase to phase voltage waveform of a 7 level inverter. Steady state phase to phase voltage is shown in Fig. 7(a) the high number of levels generated by 15 level inverter can be clearly appreciated in the voltage. With increased number of level nearly gets sinusoidal voltage waveform. Fig. 6(b) shows the line current of motor with higher ripples. The instantaneous line current of motor fed by cascade multilevel inverter at min THD is shown in Fig. 7(b).



(a) Phase to Phase Voltage (7 level)

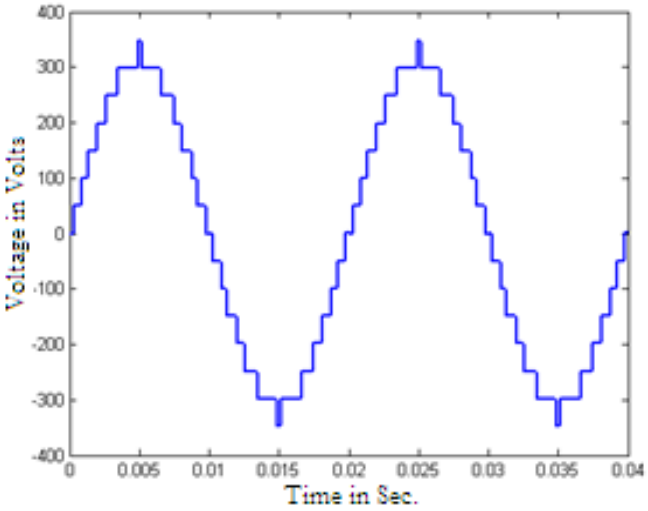


(b) Stator current (7 level)

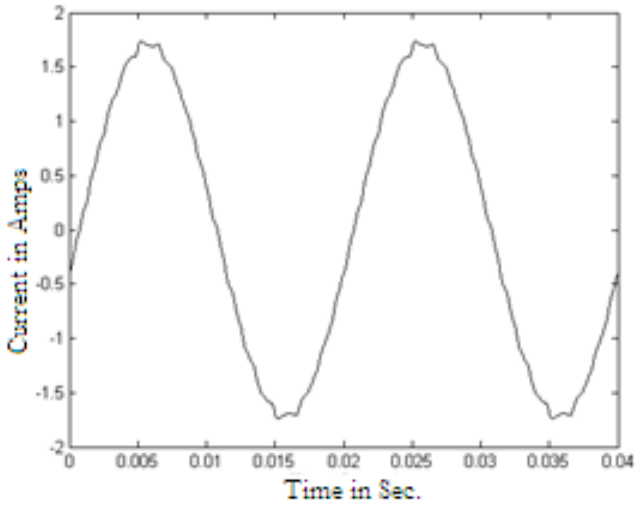


(c) Harmonic spectrum (7 level)

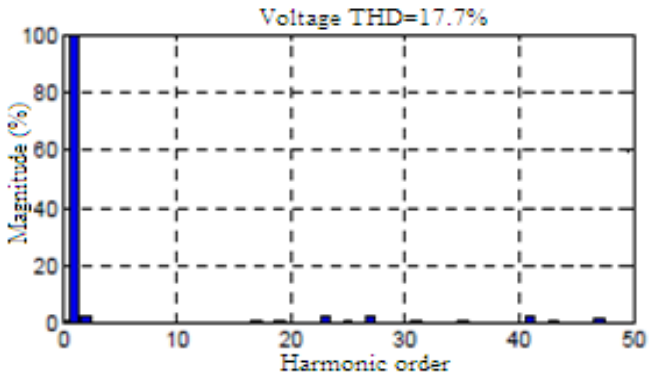
Figure 6: Hybrid multilevel inverter for 7 levels.



(a) Phase to Phase Voltage (15 level)



(b) Stator current (15 level)



(c) Harmonic spectrum (15 level)

Figure 7: Hybrid multilevel inverter for 15 levels.

The ripple of the current decreases with higher number of levels. As a result, the current waveforms become more sinusoidal. Fig. 6(c) and Fig. 7(c) represents the harmonic spectrums for seven level and fifteen level of an inverter at the modulation index 1. In Fig.8 the different THD values obtained for different modulation indexes. It is noted that THD of voltage harmonics of seven level inverter is 17.7% as compared to 6.3% that of fifteen level inverter. Thus power quality has improved largely.

Fig.8 shows the different THD values obtained for different modulation indexes. It is noted that THD of voltage harmonics of seven level inverter is 17.7% as compared to 6.3% that of fifteen level inverter. Thus power quality has improved primarily.

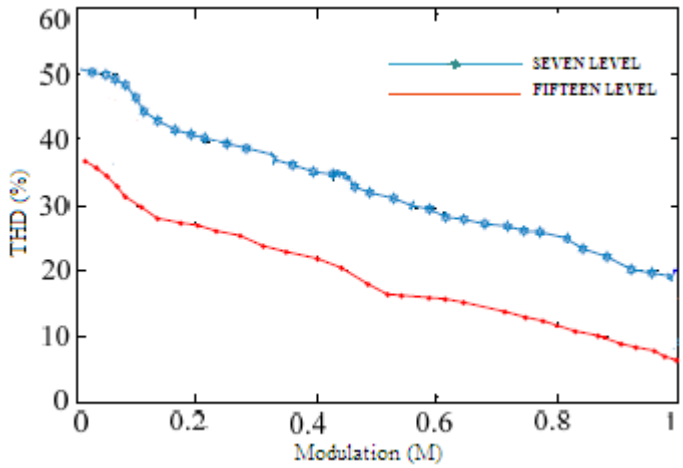


Figure 8: Variation of THD with modulation index

Conclusion

An enhanced cascaded multilevel inverter configuration is proposed. The proposed cascaded inverter design is to get the improved sinusoidal output compare with low level inverters. The asymmetrical multilevel inverter is to achieve a high resolution. The proposed technique to reduce the number of insulated supplies and to get better the efficiency. The cascaded multilevel inverter system is used to get better the level of inverter and reduces the harmonics and extends the design flexibility.

References

[1] Mariusz Malinowski, K.Gopakumar, Jose Rodriguez, and Marcelo.Perez " A survey on cascaded multilevel inverters", Industrial Electronics, IEEE Transactions, Vol. 57, issue:7, pp. 2197-2206, July 2010.

[2] S. Mariethoz and A.C. Rufer. Design and control of asymmetrical multilevel inverters. *IECON'02*, November 2002.

[3] D. Zhong, L.M.Tolbert, J, NChiasson, B.Ozpineci, Li Hui, and A.Q.Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles", in Proc. 37th IEEE Power Electronics Specialists Conference, PESC'06, June 2006, pp.1- 6.

[4] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel converters for large electric drives, " *IEEE Transactions on Industry Applications*, vol. 35, no. 1, Jan./Feb. 1999, pp. 36-44.

[5] M.Balachandran and N.P.Subramaniam, "Multilevel Inverter Based Induction Motor Drive" in proc., of International Conference, ICPCES- 2010 organized by College of Engineering Guindy, Anna University, Chennai, pp. 264-268, Dec. 2010.

[6] J. S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters, " *IEEE Transactions on Industry Applications*, vol. 32, no.3, May. /June 1996, pp. 509-517.

[7] S. Khomfoi, L. M. Tolbert, "Multilevel power converters, " *PowerElectronics Handbook*, 2nd Edition Elsevier, 2007, ISBN 978-0- 12- 088479-7, Chapter 17, pp. 451-482.

[8] J. Liao, K. Corzine, M. Ferdowsi, "A new control method for single-DC-source cascaded H-Bridge multilevel converters using phase-shift modulation, " *IEEE Applied Power Electronics Conference and Exposition*, Feb. 2008, pp.886-890

[9] M. Veenstra and A. Rufer. "Control of a hybrid asymmetric multi- level inverter for competitive medium-voltage industrial drives". *IAS'2003*, 1:190 – 197, October 2003.

[10] A.k.Ali Othman "Elimination of harmonics in multi level inverters with non equal DC sources using PSO".IEEE conf.proce EPE PEMC 2008.

[11] J. Chiasson, L. M. Tolbert, and K. McKenzie, "A new approach to solving the harmonic elimination equations for a multilevel converter, " in *Proc. IEEE Industry Applications Conference*, vol. 1, Oct. 2003, pp. 640-647.

Biographies

M. Balachandran (M'37) was born in Komarapalayam on January 10, 1974. He is graduated in 2000 from Bharathiar University, Coimbatore and post graduated in 2006 at Anna University, Chennai. He is currently pursuing Ph.D in the department of Electrical and Electronics Engineering. He has been working as an Assistant Professor for various engineering colleges, since 2000. He published 6 international/national conferences. His research interest involves in power electronics, inverter, modeling of induction motor and optimization techniques. He is guiding UG, PG students. He is member of ISTE and IEEE.

Senthilkumar P. (M'34) obtained his B.E. degrees in electrical and electronics engineering from Bharathiyar University in 1999 and received M.E. degree in Power System Engineering from Anna University in 2008. He currently is pursuing as a Research Scholar in the field of Power System Engineering.. He specializes in

harmonics, DC systems and power system transients. He has authored papers on power system restoration, harmonics and DC modeling. He is a member of IET, IEEE and life member in ISTE. From 2000 to 2010, he has been working as Lecturer for various engineering colleges around Chennai. He guided many projects for students and revolved around transistorized drives, induction heating inverters and power flow control devices for power systems. Now, he is doing Grid Controller projects where he is currently involved in design and simulation of main circuit of Smart Grid Controllers and its stability studies.

N.P. Subramaniam received the B.E. degree in Electrical and Electronics Engineering from the Bharathiar University in 1997. He also received the M.E. degree in Power System Engineering from Annamalai University in 1999. In 2008 he received Ph.D degree from Anna University Chennai in the field of Electrical Engineering. From 2001 to 2005 he worked as Teaching Research Associate in the Department of Electronics Engineering, MIT Campus Anna University. He worked as a Lecturer in the Department of EEE, CEG, Anna University from 2005 to 2007. He is currently an Assistant Professor of Electrical Engineering in the Pondicherry Engineering College, Puducherry. His research interests include power system, power electronics, signal processing applications to power system and power quality.