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A 90nm CMOS Low Noise Amplifier with Shunt – Series Peaking for Ultra Wide Band Communication Systems

Vaithianathan Venkatesan[1]*, Raja Janakiraman[2] and Srinivasan Raj[3]

[1]Dept. of ECE, SSN College of Engineering,
Chennai, Tamil Nadu, 603110, India,
E-mail: vaithianathanv@ssn.edu.in
[2]Dept. of ECE, Anna University of Technology,
Tiruchirapalli, Tamil Nadu, 620024, India
E-mail: rajajanakiraman@gmail.com
[3]Dept. of IT, SSN College of Engineering,
Chennai, Tamil Nadu, 603110, India
E-mail: srinivasanr@ssn.edu.in

Abstract

An Ultra wideband (UWB) CMOS Low Noise Amplifier (LNA) with shunt series peaking is proposed with a cascode stage as a core amplifier. A common gate (CG) stage is used to achieve a broad band input matching with low power consumption while a buffer is used to obtain the output matching. Shunt – Series peaking technique is used to enhance the bandwidth while current reuse technique is used to increase the gain without increasing the power consumption. The proposed LNA is designed with 90 nm CMOS technology and its performance is analyzed using Agilent's ADS simulator. The simulation results are presented and compared with recently reported LNAs. The proposed LNA achieves a power gain greater than 14.6 dB and noise figure less than 3.5 dB in the 3 to 16 GHz band. The input matching is kept well below –16 dB, while the output matching is below – 11.5 dB and the reverse isolation is below – 56 dB in the entire band. The proposed LNA ensures a better linearity with an IIP_3 of – 3 dBm. The LNA consumes as low as 3.548 mW power while using 1 V supply.

Keywords: Current Reuse, Power Gain, Input Matching, Noise Figure, IIP3, Power Consumption

Introduction

In recent years, the academia and industry put forth their interest in UWB technology because it offers a promising solution to the radio frequency (RF) spectrum drought by allowing new services to coexist with the other radio systems with minimal or no interference. The UWB technology offers several advantages, such as wide bandwidth, large throughput, and robustness to jamming. This technology is suitable for short range and high data rate wireless applications. As per the Federal Communications Commission (FCC) approved First Report and Order (R&O) [1] released in 2002, the UWB signals must have bandwidth of more than 500 MHz or fractional bandwidth larger than 20 percent at all times of transmission with an average power spectral density of –41.3dBm/MHz in the 3.1 – 10.6 GHz band.

UWB systems are classified into Multi Band Orthogonal Frequency Division Multiplexing (MB -OFDM) and Direct Sequence (DS) UWB systems [2]. DS - UWB is a single-band approach that uses narrow UWB pulses to transmit and receive information. As shown in Figure 1, the entire band is divided into lower and upper bands. The lower band occupies the spectrum in the range of 3.1 to 4.85GHz while the upper band falls in the range of 6.2 GHz to 9.7 GHz.

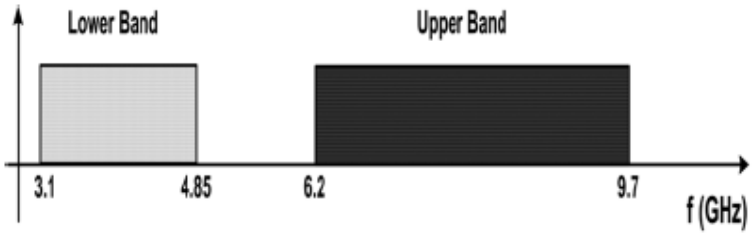

Figure 1: DS UWB

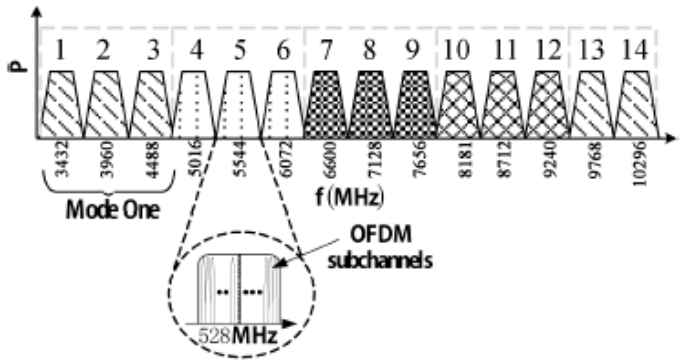

Figure 2: MB-OFDM UWB

On the other hand the MB - OFDM based UWB approach uses the entire 7.5 GHz band by dividing it into 14 bands with a bandwidth of 528 MHz each. These bands are organized into five groups wherein the operation within the first group is mandatory, while all the other groups are optional. This is illustrated in Figure 2.

Problem Statement

Even though several favourable features are available with the UWB systems, serious design challenges still exist in the realization of the UWB receiver front-end circuits, especially in the design of LNA. Since FCC forces stringent power-emission limitations at the transmitter and due to the additional transmission path loss, the received UWB signal exhibits very low Power Spectral Density (PSD) at the receiver antenna, resulting in a received signal power that is typically three orders of magnitude smaller than that of the narrow-band transmission systems. Thus the LNA plays an important role in the receiver designs. The ultimate aim of the LNA is to amplify the weak signal received from the antenna to acceptable levels while trying to cut out the additional self generated noise without introducing any distortions. The LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible power consumption and it should also occupy less area.

In [3], Zhe Yang Huang proposed a cascode UWB LNA with current reuse technique and filter network for input matching. This LNA consumes more power while providing a moderate gain and noise figure. In [4] the current reuse technique is used in cascaded topology. The noise figure is significantly decreased in the entire band but it consumes more power to provide the necessary gain. A conventional CG LNA is used along with an active feedback circuit in [5] in order to achieve a wideband input matching and a very low noise figure. This circuit provides a very good linearity but the power consumption is moderately high and its performance is significantly degraded at the upper UWB band. An improved noise reduction technique is proposed in [6] using an active positive feedback, input matching extender and a transformer. This helps in achieving a reduced noise figure in the entire band. This circuit consumes very low power but the circuit complexity is high and it offers poor linearity.

In this paper, in order to reduce the circuit complexity and power consumption, an UWB CMOS LNA is proposed using an input CG stage instead of filter networks in order to obtain broad band input matching. The output capacitance of the first stage will limit the bandwidth, and it is compensated by an inductor L2. A Cascode stage with a shunt-series peaking as a bandwidth enhancement technique and a current reuse method for reducing power consumption is used as a core amplifier. A buffer is used to obtain output matching with lesser circuit complexity. The overall gain of the amplifier is calculated after considering the loss introduced by this buffer. Section 3 discusses the operation of the proposed circuit. In Section 4, the simulation results with performance analysis are presented. The effect of current reuse is also addressed. The conclusion is presented in Section 5.

Circuit Description

The schematic of the proposed LNA is shown in Figure 3 and its analysis is presented in the subsections.

Input Stage

The equivalent circuit for input stage is shown in Figure 4. The proposed architecture has a CG amplifier as the first stage to provide input matching. In CG amplifier the resistance looking into the source terminal is $1/g_m$. The input impedance of the proposed LNA including the parasitic capacitance is given by the equation (1)

$$Z_{in} \approx \frac{sL_1}{1+(sC_{gs1}+g_{m1})sL_1} \tag{1}$$

The parasitic capacitance present in the equation (1) will make the input matching get worsen at the higher frequencies. So, the best input matching is obtained at the resonant frequency given by the equation (2)

$$\omega_S = \frac{1}{\sqrt{C_{gs1}L_1}} \tag{2}$$

The resonant frequency is fixed at the centre of our band of interest by suitably selecting the values of C_{gs1} and L_1. This ensures better input matching without degrading the noise figure and power gain. Thus, the input matching of 50Ω can be easily achieved by selecting the value of L_1 and the width of M_1 appropriately. The gain achieved by this first stage is given in equation (3).

$$A_{v1} \approx g_{m1}(\frac{1}{sC_{gd1}} \,||R_1||Z_{in2}) \tag{3}$$

where,

$$Z_{in2} \approx s(L_1 + L_2) + \frac{1}{sC_{in2}} + \frac{g_{m2}L_3}{C_{in2}}$$

$$C_{in2} \approx C_{gs2} + (1 + A_{v2})C_{gd2}$$

Cascode Stage

The equivalent circuit for cascode stage is shown in Figure 5. A conventional Cascode Amplifier employing current reuse technique and shut-series peaking is used as the second stage in order to provide a sufficient gain with a wider 3-dB bandwidth. The current reuse [4] topology is constructed by using C_1, L_4 and L_5. The combination of L_5 and C_1 provides a low resistance path, as a consequence of which the input signal can be amplified twice through the two paths available. With this design technique, a high gain can be obtained at low dc power consumption. The inductor L5 is used for cancelling the pole introduced by C1. The dimension of the Cascode transistor M_3 is chosen 10 times smaller than that of common source transistor M_2 to provide very less parasitic capacitance. The shunt-series peaking [7] is used to enhance the bandwidth so that the proposed LNA will provide sufficient gain over the entire band of 3-16GHz.The gain achieved by this second stage is given by the equation (4).

$$A_{v2} = \frac{g_{m2}g_{m3}Z_{L2}Z_{L3}}{1 + g_{m2}(sL_3)} \tag{4}$$

where,

$$Z_{L2} \approx \left(sL_5 + \frac{1}{sC_1}\right)||(sL_4 + \frac{1}{sC_{gs3}} + \frac{1}{g_{m3}})Z_{L3} \approx (sL_6 + R_2)||(sL_7 + \frac{1}{sC_{gs4}} + \frac{1}{g_{m4}})$$

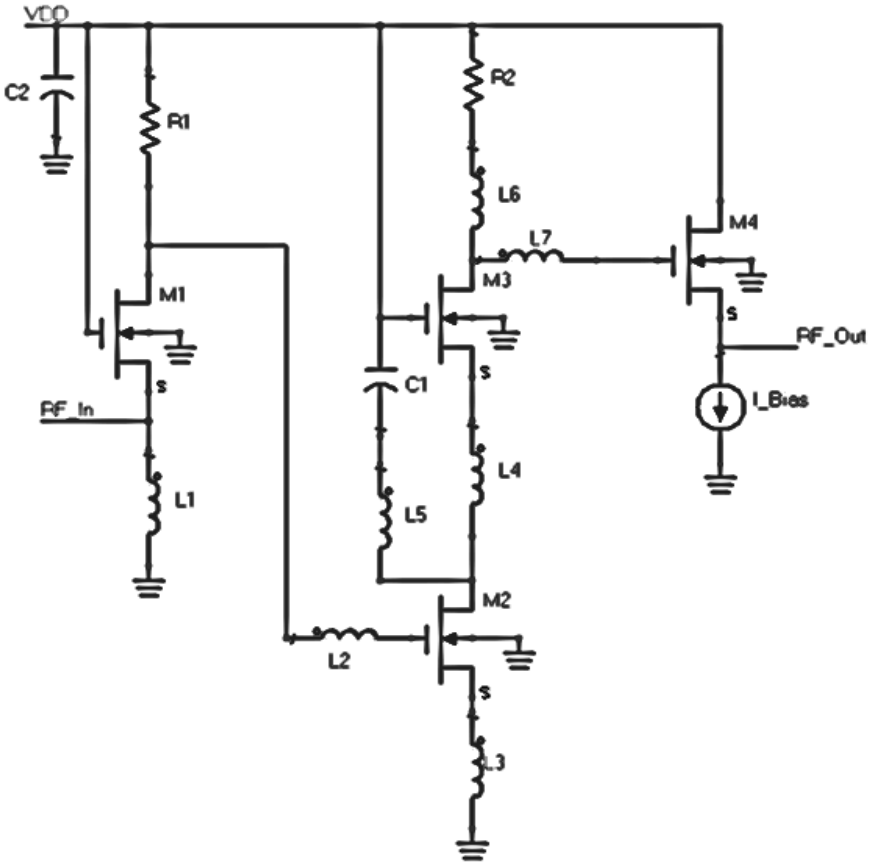

Figure 3: Proposed LNA

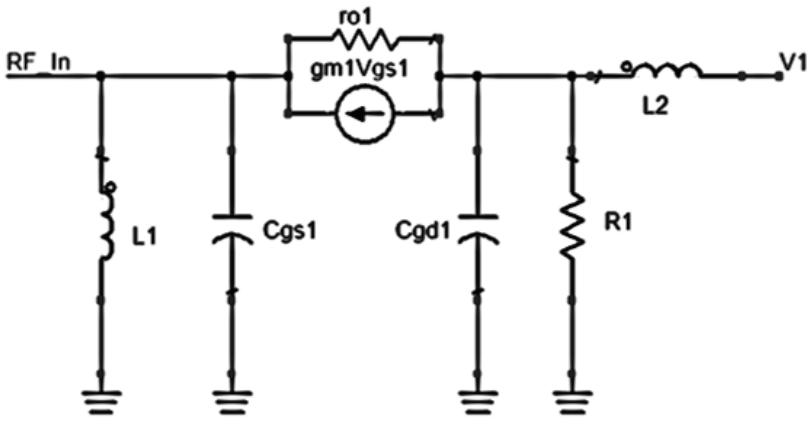

Figure 4: Equivalent Circuit for input stage of the proposed circuit

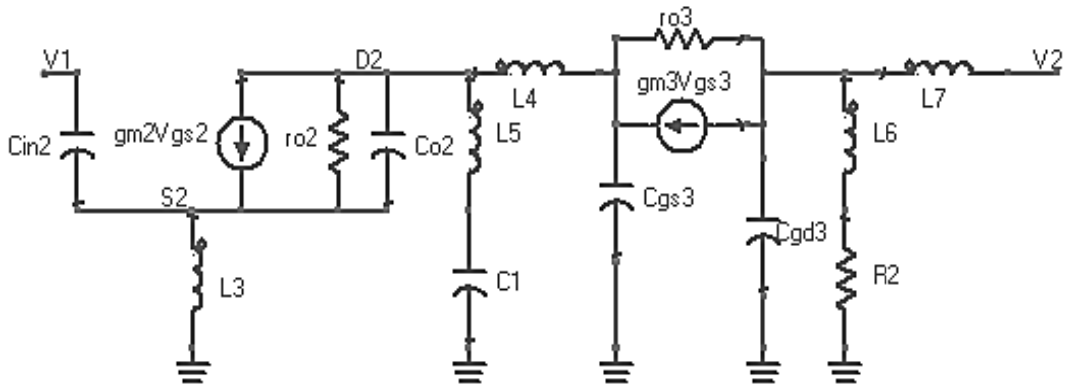

Figure 5: Equivalent circuit for Cascode stage of the proposed circuit

Output Stage

A buffer is added to provide the output impedance matching. The equivalent circuit for output stage is shown in Figure 6. This buffer is simply a source follower (M_4) which has low output impedance thereby enabling easy output matching. The drain resistance of the transistor M_4 serves as the load of the UWB LNA. A current source I_Bias is used at the load in order to improve the linearity of the common drain buffer [8].

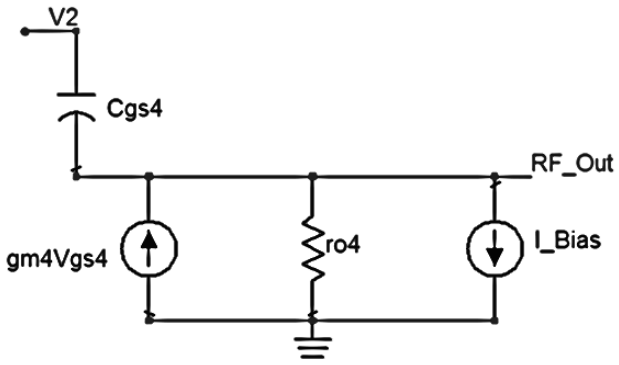

Figure 6: Equivalent circuit for output stage of the proposed circuit

The output impedance of the proposed LNA is given by the equation (5)

$$Z_{out} \approx r_{o4} \tag{5}$$

The gain of the buffer is given by the equation (6)

$$A_{v3} \approx \frac{g_{m4} r_{o4}}{1 + g_{m4} r_{o4}} \tag{6}$$

So, the overall gain of the proposed LNA is given by the equation (7)

$$A_{v,total} = A_{v1} \times A_{v2} \times A_{v3} \tag{7}$$

Simulation Results

The simulation results of the proposed LNA are obtained using Agilent's ADS simulator. A 90nm CMOS technology file is used for the simulation purposes. The results are elaborated in the following sections.

Power Gain (S_{21})

The LNA is required to achieve a high power gain in order to reduce the effect of noise introduced by the subsequent stages at the receiver front end. So, in our circuit by using both current reuse and shunt-series peaking techniques, power gain of higher than 14.6 dB is achieved over the entire bandwidth of 3 to 16 GHz while the peak power gain of 17.6 dB is achieved at the frequency of 8 GHz. This is illustrated in Figure 7.

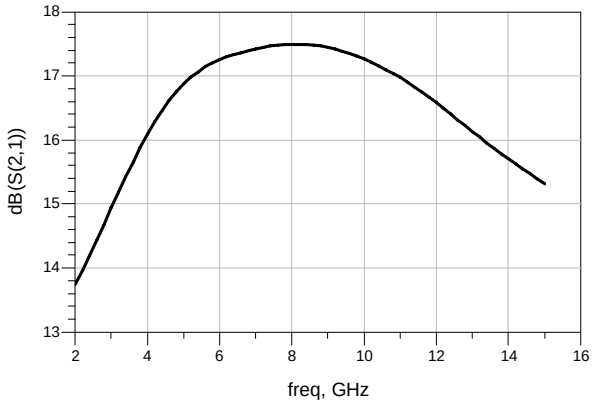

Figure 7: Power gain (S_{21})

Noise Figure (NF)

Noise figure (NF) is a measure of degradation of the signal-to-noise ratio (SNR), caused by components in a Radio Frequency (RF) signal chain. The bulk contact of all the transistors in the proposed circuit is grounded in order to reduce the substrate coupling noise. The simplified equation for noise figure derived from the noise model is given in equation (8).

$$F \approx 1 + \frac{1}{g_{m1}\left(\mathrm{Re}\{Z_S\}\right)} + \frac{2}{3\left(\mathrm{Re}\{Z_S\}\right)} \tag{8}$$

where Z_s is the source impedance. The noise figure of our proposed circuit is kept below 3.5 dB in the entire 3 to 16 GHz bandwidth as shown in Figure 8.

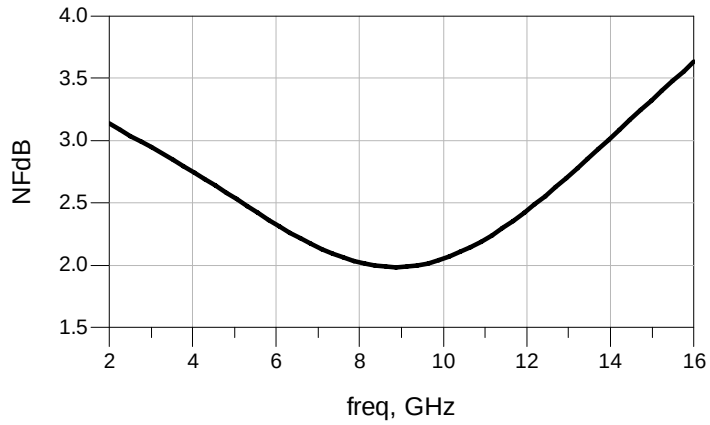

Figure 8: Noise Figure

Input Matching (S_{11})

In general, it is difficult to achieve both noise matching and power matching simultaneously in an LNA design, since the source admittance for minimum noise is usually different from the source admittance for maximum power delivery.A simultaneous noise figure and input matching approach is achieved by using a CG input stage along with an inductor L_1 to transform the source impedance from 50 ohms to the optimum value for minimum noise. Its typical value should be less than –10 dB while maintaining lowest noise figure. In our proposed LNA, a minimum of –23 dB is achieved at 9.5 GHZ while less than –16 dB is maintained throughout the bandwidth of 3 to 16 GHz as presented in Figure 9.

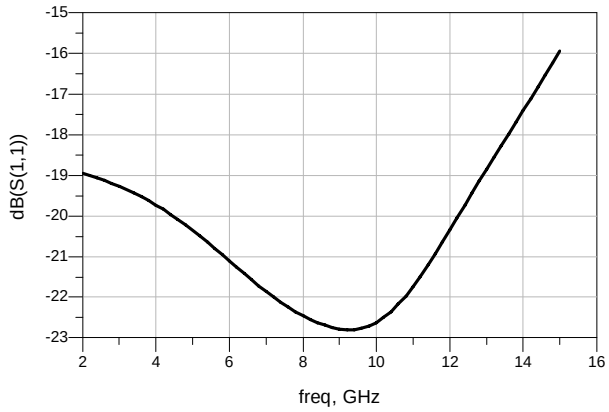

Figure 9: Input Matching (S_{11})

Output Matching (S_{22})

It is also required to make sure the output matching network does not change the DC bias of the active device. Since source follower is having very low output impedance,

it is very easy to achieve the required output matching without any filter network at the output. Thus in our proposed circuit it is kept less than –11.5 dB is throughout the 3 to 16 GHz band. This is shown in Figure 10.

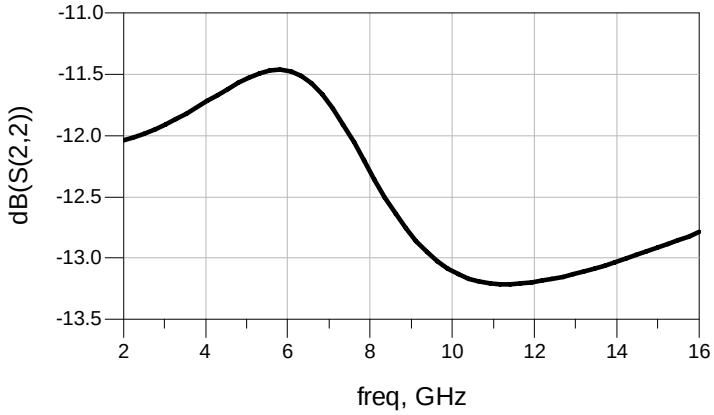

Figure 10: Output Matching (S_{22})

Reverse Isolation (S_{12})

The input–output isolation (S_{12}) is very important parameter to ensure better stability. If the isolation is poor; the output matching will affect the input matching. Since the Cascode stage eliminates the Miller capacitance, it is chosen to provide better isolation. In our proposed circuit a better reverse isolation of less than – 56 dB is achieved throughout the bandwidth as shown in Figure 11.

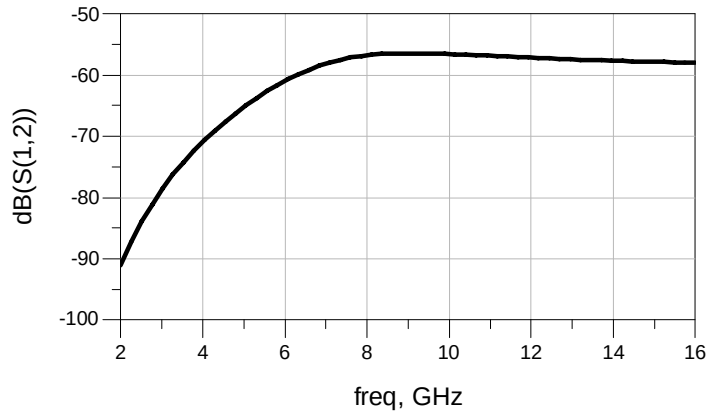

Figure 11: Reverse Isolation (S_{12})

Linearity (IIP3)

Linearity is the criterion that defines the upper limit of detectable RF input power and sets the dynamic range of the receiver. The linearity of an amplifier is described in

terms of 1dB compression point (P_{1dB}) and Third-order Input Intercept Point (IIP_3). The saturation effect begins once the main component of the output signal stops following the input signal with ideal ratio. This is known as 1 dB compression point and is defined as the level at which the gain drops by 1 dB. For the IIP_3, the inter modulation products will increase in amplitude by 3 dB when the input signal is raised by 1 dB. Since the UWB signal seldom suffers from gain compression in the LNA due to the low power of the received signal, only IIP_3 is very important. To measure the linearity of the proposed LNA, two test zones of – 20 dBm separated by 200 KHz with sweeping frequency range from 3 to 11 GHz are used. From the simulation result as shown in Figure 12, the achieved in band IIP_3 is – 3 dBm at the frequency of 8 GHz.

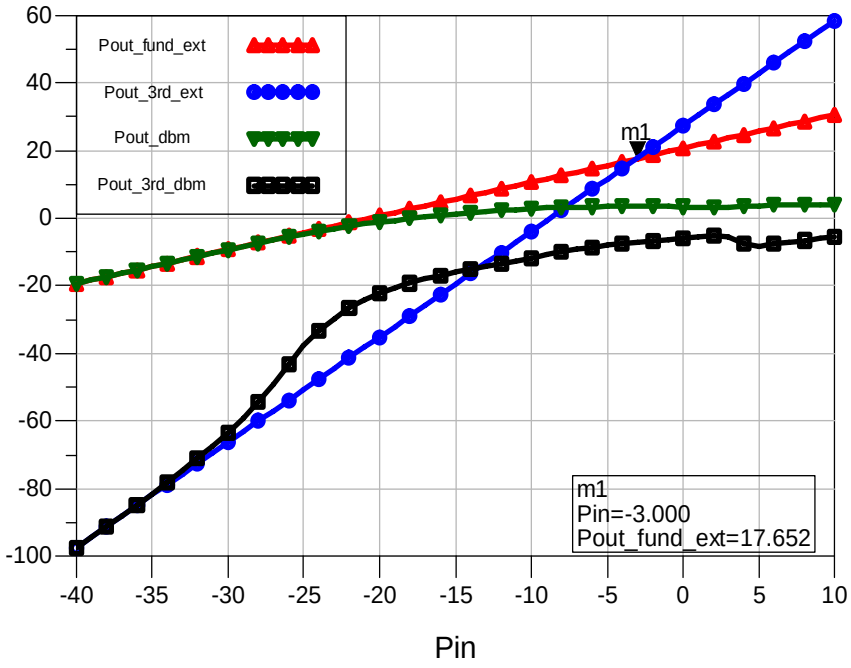

Figure 12: Input Third Order Intercept Point (IIP_3)

Stability Factor (K)

The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design of an LNA and can be determined from the S parameters, the matching networks, and the terminations. The stability factor, `*K*' is calculated over the frequency band 3 to 16 GHz by using the equation (9). From the simulation results as shown in Fig 13, it is evident that its value is greater than 1 and hence the circuit is unconditionally stable [9].

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \tag{9}$$

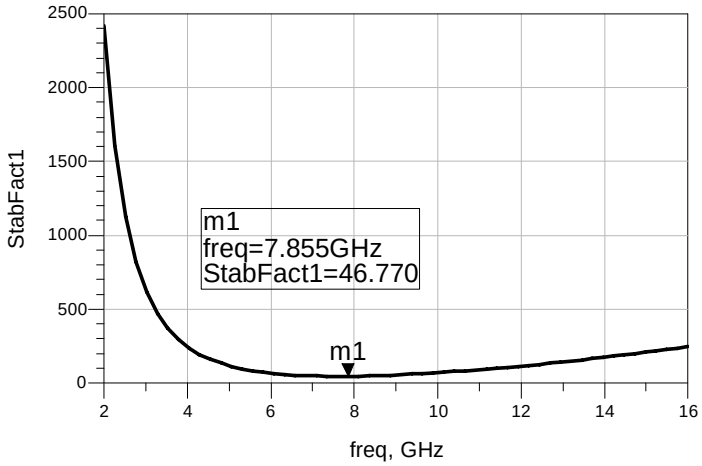

Figure 13: Stability Factor (K)

Power Consumption

As shown in Table 1, the proposed LNA consumes 3.548mW power at 1V power supply. This power consumption is calculated including the 1mA DC provided for the source follower. If it is omitted, the proposed circuit will consume dc power as low as 2.548mW.

Table 2 presents the simulation results summary our paper and comparison of recently reported CMOS UWB LNAs. From the comparison, it is evident that our LNA achieves very high gain for very wide bandwidth while providing better input matching with low noise figure and less power consumption.

Table 1: DC Current drawn from 1V power supply

Frequency	I_Probe	I_Probe *
0.000 Hz	3.548 mA	2.548 mA

* Without Buffer

Table 2: Simulation Results Summary & Comparison of Recently Reported CMOS UWB LNAs

	[3]	[4]	[5]	[6]	This Work
Technology	0.18µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	90 nm CMOS
BW_{-3dB} (GHz)	3.1 – 12.2	2 – 16	2 – 6.5	2 – 7.6	3 – 16
Gain S_{21} (dB)	10 – 13.1	10.7 – 12.3	17	13.1 – 13.8	14.6 – 17.6
NF (dB)	2.7 – 4.9	<2.8	2.5 – 2.7	1.85 – 2.1	2 – 3.5
IIP_3 (dBm)	- 9	-7	3.4 – 5.4	- 15.2	- 3
Input Matching S_{11} (dB)	< - 8.7	< -8.3	< - 10	< -10	< - 16
Output Matching S_{22} (dB)	< - 10.9	< -8	-	-	< - 11.5
Reverse Isolation S_{12} (dB)	-	-	-	-	< - 56
DC Power (mW)	13.9@ 1.8V	18.4@ 1.8V	7.6@ 1.8V	2.15@ 1.1V	3.548@ 1V

Conclusion

In this paper, the performance of current reuse LNA with shunt-series peaking with input CG amplifier for providing input matching instead of filter networks is analysed. The UWB LNA has been simulated in a 90nm CMOS technology. The achieved peak power gain achieved is 17.6 dB and the noise figure is less than 3.5 dB in the bandwidth of 3 to 16 GHz. The input matching achieved is below – 16 dB and the output matching is kept below – 11.5 dB. The reverse isolation is below – 56 dB throughout the entire band. This LNA consumes very low power of 3.548 mW from 1 V supply. The presented LNA claims the advantages of less design complexity, high bandwidth, better noise figure and low power.

References

[1] Federal Communications Commission (FCC), "First Report and Order", 2002.
[2] Maria Gabriella Di Benedetto, Guerino Giancola, 2004, "Understanding Ultra Wide Band Radio Fundamentals", Prentice Hall, Chapter: 1 – 2.
[3] Zhe Yang Huang, et al, 2008, "A 0.18μm CMOS Current Reused LNA with Gain Compensated for UWB Wireless Receiver", 23rd International Technical Conference on Circuits/Systems, Computers and Communications, pp: 437-440.
[4] K. Yousef, et al, 2011, "A 2-16 GHz CMOS Current Reuse Cascaded Ultra wideband Low Noise Amplifier", Electronics, Communications and Photonics Conference (SIECPC), pp: 1-5.
[5] Mohammad Sadeh Mehrjoo, Mohammad Yavari, 2010, "A new input matching techniques for Ultra Wideband LNAs", IEICE Electronics Express, Vol.7, No.18, pp: 1376-1381.
[6] Mohammad Sadeh Mehrjoo, Mohammad Yavari, 2011, "A Low Power UWB Very Low Noise Amplifier Using an Improved Noise Reduction Technique", Circuits and Systems (ISCAS) IEEE International Symposium, pp: 227-280.
[7] Thomas H. Lee, 2004, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, Chapter: 9-11.
[8] Behzad Razavi, 2001, "Design of Analog CMOS Integrated Circuits", McGraw Hill Publications, Chapter-3.
[9] Robert Caverly, 2007, "CMOS RF IC Design Principles", Artech House Publications, Chapter-4.