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Modeling and Analysis of Flyback Switching Power Converter using FPGA

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Abstract

This paper presents a modeling of Pulse Width Modulation (PWM) for conducted noise reduction in Switching Power Converters (SPC) using Field Programmable Gate Array (FPGA) based controller. Buck boost Flyback converter is the preferred choice among variety of switching power converters due to its low component count, cost-effective structure as well as its large dynamic range. Converters should act in agreement with Electro-Magnetic Compatibility (EMC) rules so that the Electro-Magnetic Interference (EMI) caused by switching cannot obstruct the normal operation of adjacent circuits and also the converter itself. In this paper, some techniques are used in switching converters to suppress EMI with emphasis on its conduction form. EMI analysis and evaluation of a conventional flyback converter is achieved by simulation results. According to the simulated results, the circuit and parameters of the converter are modified. Experimental results are included to verify the validity of the proposed method. The proposed model is easy to apply in practice for understanding, diagnosing and approximating EMI behaviors and to improve EMI in the topology design stage. The resulting model assumes a minimum number of noise sources and contains essential coupling paths that allow easy physical interpretations.

Keywords*:* Electro-Magnetic Interference, switching power converters, modeling.

Introduction

The flyback circuit topology has attracted interest from many researches when utilizing AC as an input source [1]. However, the drawbacks of flyback converter are high ripple output voltage, poor regulation, and low-power DC conversion. Increasing power density of switch mode power supplies increases their switching frequency which becomes a challenging obstacle for EMI mitigation. The passive EMI suppression technique has always been the primary solution to fulfill the EMC requirement in terms of conducted emission limits. In this paper FPGA-based EMI modeling technique to mitigate the conducted emission of switch mode power converter is proposed. Switching power supply consists of two parts, one is converter section and the other is control section. The converter section is composed of the switching elements, the auxiliary devices, and the conductors to the load. The switching elements are semiconductor devices with switching frequency from ten kilohertz to a few Megahertz [2]. During turn-on and turn-off operations they give rise to rapid voltage and current transients (di/dt and dv/dt). These transients are the sources of conducted and radiated EMI. This disturbs not only other utilities indirectly connected to the polluting device, but also the device itself.

For cost-effective design approach, EMC should be considered at early stage of the power converter design. Hence, designing to achieve EMC involves a series of measures to reduce emissions at the source. This can be done by identifying and minimizing the coupling paths and diverting noise away from ground. As product development progresses from the design stage to testing the prototype and mass production, the range of available noise suppression techniques decreases steadily. As the first step, the power converter should be analyzed for its EMI generation to determine the required measures of suppressions that can be implemented at the design stage without the need for passive EMI filters.

The switching power converter is based on a non-linear action of the switching devices, such as MOSFETs which are controlled by the pulse modulated signal with variable or fixed frequency, to step-down or to step-up the input voltage to a desired level. These switching waveforms contain significant energy levels at the fundamental switching frequency and its multiple harmonics and therefore generate EMI problems. The issues with the existing methods in terms of their performance and their limitations have covered the way for the proposed technique that surpasses some drawbacks. The Digital-signal-processor (DSP) based solution for modeling has a slight disadvantage which resides in the delay embedded in the execution of the algorithm instructions that is processed sequentially [3]. This execution delay can results in phase lag between the sensed signal and the injected signal which has a direct impact on the attenuation performance. Therefore, an FPGA based EMI modeling is proposed to alleviate the problem of the phase delay while using the same interface circuit. This method uses a FPGA device, in order to exploit its concurrent operation.

All the internal logic elements of FPGA and the control algorithm are executed continuously and simultaneously. The control algorithm has been developed in Very high speed integrated circuit Hardware Description Language (VHDL) [4]-[6]. This method is as flexible as any software solution the same can be synthesized into any

FPGA device and even has a possible direct path to a custom chip. In this way, the FPGA could be substituted by an Application Specific Integrated Circuit (ASIC), opening interesting possibilities in EMI modeling techniques in terms of performance, cost and flexibility. VHDL has been used for modeling the phase inversion by using a logic inverter implemented in VHDL [7].

Analysis of Flyback Converter

The model of the supply takes into account the main parasitic elements of its electronic component parts. The model is implemented using only basic functions of MATLAB programming environment. The modeling and implementation procedure can be used to analyze more complex DC-DC converters.

One of the major advantages of Flyback converter is that they don't require an output filter inductor, thus saving cost and volume. This also makes Flyback converters valuable for high output voltages unlike forward converters which have an output inductor potentially causing problems as the inductor must sustain large voltages. Flyback also doesn't require a high voltage freewheeling diode.

The filter capacitor at the output is typically larger in Flyback converters as it alone supplies the load current when the transistor is ON. Equivalently the full DC current flows from ground through the capacitor to the load during the transistor ON time. Thus the ripple current rating of the capacitor and output ripple voltage requirement collectively determines the final choice of output filter capacitor.

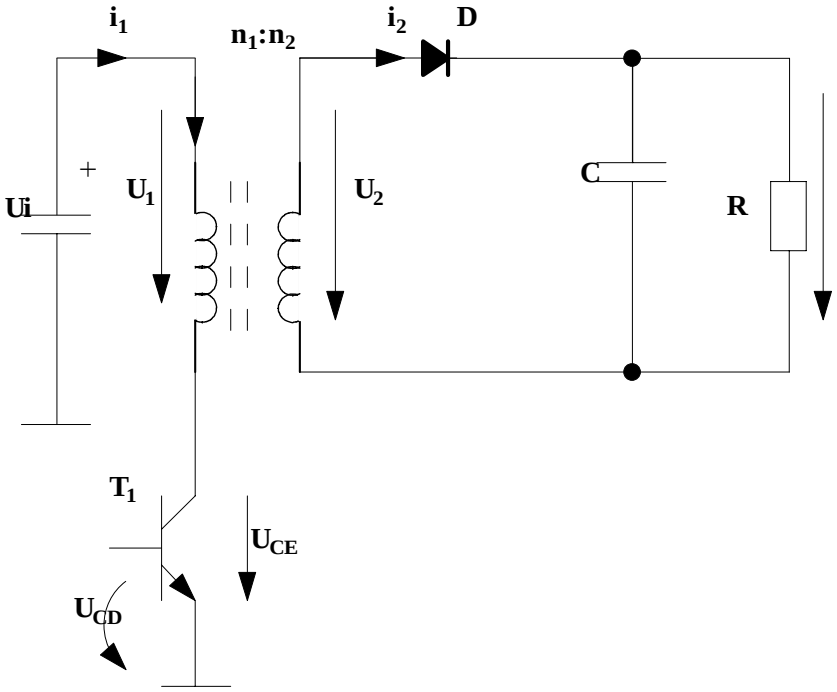

Figure 1: Fly-Back Topology

The circuit diagram of a Fly-back switching power converter as shown in Fig.1.When the transistor is in ON state primary winding of transformer act as an inductor. The transformer assures the isolation between the load and the input power supply when the transformer T1 is turned OFF. It provides an output voltage as load circuit request as long as there is energy stored in the magnetic core with turns ratio *n = n1 / n2.*

The waveforms that describe the operation modes of the switched mode Fly-back converter are shown in Fig.2. If the converter operates in steady state Continuous Conduction Mode (CCM) which means the energy that exist the operation in transformer is greater or at least equal to zero during the supply and if input *Ui* and output U_O voltages are considered for simplicity both constant using the volt-second balance or the primary winding, one can derive the next relation:

$$U_O = N^{-1} \frac{\alpha}{1-\alpha} U_i \tag{1}$$

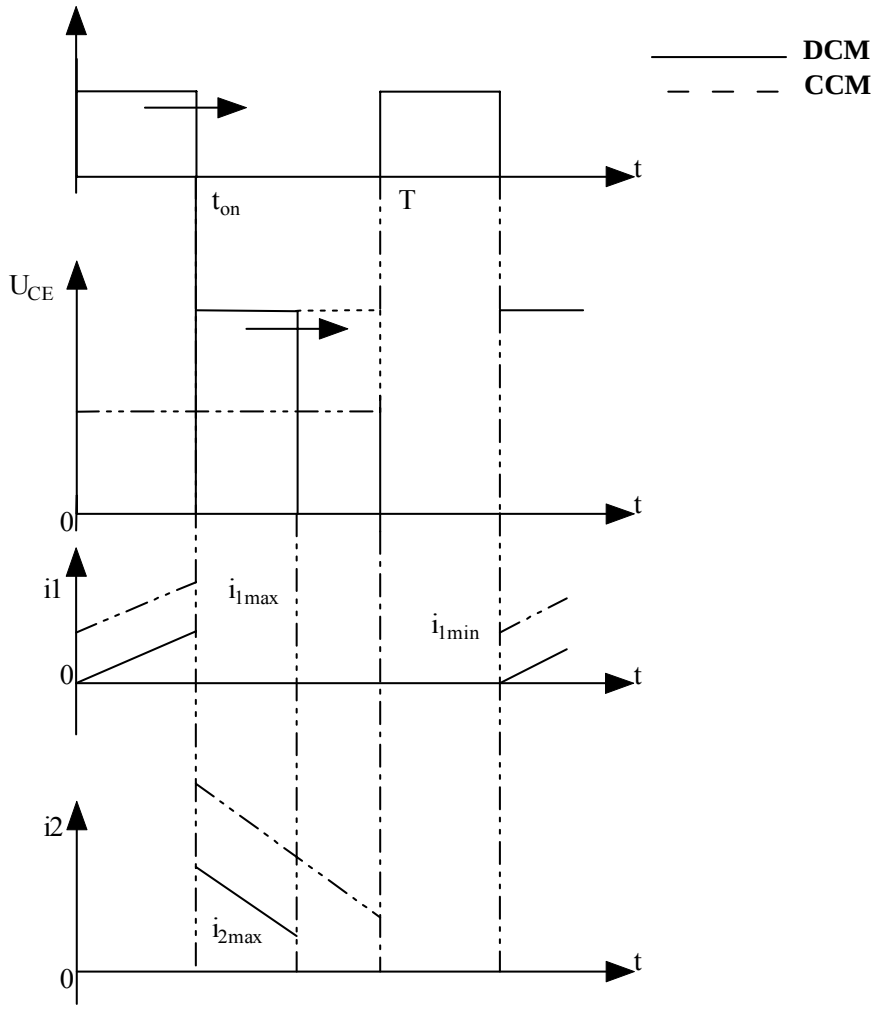

Figure 2: Wave forms for DCM and CCM

In (1) α is the duty cycle of the pulse width modulated command voltage *ucd* which has a constant time period *T* when the transistor *T1* is turned ON, the current *i1* can be described by the next equation:

$$i_{1\max} - i_{1\min} = \frac{U\,i}{L_1}\alpha\,T \tag{2}$$

The average current through diode *D* reflected in the primary winding of the transformer *Tr* is obtained with the next relation:

$$\frac{i_{1\max} + i_{1\min}}{2} = n^{-1}\,\frac{U\,o}{(1-\alpha)R} \tag{3}$$

From (2) and (3) one can derive the minimum value of the primary winding inductance at the boundary condition between CCM and discontinuous conduction mode (DCM), when $i1min = 0$, with the following relation:

$$L_{1\min} = \frac{1}{2}n^2(1-\alpha)^2 RT. \tag{4}$$

The relation (4) is useful in the design of the switched mode Fly-back converter.

Simulation Models

Various PWM techniques differ in concept and performance are widely used to control the output of power converters. Sinusoidal PWM, hysteresis PWM, space vector modulation (SVM), and optimal PWM techniques based on performance criteria are some of the widely used strategies [8]. In sinusoidal PWM, the sinusoidal modulating signal is compared with a triangular carrier signal to generate gate signals of the converter switches that can be implemented easily by using analog techniques. However, the use of analog comparators does not produce a fixed relation between the carrier signal and the reference signal but will introduce sub-harmonics into the system. Recent developments have made it possible to generate sinusoidal PWM digitally. In this paper, a modified sinusoidal PWM, capable of minimizing harmonics present on the AC side of the converter system is implemented by using a FPGA [9].

PWM is the most widely used method for controlling the output voltage. It maintains a constant switching frequency and varies the duty cycle. Duty cycle is defined as the ratio of switch on time to reciprocal of the switching frequency. Since the switching frequency is fixed, this modulation scheme has a relatively narrow noise spectrum allowing a simple low pass filter to sharply reduce peak-to-peak ripple at output voltage [10]. This requirement is achieved by arranging an inductor and capacitor in the converter in such a manner as to form a low pass filter network. This requires the frequency of low pass filter to be much less than switching frequency [11].

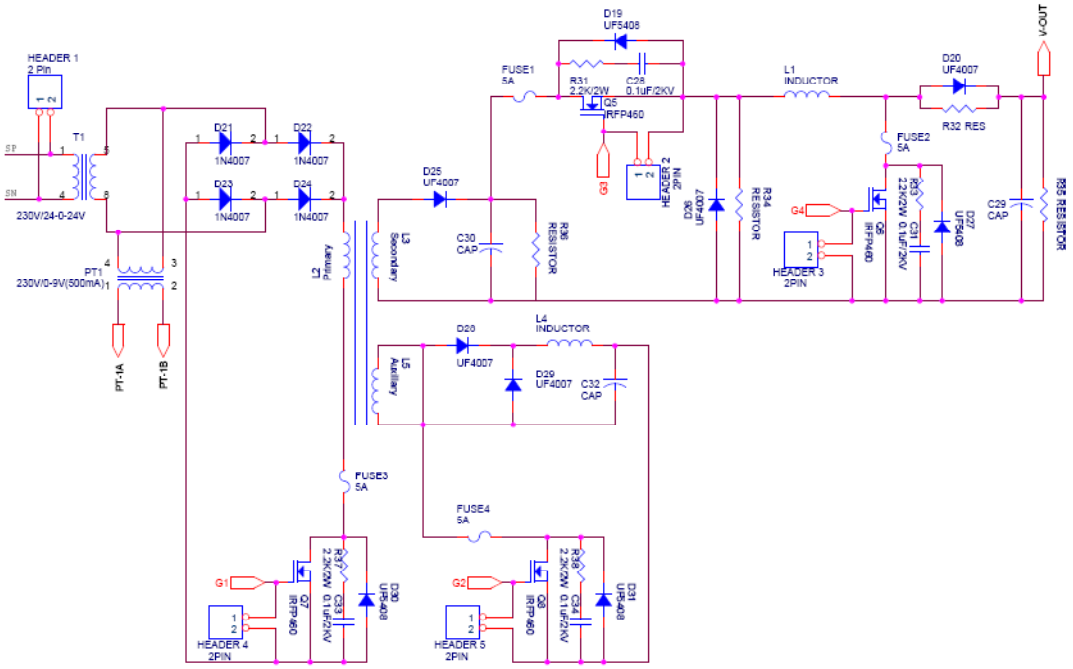

Figure 3: Buck Boost Flyback Converter

Fig. 3 shows the simulation model of the Buck Boost Flyback Converter. The proposed converter used here having many advantages, it uses 10V gate driver circuit to minimize the power loss in the external MOSFET and has an operational current of typically180µA that can accommodate off-line, Telecom and non-isolated applications. It provides internal under voltage lockout, slope compensation and peak current limiting to minimize the external component count. This buck boost Flyback converter gives 330 kHz frequency of operation and also it uses current mode architecture to regulate the feedback voltage.

Simulation and Hardware Results

For simulation and experiments uses a transformer that presents the characteristics of maximum output power 9W, inductance of primary winding is about 30µH (including leakage inductance) when the secondary winding is floating and finally and $n2 = 9*n$

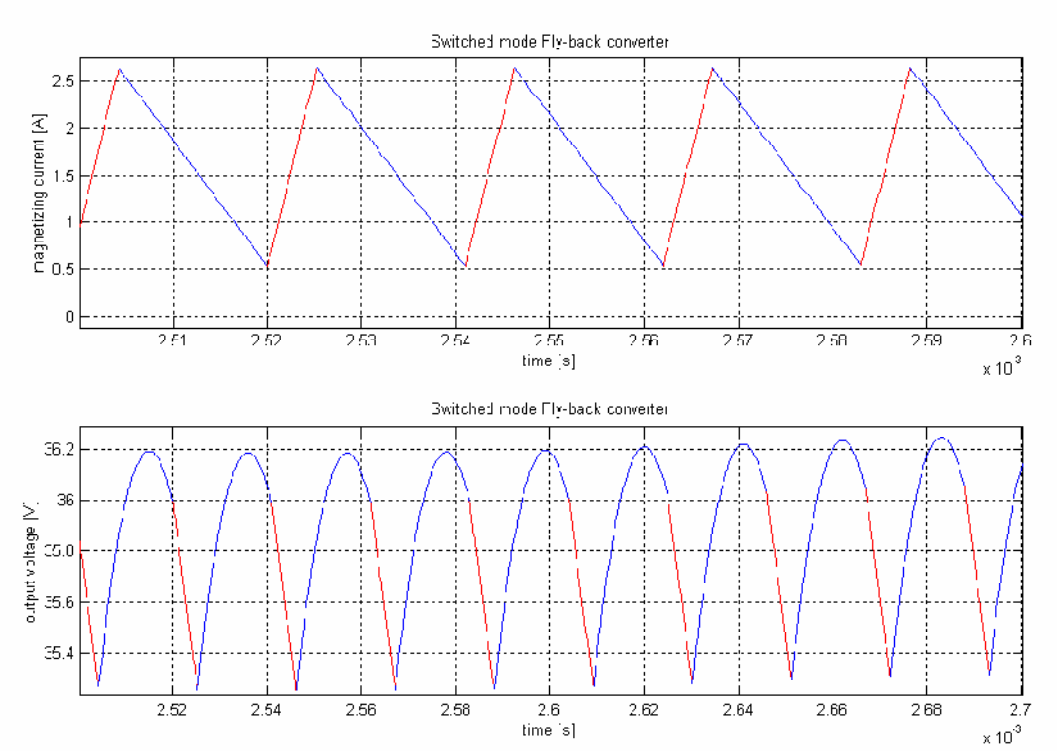

Figure 4: Continuous Conduction Mode.

The switching period of the transistor is T
$C1$ = 21µs and the input voltage is U = 12V

The output filtering capacitor is C = 940 nF/630V. In the Fig.4 shows the simulation result for CCM operating mode. The peak of the current through magnetizing inductance and average value of the output voltage increase their values gradually with the duty cycle of the command voltage for the transistor T. The output ripple also increase but is limited to few hundred of mV that is acceptable for a switched mode supply.

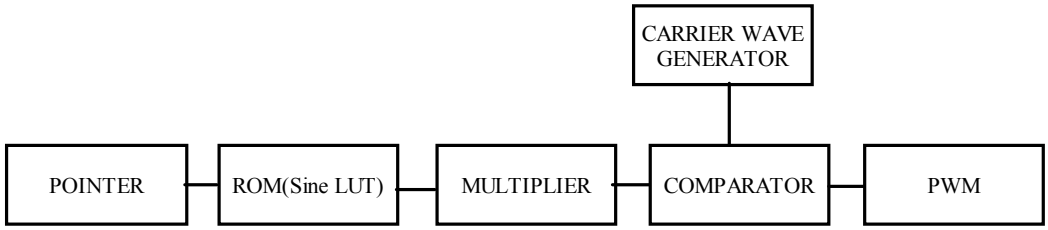

Figure 5: A typical block diagram of a PWM generator

Fig.5 shows the basic structure for generating digital PWM. Figure.6 shows the reference voltage compared with a high-frequency triangular carrier wave. The comparator output forms the switching state of the corresponding rectifier leg.

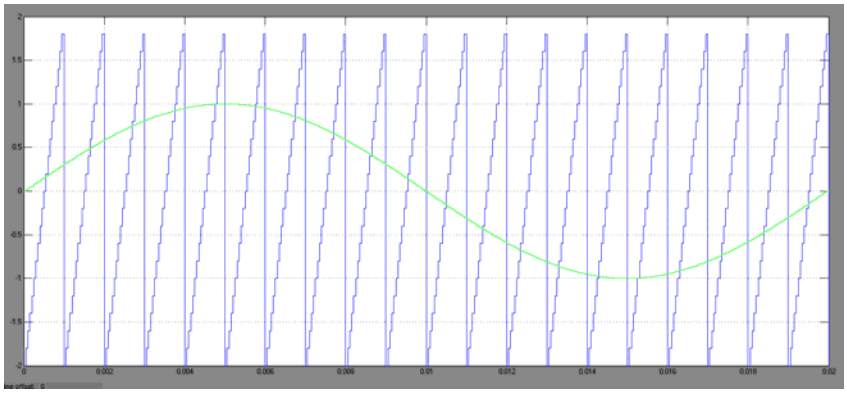

Figure 6: Carrier signal Vs modulating Signal

In Fig.6, the triangular carrier is generated digitally by using an UP/DOWN counter. The counter is clocked by a clock generated by the internal phase-locked loop (PLL) of the FPGA. The relationship between the carrier frequency and the main clock frequency of the UP/DOWN counter is

$$fc = \frac{fclk}{(2n-1).2} \tag{5}$$

where *fc* is the carrier frequency, *fclk* is the main clock frequency, and *n* is the number of bits of the UP/DOWN counter.

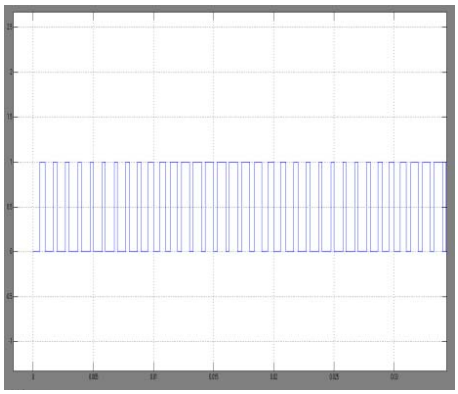

Figure 7: Generated PWM pattern in Matlab Simulink

In this model, an 8-bit UP/DOWN counter will generate a carrier wave of approximately 19.6 kHz from the main clock frequency of 10MHz. The sinusoidal

waveform uses 60° look-up table, where 60 sampled data is stored into the EPROM. A MOD 60 counter acts as a pointer for these data. The amplitude of the carrier wave is fixed at 255 while the amplitude of the modulating wave can be varied by multiplying the look-up table data with input from the user. The output of the PWM generator produces PWM patterns as shown in Fig. 7. Fig. 8 shows the PWM waveforms generated by FPGA. The simulated PWM signals are applied into the flyback converters.

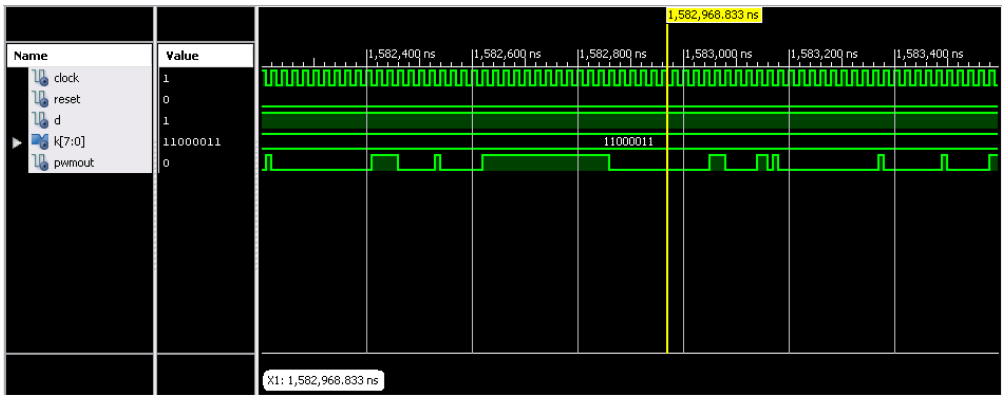

Figure 8: Simulation result for PWM waveform generated using FPGA

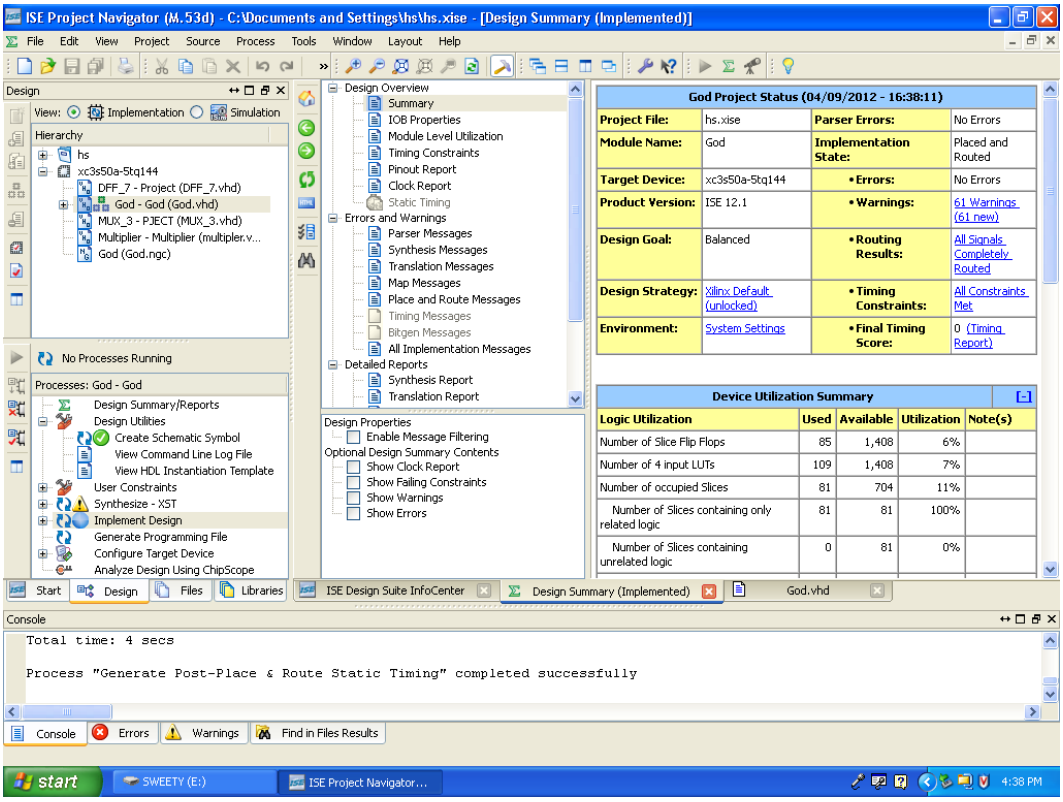

Figure 9: Design Summary

The MOSFET switches are controlled by the switching pattern signals which are applied into the flyback converter. The Design summary block as shown Fig.9 is added to the model for analyzing and synthesizing the design. A netlist, containing information of logic gates and their interconnections, will be created and will be used to realize the target circuit in the hardware. The fitting process in the compiler will map the design into the target before placing the parts and routing the paths between the components based on the specified timing requirements. Once the fitting process is completed, the design is ready to be programmed into the FPGA. Fig. 10 shows the PWM waveforms generated by experimental setup using FPGA. Figure.11 shows the AC source voltage and current which are almost in phase. Fig.12 shows the photograph of FPGA hardware for PWM generation.

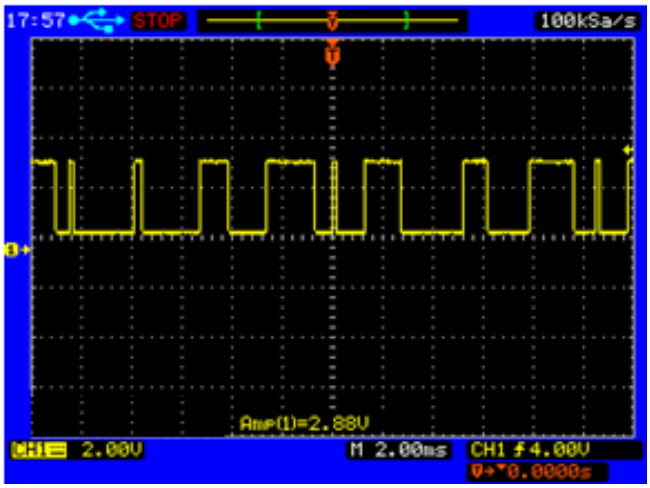

Figure 10: Experimental result for PWM waveform generated using FPGA

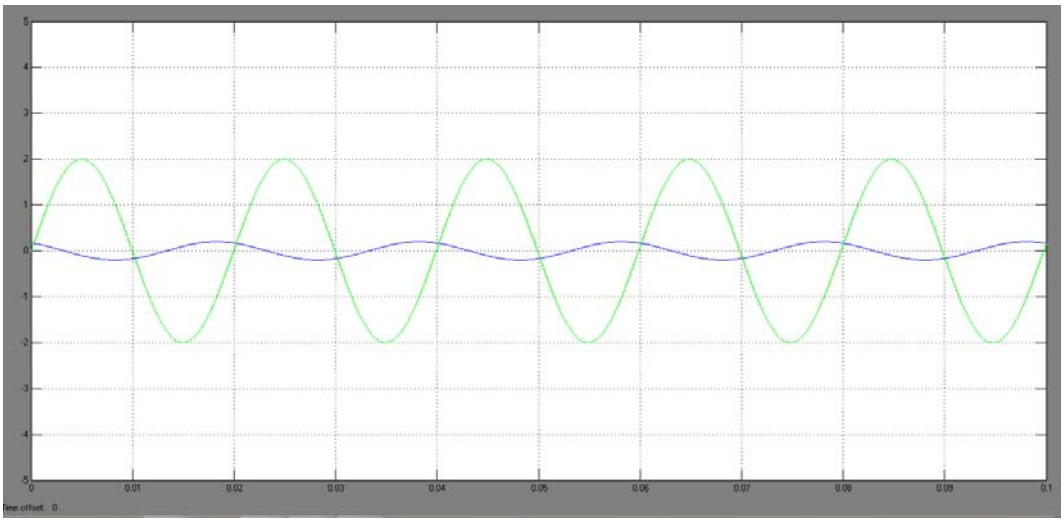

Figure 11: AC voltage and current of flyback converter in Matlab Simulink

Figure 12: Photograph of the FPGA hardware.

Conclusion`

Modeling of flyback converter as well as PWM generator, based on FPGA configuration, has been developed in Matlab Simulink environment. Simulation results are provided and the experiment result of the generated PWM signals is presented. In this paper, a modeling procedure applied to a switched mode Fly-back converter and using the standard functions from MATLAB programming environment, they implemented a program able to simulate the operation of this supply are presented. This EMI modeling helps designers to predict EMI levels in the design stage and before system realization. FPGA is shown to offer the flexibility to reconfigure the design of a PWM circuit without modification to hardware.

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