International Journal of Electrical Engineering.
ISSN 0974-2158 Volume 5, Number 7 (2012), pp. 853-862

http://www.irphouse.com

A Novel FPGA based PWM Active Power Filter for Harmonics Elimination in Power System

[1]Sreekanth C. and [2]Dr.Moni R.

[1.] Asst. Professor, Dept. Of Electronics & Instrumentation Engg,
[2.] Professor, Dept. Of Electrical & Electronics Engg,
Noorul Islam University, Kumaracoil – 629180. India.
[1.]Email :sreekanthc76@gmail.com
[2.]Email: moni2006_r_s@yahoo.co.in

Abstract

Most of the pollution issues created in power systems are due to the non-linear characteristics and fast switching of power electronic equipment. Power quality issues are becoming stronger because sensitive equipment has been more sensitive for market competition reasons, equipment will continue polluting the system more and more due to cost increase caused by the built-in compensation and sometimes for the lack of enforced regulations. Active power filters have been developed to solve these problems to improve power quality. Shunt active power filter have been used to eliminate load current harmonics and also for reactive power compensation. The Active Power Filter (APF) has been implemented with Pulse Width Modulation (PWM) based on current controlled Voltage Source Inverter (VSI). This VSI switching signals have been generated through proposed three-level Hysteresis Current Controller (HCC) that achieves significant reduction in the magnitude and variation of the switching frequency. The system has been modeled and investigated under different unbalanced non-linear load conditions. The simulation results reveal that the active power filter has been effectively compensating the current harmonics. Due to non-linear characteristics, the load current gets distorted which causes undesirable effects like heating, equipment damages etc. in power network. APF is the best solution for eliminating the harmonics caused by the non-linear loads. This paper presents the three-phase four-wire active filter for Power Line Conditioning (PLC) to improve power quality in the distribution network and also implementation of a digitally controlled APF. Synchronous reference frame has been used for generation of reference current. PI currents algorithm and HCC together has been written in VHDL code and were implemented using SPARTAN VI

FPGA platform. Various simulation results has been presented under steady state and transient state condition and their performances has been analyzed. Simulation results obtained shows that the performance of three phase system with APF has been found to be better and a digital controller add a new aspect for the controller from low cost, high speed and hardware implementation. Thus PWM and hysteresis based current control has been used to obtain the switching signals to the VSI.

Keywords: Active Power Filter, Hysteresis Current Control, Harmonics, Voltage Source Inverter, Power Line Conditioning

1. Introduction

The large usages of power electronic devices cause disturbances on the electrical supply network. The disturbances are due to the use of non-linear devices. These devices will introduce harmonics in the power system thereby causing equipment overheating and device damage. Several methods were described in various papers to solve these problems. The concept of using APF to mitigate harmonics and to compensate reactive power was proposed 'in ref. 1,2' Harmonics-Causes, Effects, Measurements, and Analysis are described in detail 'in ref.3'. Active Power Line Conditioning Methodologies is explained 'in ref.4'. Continuing proliferation of nonlinear loads such as power converters, SMPS, photo copiers, printer, UPS, ASDs were creating disturbances like harmonic pollution and reactive power problems in the power distribution lines 'in ref. 5,6'. Conventionally these problems were solved by passive L-C filters. But these L-C filters introduce tuning, aging, resonance problems and were suited only for fixed harmonic compensation. So active power-line conditioners have become popular than passive filters. It compensates the harmonics and reactive power simultaneously. The active power filter topology can be connected in series or shunt and combinations of both. Passive filters combined with active shunt and series were some typical (hybrid) configurations that can be used for the same purpose. Shunt active filter has been more popular than series filter, because most of the industrial applications require current harmonics compensation 'in ref. 7'. The shunt active power converter can be executed with Current Source Inverter (CSI) or VSI. The voltage source inverter has three coupling inductors in series in the ac-side and an energy storage capacitor on the dc-side. Similarly, the current source inverter has three coupling capacitors in parallel in the ac-side and an energy storage inductor in series with the dc-side 'in ref. 8'. In general, the voltage source inverter type has been preferred for the shunt active power circuit due to the lower losses in the dc-side and also possible to create multilevel inverter topologies for higher power level applications. The current control techniques of the voltage source inverters can be broadly classified into linear and non-linear controller. The SRF (Synchronous Reference Frame) theory has been used for generation of reference currents from distorted load currents 'in ref. 9. The control scheme was based on sensing line currents only; an approach different from convention ones, which were based on sensing harmonics and reactive volt-ampere requirements of the nonlinear load. The

three-phase currents/voltages were detected using only two current/voltage sensors. The DC capacitor voltage has been regulated to estimate the reference current template. The role of the DC capacitor was described to estimate the reference current 'in ref. 10'. The hysteresis and adaptive hysteresis method was used for gating pulse generation 'in ref. 11'. But as discussed these analog controllers were having drawbacks during real-time implementations and the difficulties can be overcome by adopting digital controller (FPGA).

Rest of the paper is organized as follows:
Extraction of compensation current is given in section 2. Estimation of source current is explained in section 3. Section 4 discusses about the role of dc side capacitor and about SRF controller implementation in section 5.Section 6 describes about the simulated results and its discussion, followed by the conclusion of the present research work in Section 7.

2. EXTRACTION OF COMPENSATION CURRENT

Figure 1 shows the overview of APF connected to the power network based on compensation principle of a shunt active power filter. It is controlled to draw or supply a compensating current i_c from the utility, so that it cancels current harmonics on the AC side, and makes the source current in phase with the source voltage. The load current waveform, the desired mains current and compensating current injected by the active filter containing all the harmonics, to make mains current sinusoidal.

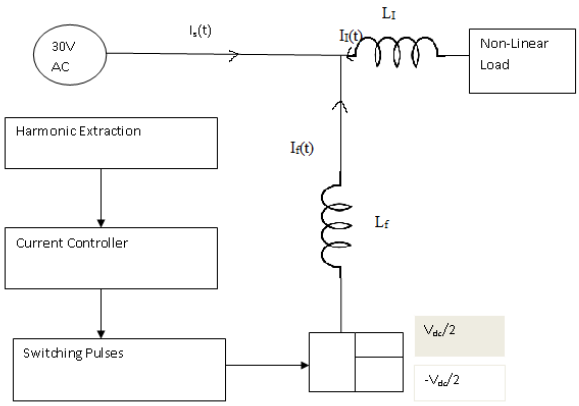

Figure 1: Overview of APF connected to the power network

From Figure 1, the instantaneous current can be rewritten as:

$$i_s(t) = i_l(t) + i_f(t) \quad (1)$$

Source Voltage is given as

$$V_s(t) = V_m \sin\omega(t) \quad (2)$$

If a non-linear load is applied, then the load current will have a fundamental component and harmonic components which can be represented as:

$$i_I(t) = \sum (\ln \sin (n\omega(t) + \phi) \qquad (3)$$

3. ESTIMATION OF SOURCE CURRENT

The peak value of the reference current can be estimated by controlling the DC side capacitor voltage. Ideal compensation requires the mains current to be sinusoidal and in phase with the source voltage, irrespective of the load current nature. The desired source currents, after compensation, can be given as:

$$I_{sa}^*(t) = I_{sp}\sin wt \qquad (4)$$

$$I_{sb}^*(t) = I_{sp}\sin(wt-1200) \qquad (5)$$

$$I_{sc}^*(t) = I_{sp}\sin(wt+1200) \qquad (6)$$

Where I_{sp} ($=I_1\cos\Phi_1+I_{sl}$) is the amplitude of the desired source current, while the phase angle can be obtained from the source voltages. Hence, the waveform and phases of the source currents are known, and only the magnitudes of the source currents need to be determined. This peak value of the reference current has been estimated by regulating the DC side capacitor voltage of the PWM inverter. This capacitor voltage is compared with a reference value and the error is processed in a PI controller. The SRF theory is used for reference current generation and also the reference currents can be estimated by multiplying this peak value with unit sine vectors in phase with the source voltages.

4. ROLE OF DC SIDE CAPACITOR

The DC side capacitor serves two main purposes: (i) it maintains a DC voltage with small ripple in steady state, and (ii) serves as an energy storage element to supply real power difference between load and source during the transient period. In the steady state, the real power supplied by the source should be equal to the real power demand of the load plus a small power to compensate the losses in the active filter. Thus, the DC capacitor voltage can be maintained at a reference value. However, when the load condition changes, the real power balance between the mains and the load will be disturbed. This real power difference is to be compensated by the DC capacitor. This changes the DC capacitor voltage away from the reference voltage. In order to keep satisfactory operation of the active filter, the peak value of the reference current must be adjusted to proportionally change the real power drawn from the source. This real power charged/discharged by the capacitor compensates the real power consumed by the load. If the DC capacitor voltage is recovered and attains the reference voltage, the real power supplied by the source is supposed to be equal to that consumed by the load again. Thus, in this fashion the peak value or the reference source current can be obtained by regulating the average voltage of the DC capacitor. A smaller DC capacitor voltage than the reference voltage means that the real power supplied by the

source is not enough to supply the load demand. Therefore, the source current (i.e. the real power drawn from the source) needs to be increased, while a larger DC capacitor voltage than the reference voltage tries to decrease the reference source current. This change in capacitor voltage has been verified from the simulation results. The real/reactive power injection may result in the ripple voltage of the DC capacitor. A low pass filter is generally used to filter these ripples, which introduce a finite delay. To avoid the use of this low pass filter the capacitor voltage is sampled at the zero crossing of the source voltage. A continuously changing reference current makes the compensation non-instantaneous during transient. Hence, this voltage is sampled at the zero crossing of one of the phase voltage, which makes the compensation instantaneous. Sampling only twice in cycle as compared to six times in a cycle leads to a slightly higher DC capacitor voltage rise/drop during transients, but settling time is less.

5. SRF CONTROLLER IMPLEMENTATION

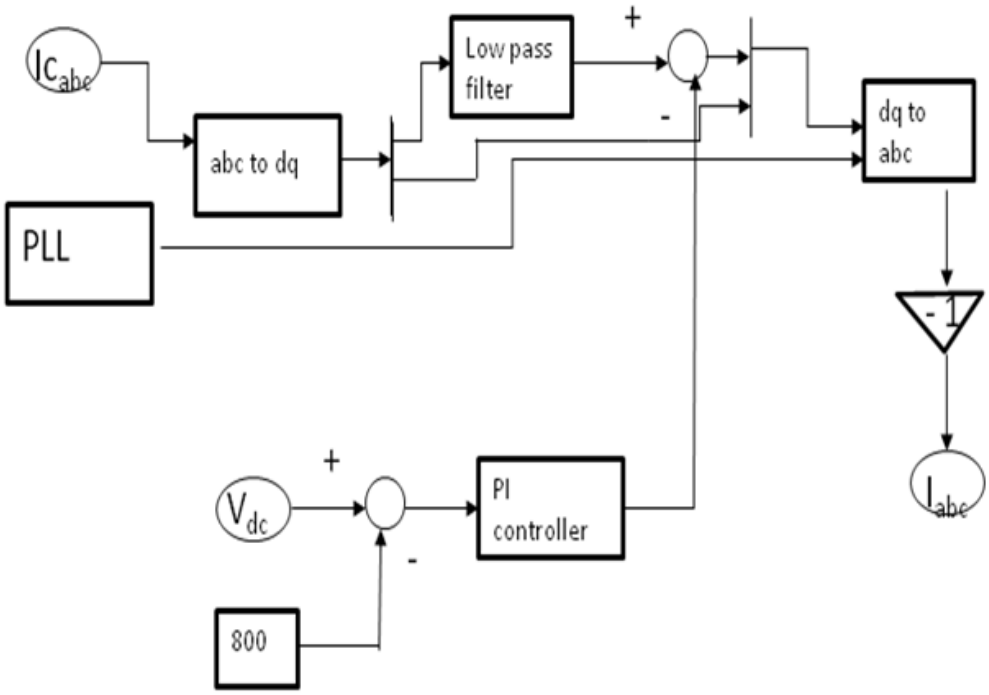

Figure 2: Synchronous d-q-0 reference frame based compensation algorithm.

In Figure 2, the PLL circuit provides the vectorized 50 Hz frequency and 300 phase angle followed by sin and cosθ sinθ for synchronization. The id-iq current are passed through Low Pass Filter (LPF) for filtering the harmonic components of the load current, which allows only the fundamental frequency components. The LPF is a second order Butterworth filter, whose cut off frequency is selected to be 50 Hz for

eliminating the higher order harmonics. The PI controller is used to eliminate the steady state error of the DC component of the d-axis reference signals. Furthermore, it maintains the axis capacitor voltage nearly constant. The DC-side capacitor voltage of PWM-voltage source inverter is sensed and compared with desired reference voltage for calculating the error voltage. This error voltage is passed through a PI controller whose propagation gain (K_P) and integral gain (K_I) is 0.1 and 1 respectively.

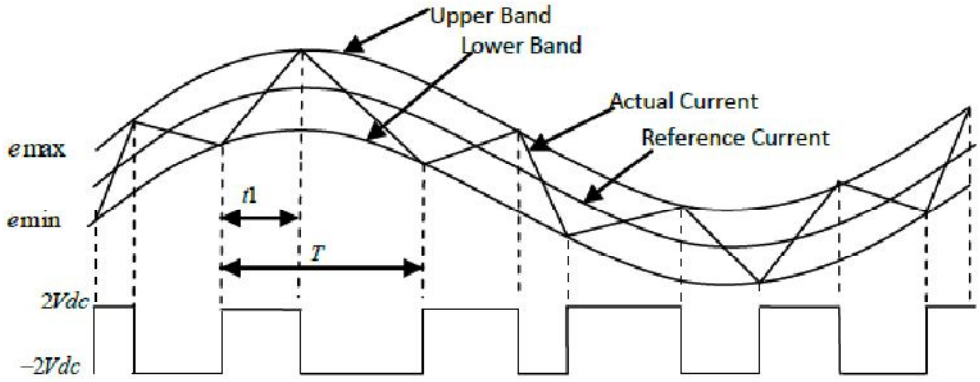

Figure 3: Diagram of two-level hysteresis current control

Conventional hysteresis current control operates the PWM voltage source inverter by comparing the current error against fixed hysteresis bands. This current error is difference between the desired current and the current being injected by the inverter as shown in Figure 3. If the error current exceeds the upper limit of the hysteresis band, the upper switch of the inverter arm is turned OFF and the lower switch is turned ON. If the error current crosses the lower limit of the hysteresis band, the lower switch of the inverter arm is turned OFF and the upper switch is turned ON. These two level switching strategies does not use the inverter zero output condition, but the 3-level switching is possible by incorporating zero level.

This control strategy of the switching frequency is determined as follows. The rate of change of phase current at any point of time is written as:

$$\frac{dI}{dt} = \frac{\pm 2Vdc}{L} \tag{7}$$

Where ΔI is rate of change of inverter current, Δt is rate of change of time period and L is the series inductance of the filter. A complete switching cycle goes from $0 \rightarrow t_1 \rightarrow T$

For the period $0 \rightarrow t_1$ and therefore:

$$t_1 = \frac{+\Delta IL}{2Vdc} \tag{8}$$

For the period $t_1 \rightarrow T/2$, $\Delta t = T - t_1$ and therefore:

$$T - t_1 = \frac{-\Delta IL}{-2Vdc} \tag{9}$$

The total switching time is obtained by combining these two equations and it give as:

$$f_s = \frac{1}{T} = \frac{Vdc}{\Delta IL}; \quad f_{max} = \frac{Vdc}{\Delta IL} \tag{10}$$

Here f_{max} is maximum switching frequency of the inverter. The variation in the switching frequency influences the performance of the current controller, both in terms of harmonics and the maximum switching frequency.

6. Results and Discussions

The performance of the three-phase four-wire shunt APLC system has been evaluated through MATLAB programs in order to program and test the system under unbalanced non-linear load conditions. The system parameters values are; Line to line source voltage is 1000 V; System frequency (f) is 50 Hz; DC-link capacitor C1=1100 µF and C2=1100 µF; Reference dc voltage 1200 V. The three-phase four-wire AC power supply connected to the unbalanced non-linear load. Figure 4 (a), (b) shows the gating pulses generated using FPGA (Spartan 6) as digital controller.

Figure 4 (a), (b): Gate pulses generated using FPGA as digital controller

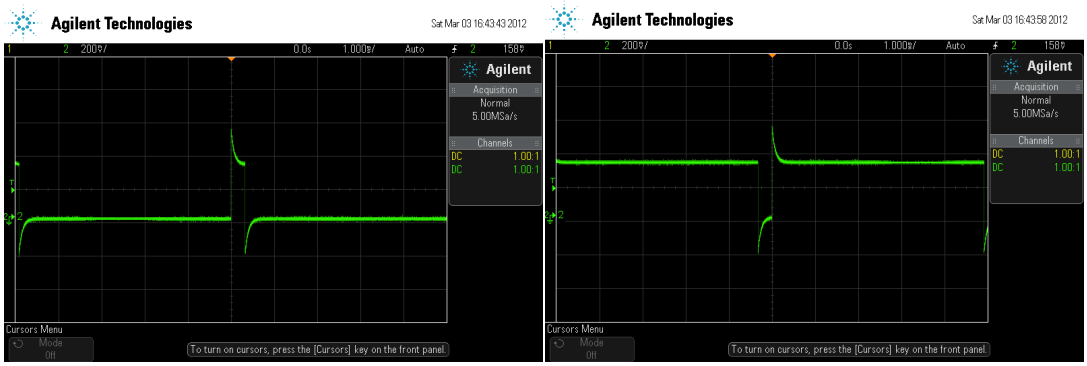

Figure 5 (a) :Gating pulse for S1 and S3 MOSFET (b): Gating pulse for S2 and S4 MOSFET

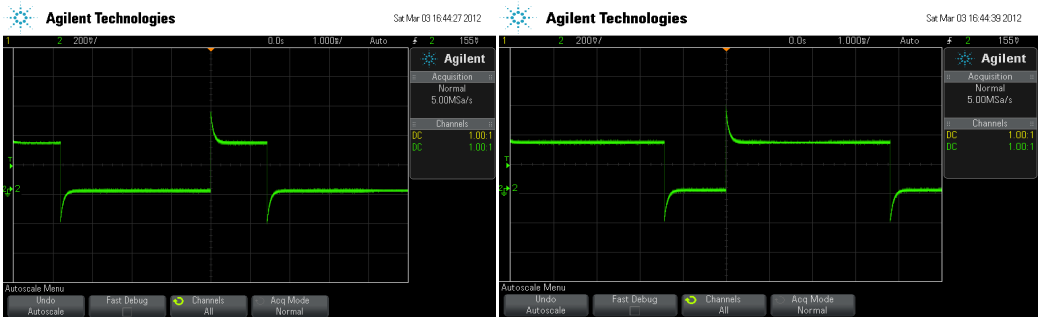

Figure 6 (a), (b):Gating pulse variations

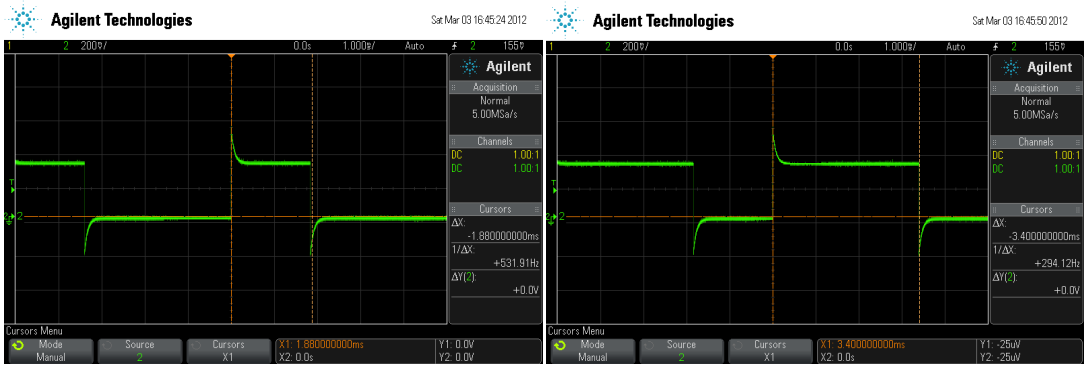

Figure 7 (a),(b) :Gating pulse variations measurement

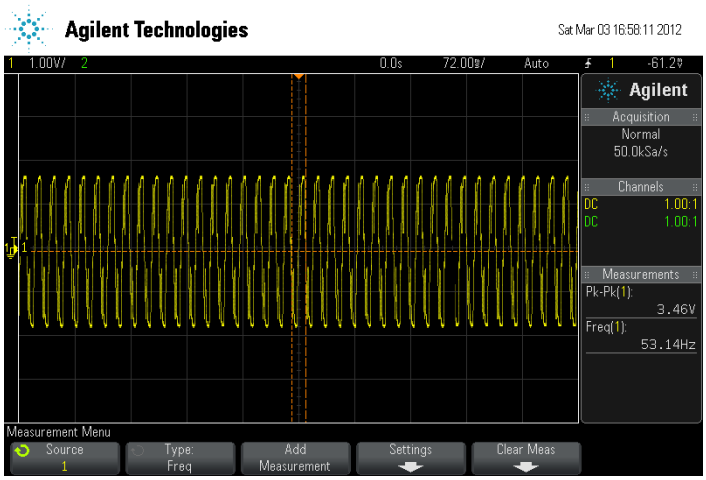

Figure 8:Gating source current after compensation

Figure 5 (a) shows the gating pulse for S1 and S3 MOSFET and 5 (b) denotes the gating pulse for S2 and S4 MOSFET. Similarly Figures 6 (a), (b) and 7(a), (b) shows the gating pulse variations. Finally Gating source current after compensation is shown in Figure 8.

Input is taken as 1000 V 3-phase power supply and it is given as the input to the system in which nonlinear load is applied.

7. Conclusion

Thus this paper has presented about the design and implementation of FPGA based three level hysteresis current control scheme for three-phase four-wire active power line conditioners. The three-level hysteresis controller reduces the variation of the switching frequency and it indicates improved performance compared to 2-level HCC. This active power filter system has been tested using MATLAB program. An adaptive hysteresis current controller has been implemented for three phase shunt active power filter. The synchronous reference frame controller has been used to extract the reference current from the distorted line current. This facilitates to improve the power quality parameters such as reactive power and harmonics due to nonlinear load. The obtained results indicate that DC-capacitor voltage and the harmonic current control can be adapted easily under non-linear load conditions. The performance of the adaptive hysteresis current controller and fixed hysteresis current controlled shunt active power filter has been verified with the simulation results. These current controllers compare the transient response and steady state performance in various conditions. FPGA based PWM Controller has been designed for three phase shunt active power filter. Thus the digital controller has been implemented in Spartan VI FPGA KIT.

References

[1] Brod D. M., and Novotny D.W.,1985, "Current Control of VSI PWM Inverters", IEEE Transactions on Industrial Applications, 21(4), pp.562-570

[2] Takeda M., 1987, "Harmonic Current Compensation With Active Filter", in IEEEIIAS Ann. Meeting, pp.808.

[3] Joseph S. Subjak., and J.S.Mequilkin.,1990, "Harmonics-Causes, Effects, Measurements, and Analysis: An Update", IEEE Trans on Industry Applications, 26(6), pp.1034-1041.

[4] Grady W.M., Samotyj M.J., and Noyola A.H., 1990, "Survey of Active Power Line Conditioning Methodologies" IEEE Trans. on Power Delivery, 5(3), pp. 1536 - 1542.

[5] Henderson R.D., and Rose, P.J., 1994, "Harmonics Effects on Power Quality and Transformers", IEEE Trans. Industrial Applications, pp.528-532.

[6] Marian P. Kaunierkowski, Maciej A.Dzieniakowslu,1994,"Review of Current Regulation Techniques For Three-phase PWM Inverters", Conference on IECON 94, 1, pp.567-575.

[7] Akagi H., "Trends in Active Powerline Conditioner", 1994, IEEE Trans. on Power Electronics, 9(3), pp. 263-268.

[8] Wu J.C., Jou H.L., 1996, "A Simplified Control Method for Single Phase Active Power Filter", IEE Proc-Electr. Power Appl, 143 (3), pp. 219-224.

[9] Bhim Singh., and Kamal AL-Haddad, 1999, "A Review of Active Filters for Power Quality Improvements", IEEE Trans. on Industrial Electronics, 46(5), pp.960-971.

[10] Barrero F., Martinez S., Yeves F. and Martinez, P.M., 2000, "Active Power Filters for Power Line Conditioning: A Critical Evaluation", IEEE Trans. on Power Delivery, 15(1), pp. 319-325.

[11] Jou H.L., Wu J,C, Chang Y.J. and Feng Y.T.,2005, "A Novel Active power Filter for Harmonic Supression", IEEE Trans.on Power Delivery, 20(2), pp.1507-1513.