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Design of Area Optimized, Low Power, High Speed Multiplier Using Optimized PDP Full Adder

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Abstract

Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is of great importance in digital signal processing as well as in the general purpose processors. Now a days, there are an increasing number of portable applications requiring small-area, low power and high throughput circuitry. The circuits with low power consumption become the major issues for the design of microprocessor and system components. The adders and multipliers are the basic elements to construct the ASIC applications. One fast approach to reduce the power dissipation of multiplier is Binary Tree Based Architecture. In BT architecture is based on the generation of all partial products of the multiplication can be done in parallel and then summing these partial products using binary tree network. This method has minimum power consumption with increasing speed of operation. The adders used in the multiplier are designed with multiplexer and four transistor based XOR adder for further power reductions. The power consumption of proposed structure is 60% lesser than array structure with CMOS transistor adder. The designed circuit is simulated with 5 micron technology with an operating voltage of 3V using Tanner ED*A*

Keywords: Multiplexer based adder, low power, Binary Tree, Multiplier architecture

1. Introduction

Low-power is the major goal for which speed and dynamic range might have to be sacrificed. High speed and high integration density are the objectives for the second application category, which has experienced a dramatic increase of heat dissipation

that is now reaching a fundamental limit. These two forces are now merging as portable equipment grows to encompass high-throughput computationally intensive products such as portable computers and cellular phones. The most efficient way to reduce the power consumption of digital circuits is to reduce the supply voltage, since the average power consumption of CMOS digital circuits is proportional to the square of the supply voltage. The resulting performance loss can be overcome for standard CMOS technologies by introducing more parallelism and to modify the process and optimize it for low supply voltage operation [2].

The objective of a good multiplier is to provide a physically compact, good speed and low power consuming chip. To save significant power consumption of a VLSI design, it is a good direction to reduce its dynamic power that is the major part of total power dissipation [14][17].

Signal processing applications typically exhibit high degrees of parallelism and are dominated by a few regular kernels of computation such as multiplication, that are responsible for a large fraction of execution time and energy. In such systems, multiplier is a fundamental arithmetic unit [9] shrinking feature sizes are responsible for increasing thermal related problems as well. The on chip temperature in current processors can vary by as much as several tens of degree from one portion of the chip to the other with the maximum temperature reaching as high as 100 degree C. The temperature gradient formed by such units can be major source of inaccuracy in delay and clock skew computations [7].

The basic multiplication principle is twofold i.e., evaluation of partial products and accumulation of the shifted partial products. It is performed by the successive additions of the columns of the shifted partial product matrix. The 'multiplier' is successfully shifted and gates the appropriate bit of the 'multiplicand'. The delayed, gated instance of the multiplicand must all be in the same column of the shifted partial product matrix. They are then added to form the product bit for the particular form. Multiplication is therefore a multi operand operation. To extend the multiplication to both signed and unsigned numbers, a convenient number system would be the representation of numbers in two's complement format.[8]

In section 2 we reviewed the various adder architecture. In section 3 deals with the proposed multiplier architecture. Section 4, Power comparison of array multiplier with proposed structure is presented. Finally, we conclude the paper in Section 5.

2. Analysis of Various Full Adder Architectures

2.1. Conventional CMOS Full Adder

The conventional adder is implemented with 28 Transistors in CMOS technology and it requires minimum of one volt supply for the proper function.

2.2. Static Energy Recovery Full (SERF) Adder

Static Energy Recovery Full (SERF) adder requires only 10 transistors to implement a full adder. Where an intermediately generated XNOR (A,B) signal is shared to generate the carry out and the sum outputs [15],[17].

2.3. Transmission Function Adder

A transmission gate, or analog switch, is an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a pMOS transistor and nMOS transistor The control gates are biased in a complementary manner so that both transistors are either on or off. The transmission function full adder which uses 16 transistors for the realization of the circuit. It occupies less area and consumes less power than Ex-or based adder.

2.4. Ex - OR and Multiplexer Based Full Adder Design

The logic approach uses only one XOR gate and two multiplexer to implement the Carry and SUM. XOR gate is the most power hungry components of the full adder cells. Therefore, the new logic approach will reduce the power consumption.

2.5. Multiplexer – Based Full Adder

In this architecture multiplexers are used to design a adder [22], As multiplexers doesn't need any supply voltage for its function, the full adder designed with multiplexer may not have the leakage problems and short circuit problems**.** The multiplexers are implemented using NMOS and PMOS pass transistors. The select line of the 2 to 1 multiplexer can be considered from any one input from the full adder. the CARRY function of full adder can be implemented by using the general equation

$$CARRY = a'bc + ab'c + abc' + abc \quad \textbf{(1)}$$

By reducing this equation we obtained

$$CARRY = a'bc + abc' + ac \quad \textbf{(2)}$$

To implement the sum and carry function in the equ 2, it requires the 6 identical multiplexers.

2.6. Proposed Multiplexer – Based 12T Full Adder

The proposed adder in this paper is designed with multiplexer. Proposed 1-bit full adder that utilizes 6 identical multiplexer, substituting each of the multiplexer with a 2-transistor circuit gives us the new MBA-12T adder, which requires a total of 12 transistors to realize the function of a full adder is shown in figure 3. The carry function of the multiplexer based adder discussed in [20] is implemented with equation 2. The input 'a' gets changed on every cycle it causes the switching of transistor at every clock cycles results in more switching power. In the proposed adder the carry function is implemented with the equation 3.

$$CARRY = ab'c + abc' + bc \quad \textbf{(3)}$$

In the proposed adder the input 'b' and 'c' are used as a select input for the multiplexer. The input 'b' gets changed in its position only for every two clock cycle and in results less switching of transistor causes the less switching power. The proposed adder in this paper is designed with multiplexer. Proposed 1-bit full adder that utilizes 6 identical multiplexer, substituting each of the multiplexer with a 2-

transistor circuit gives us the new MBA-12T adder, which requires a total of 12 transistors to realize the function of a full adder is shown in figure 1.

In addition to reduced transition activity and charging recycling capability, this circuit has no direct connections to power supply nodes and the entire signal gates are directly excited by the fresh input signals, leading to noticeable reduction in short - circuit power consumption. There are three major sources of power dissipation in a digital CMOS circuit: logic transition, short-circuit current and leakage current. The short-circuit current is defined to be the direct current passing through the supply and the ground, when both the NMOS and PMOS transistors are simultaneously active. Same short-circuit current problem as they have some internal nodes driven by signals with slow raise and/or fall times. This leads to significant (20%) short- circuit power dissipation for loaded inverters. Such problem was partially solved in SERF adders as a result of absence of connection to Vss port. In this case no direct path from supply to ground can be formed.

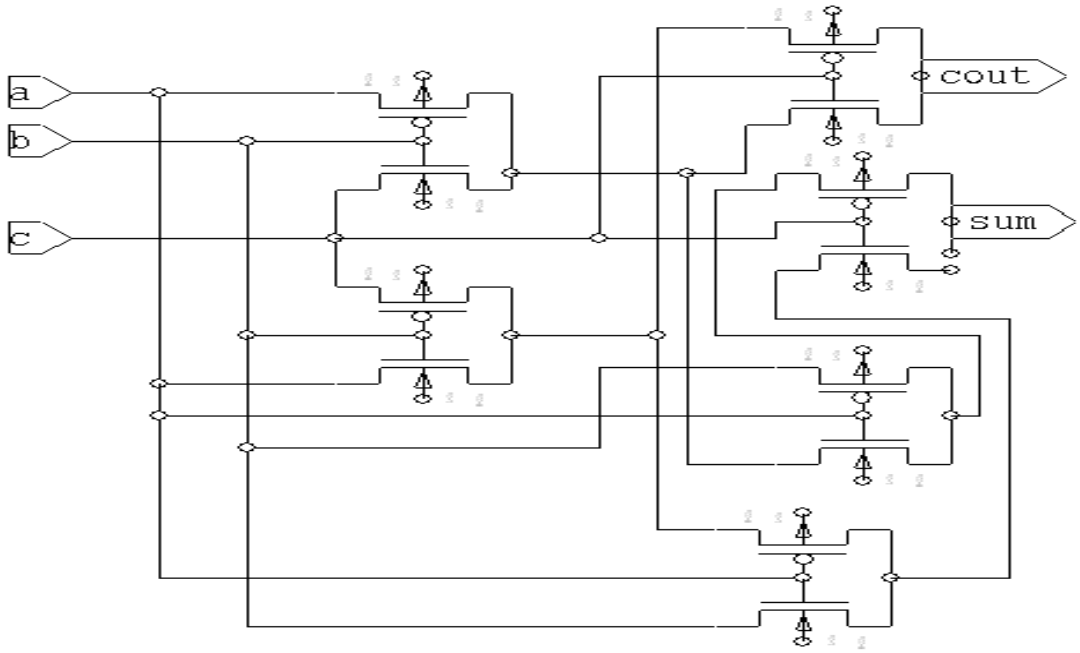


Fig.1 Proposed Multiplexer-Based 12-Transistor Circuit

The new MBA- 12T adder moves one step further and provides the best solution for the short-circuit current problem as all of its internal gate nodes are directly excited by fresh input signals. On top of that, MBA-12T does not have direct connections to Vdd or V_{ss} *port*, which can substantially reduce the probability of a direct path formation from positive voltage supply to the ground during switching.

2.7. Proposed 4T XOR Adder

XOR gates form the fundamental building block of full adders. Enhancing the performance of the XOR gates can significantly improve the performance of the adder. A survey of literature reveals a wide spectrum of different types of XOR gates that have been realized over the years. The early designs of XOR gates were based on either eight transistors or six transistors that are conventionally used in most designs. In this paper considerable emphasis has been laid on the design of four-transistor XOR gate and is shown in figure 2..

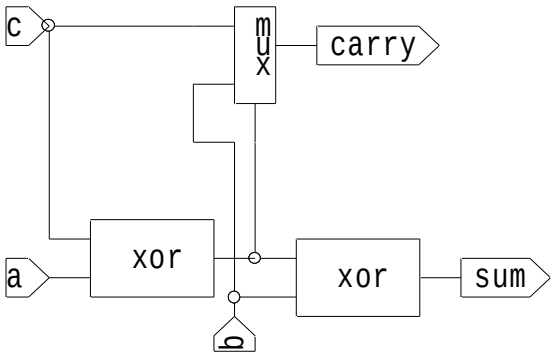


Fig.2 Proposed XOR based 10 T Adder

The various full adder structures discussed above are simulated with Tanner Spice and the dynamic power consumption of various structures are given in table 1. The proposed adder designed with multiplexer will consume less power and delay and utilized to design a multiplier. The output waveform of proposed structure is similar to other structure and it consumes less power and delay than other architecture discussed is shown in figure 3.

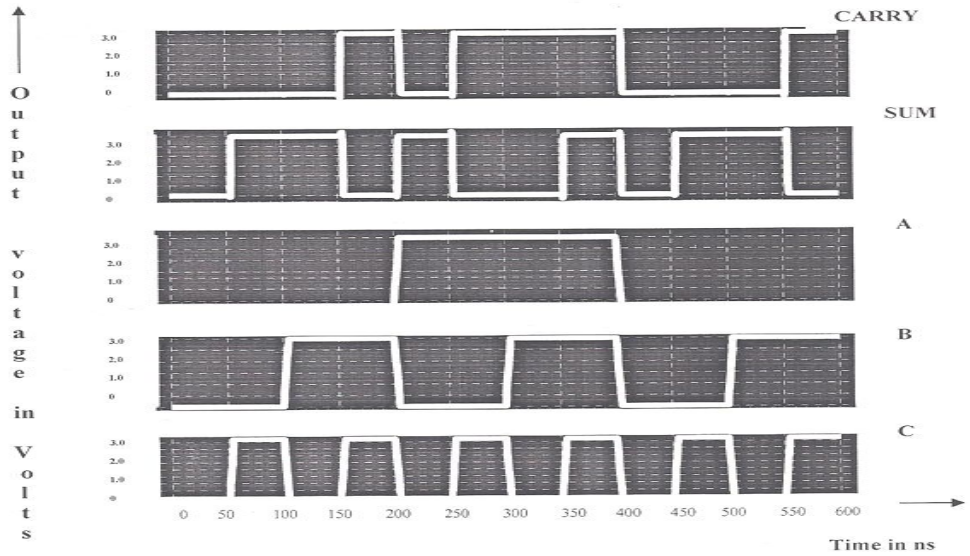


Fig. 3 Output waveform of proposed adder

Table 1: Power Comparison between the adders

S.No	Name of the adder	Avg.Power	Delay in ns	PDP(uWS)	No.of Transistor
1	CMOS adder	3.51E-05	1.2	4.21E-05	28
2	26 Transistor adder	1.22E-04	1.8	219.6 E-06	26
3	Transmission Function adder	2.85E-05	2.6	7.41E-05	16
4	SERFull adder	1.20E-05	2.5	30 E-06	10
5	XOR and MUX based adder	1.54E-05	1.2	18.48 E-06	10
6	Multiplexer based adder [18]	1.55E-05	1.8	2.79E-05	12
7	Proposed Multiplexer based 12T adder	1.39E-05	0.8	11.12 E-06	12
8	Proposed 4T XOR adder	1.52E-05	0.6	9.12E-06	10

The average power consumption of the various adder architecture is plotted in graph is shown in figure 4. The proposed adder is optimistic in power and delay and it is utilized in multiplier.

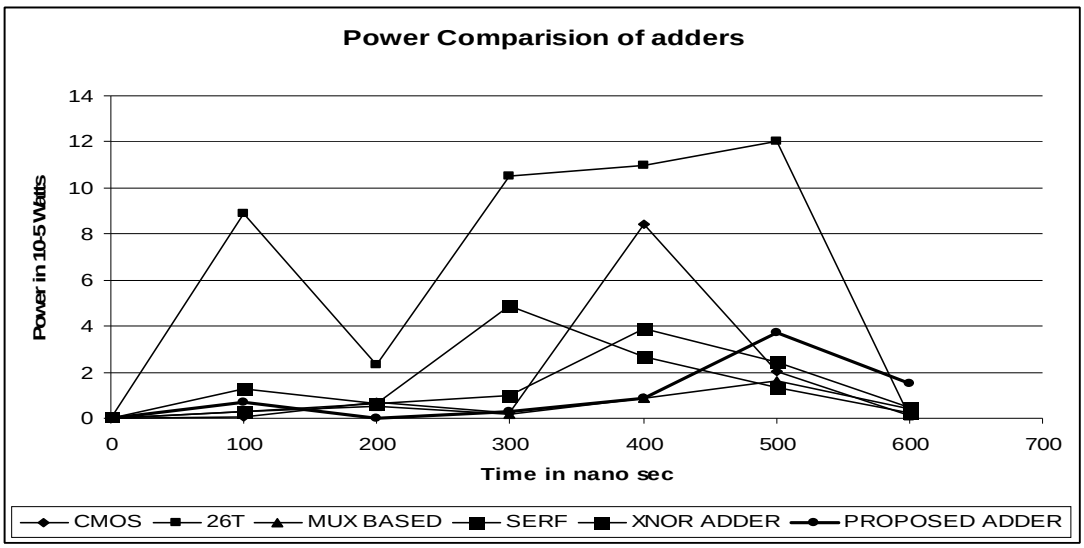


Fig. 4 Average power consumption of different adders.

3. Proposed Multiplier Architecture.

The proposed binary tree multiplier architecture is based on an algorithm consists of two concepts.

- The generation of all partial products of the multiplication can be done in parallel with a delay of d.
- Speedup of adding these partial products will take $\log_2(n)$ steps

The features of the new multiplier architecture as compared to the other architectures are as follows:

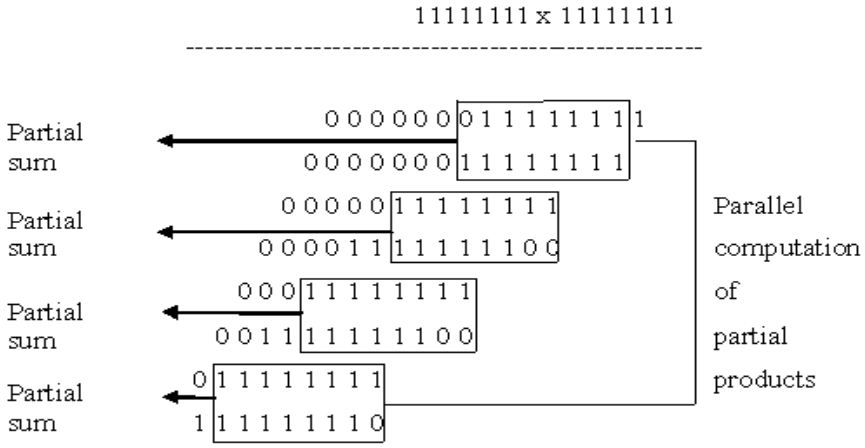
- The n-bit multiplication time is proportional to $\log_2(n)$ and the physical layout has a good repeatability.
- All the partial products are generated in one step.

The multiplicand contains zero are eliminated in [8] to reduce the power consumption. The parallelism in generating the partial product is realized by ANDing the first (LSB) of the multiplier with the multiplicand bits[18],[21]. The second partial product is achieved by ANDing the second multiplier bit with the multiplicand bits proceeded by a zero. The third partial product is achieved by ANDing the third multiplier with the multiplicand bits preceded by double zeros and so on…

For (n x n) bits there will be a n partial product. These partial products can be added in parallel. Each two adjacent partial product will be added together through n-bit adder. This will generate the first level of computation with n/2 partial sums. These partial sums are added again in the same fashion creating a second level of computation with n/8 new (n-1) of n-bit adders in the form of binary tree network and it is shown in figure 8. The number of levels needed to create this binary network is $\log_2(n)$. Figure.5 shows the basic architecture for the new multiplier structure for (8 x 8) bit binary numbers. The proposed new multiplier architecture can be constructed by a seven 8-bit full adder and one 1-bit full adder using binary tree topology.

3.1. Binary Tree Topology

For the following example, multiplying 8 bit-number can be performed as follows:



For this example, there are 8 partial products are generated, each 4 partial products

are added (indicated by dot lines) creating the first level of computation which have 4 partial sums. These four partial sums are fed to the second level of adder, resulting in the formation of the final product Since this architecture requires (n-1) of n-bit adders, it needs a total of n(n-1) full adder cells. So, the worst case delay of this architecture can be computed as follow:

$$d' + nd [\log_2 (n)]$$

Where,

d = Propagation delays of a full adder &
d' = Propagation delays 2- input AND date

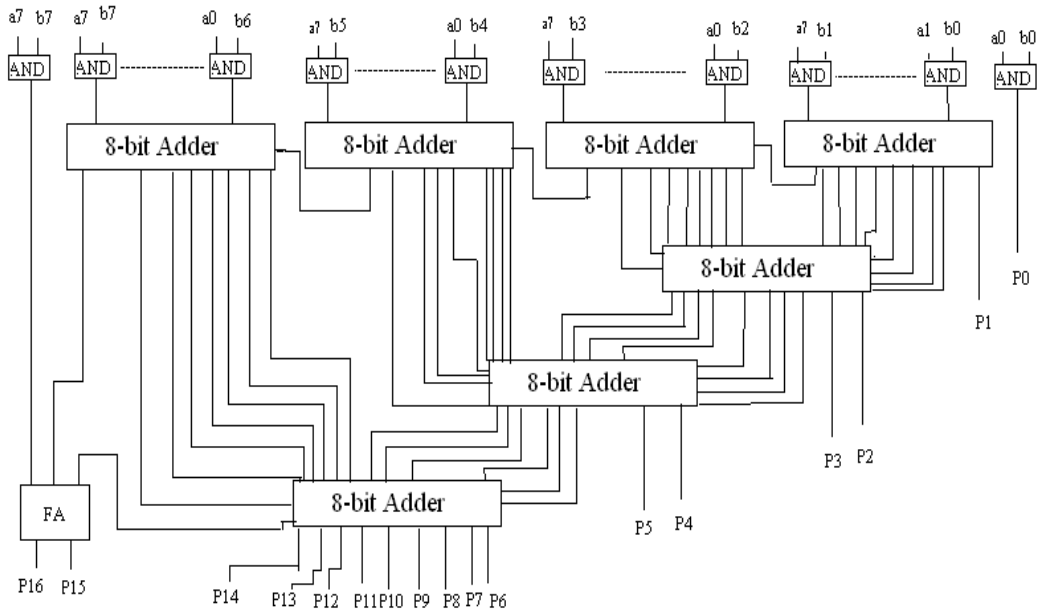


Fig. 5 Binary Tree multiplier architecture for 8 bit binary numbers

4. Results

The Binary Tree (8X8) bit multiplier architecture has been implemented using a optimized power and delay XOR and Multiplexer based adder. All the combination of 8 bit inputs is applied and the power consumption is shown in figure 6. The same input combination is forced to the array multiplier with conventional adder and the proposed multiplier structure with proposed adder and proposed multiplier with conventional CMOS adder. The average power consumption for different multiplier with different adder structure is shown in table 2.

P =A*B ; A=00000001; B=[00000000 to 11111111]

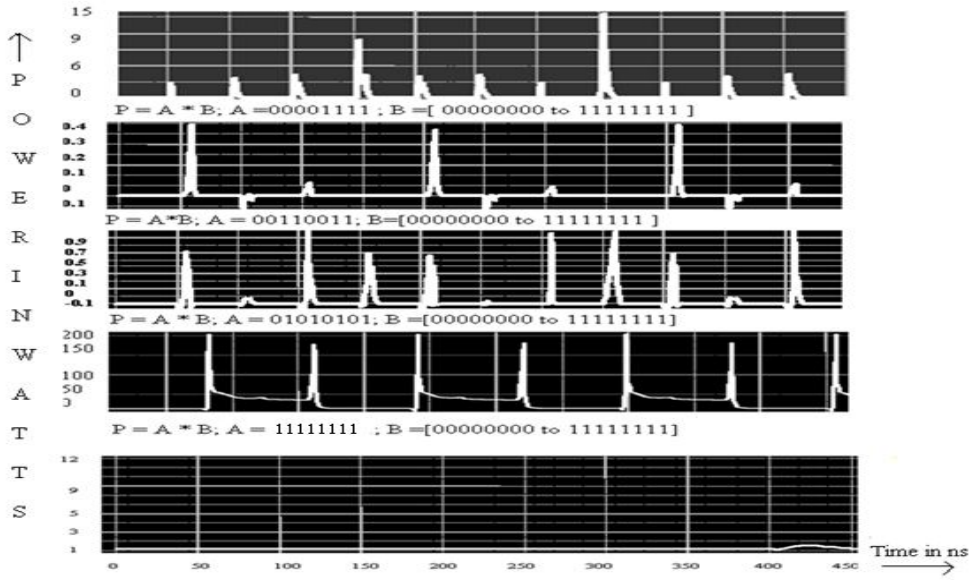


Fig 6 Power Consumption of proposed multiplier

Table 2: Performance Comparison of Different Multipliers with various adder architecture

Input (A xB)	Array Multiplier with CMOS Adder	BT multiplier with CMOS Adder (Watts)	Array multiplier with 4T XOR adder structure (Watts)	BT multiplier with MUX 12-T adder (Watts)	BT multiplier with 4T XOR adder (Watts)
00000001× (00000000 to 11111111)	9.86 E-02	9.42E-02	3.76E-02	4.34E-04	5.28E-05
00110011× (00000000 to11111111)	1.36 E-01	1.22E-01	4.44E-02	1.92E-02	4.27E-02
00001111× (00000000 to11111111)	1.30E-01	1.09E-01	4.46E-02	1.89E-02	4.56E-03
01010101× (00000000 to11111111)	1.01E-01	1.11E-01	3.35E-02	2.79-2	4.59E-02
11111111× (00000000 to11111111)	9.54E-01	9.42E-01	5.22E-02	4.67E-02	3.02E-02
Average power in Watts	1.4 E-01	1.12E-01	4.42E-02	1.34E-02	6.55E-03
Delay (nS)	60	40	44	28	15
PDP (WS)	84 E-10	44 E-10	20 E-10	37 E-10	9.8 E-10
No.of Transistor	1596	1724	628	812	698

The comparison of power consumption of different multipliers with different adder structures is shown in figure 7. From the graph it is observed that, the binary tree

multiplier with proposed adder structure will consume less power to produce the output. The PDP and Number of transistor required for implementation of multipliers is shown in figure 8 and figure 9.

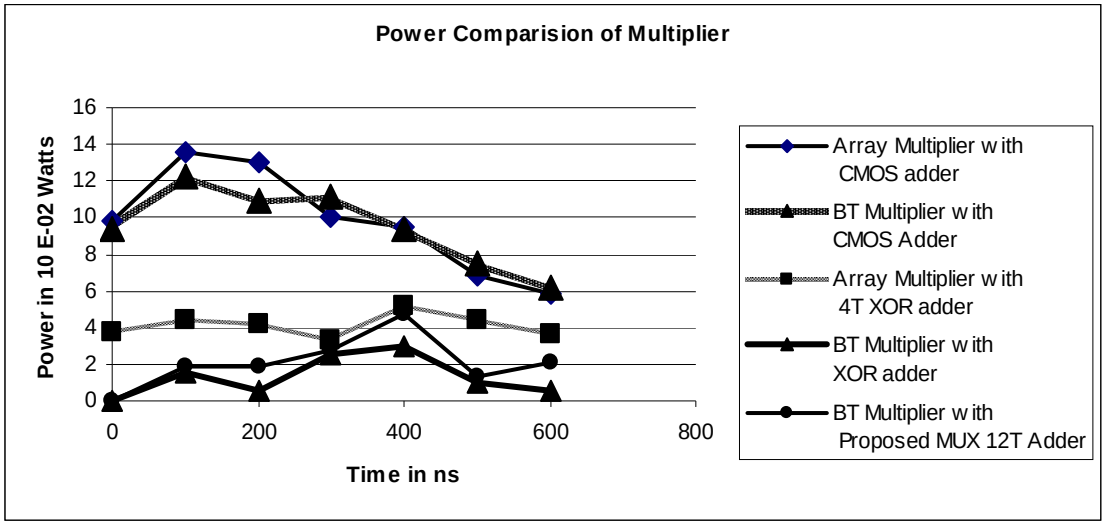


Fig. 7 Comparison of Power consumption of different Multiplier Structures

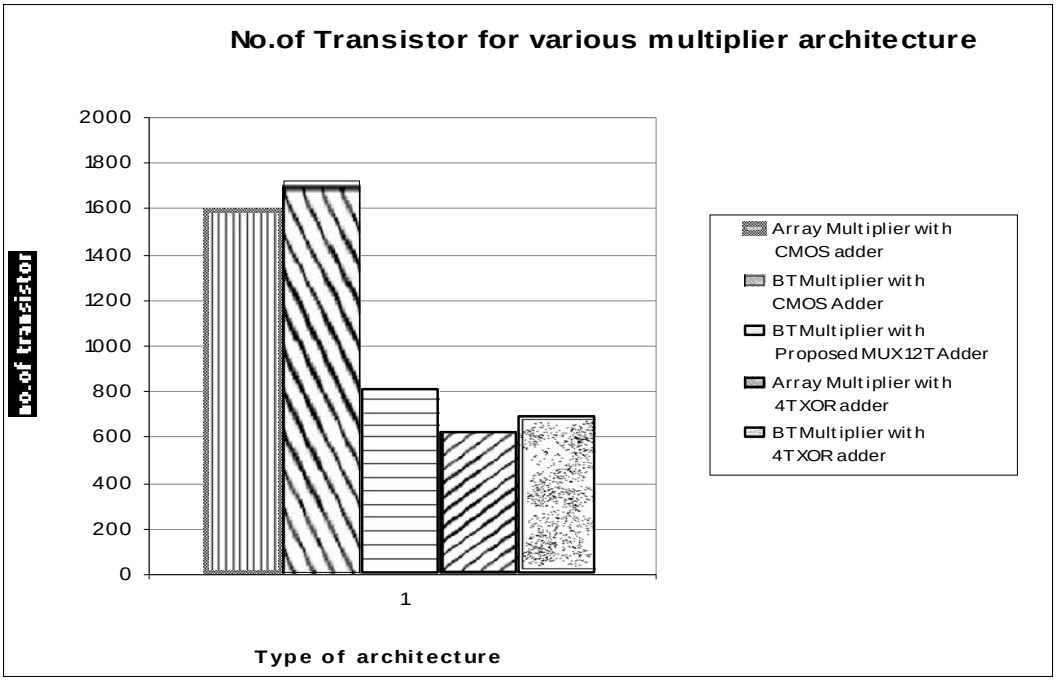


Fig.8 No.of Transistor for various multiplier Architecture

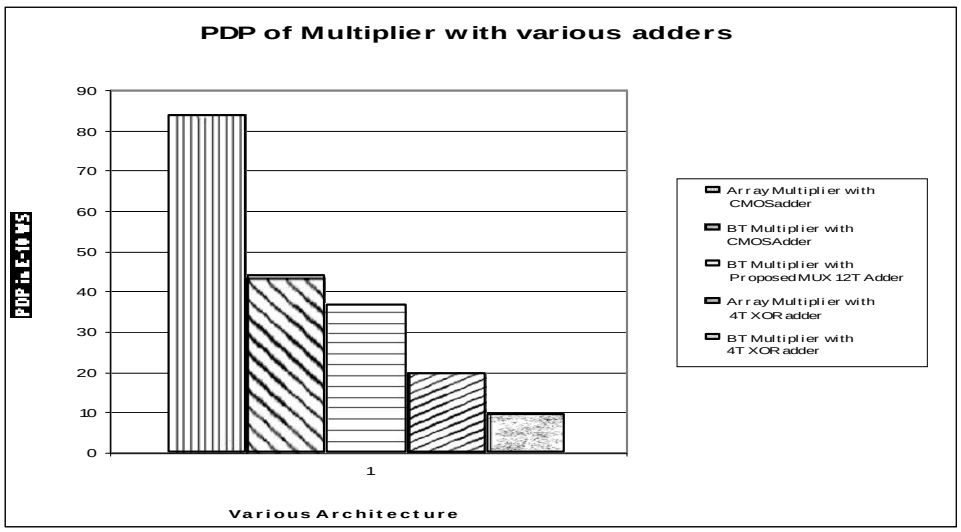


Fig.9 PDP of various multiplier Architecture

5. Conclusion

In this paper, we proposed a Binary Tree based multiplier architecture and new multiplexer based adder and 4T MUX based adder for designing a multiplier. In BT structure parallel approach is used to generate the partial products and there sums. A novel low-power, low delay XOR based 10 transistor adder and multiplexer-based 12T full adder is presented using 6 identical multiplexers. It has very low short-circuit current and is suitable for design a larger low power high performance VLSI systems. The proposed multiplier architecture exhibit 50% less PDP with 7 % rise in transistor and is suitable for high speed applications.

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