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Speed Control of Induction Motor using VHDL Implementation of PWM Technique

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Abstract:

This paper aims for design and implementation of a Variable-Voltage Variable-Frequency (VVVF) Controller based on Pulse Width Modulation (PWM) Technique for a single phase and three Phase Induction Motor using VHDL. Variable-Voltage Variable-Frequency (VVVF) technique is used extensively in the industry as it provides the accuracy required. Voltage/ frequency (v/f) controlled motors falls under the category of Variable Voltage Variable Frequency (VVVF) drives. To maintain maximum torque under given working condition, the flux in the machine must be maintained constant. The ratio of voltage to frequency must be held constant. To vary the fundamental component (voltage and frequency) of the inverter, the Modulation Index of the carrier signal has to be changed. The speed at rated supply frequency is normally used as the base speed. At frequencies below the base speed, the supply magnitude needs to be reduced so as to maintain a constant v/f ratio. The VHDL based controller is used to generate PWM pulses based on the frequency input, that are used to control the inverter output . The VVVF output of the inverter can be used as supply to a three phase induction motor and thereby speed of the motor can be controlled.

Keywords: PWM Technique, Speed Control

I. Introduction

The Motor Control industry is a strong aggressive sector. Each industry to remain competitive, must reduce costs but also has to answer to power consumption reduction and EMI radiation reduction issues imposed by governments and power plant lobbies. The results of these constraining factors are the need of enhanced algorithms. PSoc technology allows achieving both, a high level of performance as

well as a system cost reduction. The AC induction motor is the workhorse of industrial and residential motor applications due to its simple construction and durability. These motors have no brushes to wear out or magnets to add to the cost. The rotor assembly is a simple steel cage. ACIM's are designed to operate at a constant input voltage and frequency; we can effectively control an ACIM in an close loop speed application if the frequency of the motor input voltage is varied. If the motor is not mechanically overloaded, the motor will operate at a speed that is roughly proportional to the input frequency. As you decrease the frequency of the drive voltage, you also need to decrease the amplitude by a proportional amount. Otherwise, the motor will consume excessive current at low input frequencies. This control method is called "Volts-Hertz control". In recent years, Field Programmable Gate Arrays have drawn much attention due to its short design cycle, low cost and high flexibility in terms of programmability. The Field Programmable Gate Arrays (FPGAs) offer significant advantages over microprocessors and DSPs for high performance, low volume applications, particularly for applications that can exploit customized bit-widths and massive instruction-level parallelism[3][6]. The innovative development of FPGAs whose configuration could be re-programmed an unlimited number of times spurred the invention of a new field in which many different hardware algorithms could execute, in turn, on single device, just as many different software algorithms can run on a conventional processor [6]. When comparing the dynamic performance, control capabilities and concurrency in PWM controlled Power Converters, FPGA based digital techniques are better than DSPs [6].

II. SPEED CONTROL OF INDUCTION MOTOR

The synchronous speed of the induction motor is given by:

$$Ns = 120f/p \quad (1)$$

where 'f' is frequency and 'p' is number of poles. The running speed of the induction motor is given by the equation:

$$Nr = Ns(1 - s) \quad (2)$$

where 's' is slip of the induction motor expressed in terms of percentage. The speed control can be performed using open loop algorithms or closed loop algorithms. The most commonly used open loop algorithm is Voltage/ frequency control method. Open loop control of induction motor is used extensively in the industry as it provides the accuracy required at minimal cost. Voltage/ frequency controlled motors fall under the category of Variable Voltage Variable Frequency drives which are fed by an inverter.

There are no. of types of inverters. But pulse width modulated inverters are generally used to control the speed of induction motor. In this method fixed dc input voltage is supplied to inverter and output voltage of the Inverter can be controlled by controlling or modifying switching current, or in case of Power Switches, by controlling or modifying Gate current. This control is achieved by PWM control. This method is popularly called as Pulse Width Modulation (PWM) method.

The advantages of the PWM control are:

(1) PWM control is very simple and require very less hardware. So they are also cost

effective. (2) They can easily implemented using Microcontroller, DSP or FPGA. The major disadvantage of PWM control is that power switches associated with PWM switching are very costly as their response time should be very fast. They are prone to environmental noise and temperature changes . Hence they are not suitable where these factors are prominent. PWM waves are actually pulses of constant amplitude and varying pulse widths. This width can be varied by different modulation schemes. Which are : (a) Analog techniques (b) Digital techniques In the most implementation Digital Pulse Width Modulation technique is used. Many digital techniques are based on the use of counter and comparator based design. These digital techniques are easier to implement than analog techniques. Also they are immune to environmental noise and temperature change. Also they do not suffer component variation and switching losses.. For sophisticated control schemes it is desirable to use Digital PWM modulation scheme.

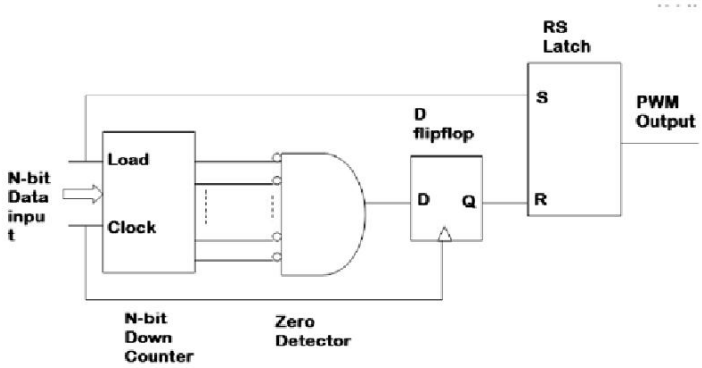

Fig. 1 Basic Implementation of counter based Digital PWM

III. THE PROPOSED SYSTEM

The system block diagram with various modules is shown in Figure 2. The FPGA controller produces the PWM pulses which are at a voltage of 3.3V. The voltage shifting from 3.3V to 12V requires a voltage-level shifting circuit. The voltage level shifted pulses will be fed to the three phase inverter to convert the DC supply to a three phase supply which is in turn fed to the induction motor. A controller was designed using VHDL. The VHDL code developed to generate a three phase sinusoidal pulse width modulated signal.

Block diagram of system

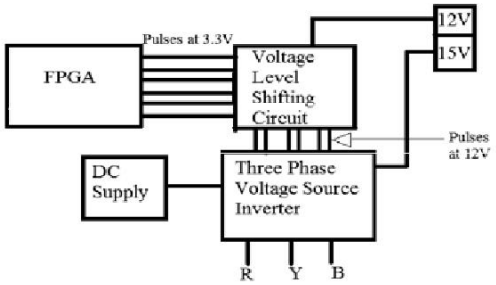

Fig. 2 System Block Diagram

HARDWARE AND SOFTWARE DEVELOPMENT FOR PROPOSED SYSTEM

Power circuit details

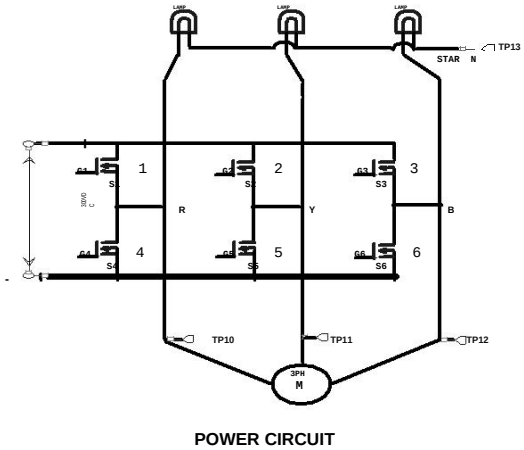

Fig.3 Power circuit.

The power ckt have used six MOSFET Power transistors in bridge configuration. It is powered by 300 V DC supply. The dummy load & motor load is connected at the remaining points of bridge in parallel. The six transistors conduct in sequence 1 - 6 -2 - 4 - 3 - 5 & generate the AC output in Quasi Square or Two Step wave format . The DC voltage is applied to the MOSFET Bridge through fuse.

Isolation and driver section:

The circuit consists of OP–AMP buffer for OPTO – ISOLATOR and the pre driver stages. The signals for the power transistors are coupled to the transistors through these isolator drivers. The pre drivers use separate supplies for each transistor signal. It gives out 5 V, 100 mA pulses for driving the MOSFET. The driver circuit consists MOSFET driver IC TLP250 (opto-isolator) and other additional components such as diodes, capacitors etc. The pulses coming from the FPGA are fed to the MOSFET driver The TLP250 is high voltage, high-speed power MOSFET drivers with independent high and low side referenced output channels. The output of the TLP250 is given to the MOSFET.

Protection circuit :

A protection circuit is provided to avoid the damage to the MOSFET Bridge due to various fault conditions like excessive over- under voltage variation, excessive load variation etc. In a comparator LM 339 three feedback signals are taken from over-under voltage sensing, R-sense resistance which is connected in series of the DC link voltage. The second i/p comes from the CT which is provided into the o/p phases both the i/p voltage compares with a preset reference. These feedback signals are compared with the reference voltages (variable according to the need of application). Whenever any of the fault conditions exceeds the set limit O/P of the comparator changes from

high to low cause the dc link supply and the control signals break. After the fault condition is removed user can continue the operation by pressing the reset push button. The comparator cuts the supply of the main relay, thus saving the load & power devices from over current .Shut Down LED indicated the over current cut out.

Control circuit details

The speed of motor is controlled by varying TON & TOFF. The count is already stored by the counter. The latched (stored) count is read. Then the count is adjusted for the output. Thus the TON period is adjusted as per the requirement. The controller card consists of Processing Unit and related circuitry. When the frequency of the pulses applied to the stator increases the speed of the induction motor increases.

Software Development:

The project is implemented using Xilinx chip (FPGA chip), which is a large capacity chip . So that future modifications and developments can also be incorporated .The code tends to be secret. Since once it is coded in FPGA chip, it is not readable . The software used in the project -

1) Modelsim for simulation

2) Xilinx's CPLD XC9572 PC-84-15 for design entry and downloading to the kit .

Along with the power circuitry on also requires VLSI hardware (i.e. the downloading kit and FPGA chip) in which one can download the VHDL code.

IV. RESULTS

Simulation Results

The architecture has been implemented in VHDL and implementation is carried out using Xilinx device .So results of implementation in VHDL are as follows.

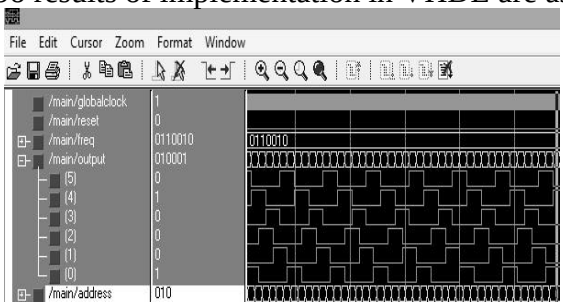

Fig.4 PWM module output

Fig. 4 shows the Pulse Width Modulated output signal for MOSFETs.

SYNTHESIS REPORT OF THE CONTROLLER

All the modules are integrated and synthesized using Xilinx project navigator and support tools. The synthesized VHDL source code is placed and routed. Finally, a bit file is created. This bit file is fused into the Xilinx5.1 interfaced with the input and output device.

Device utilization summary for the Pulse width
Modulation: Selected Device: Xilinx's CPLD XC9572 PC-84-15
Design Statistics
IOs : 15
Cell Usage :
BELS : 158
AND2 : 57
INV : 91
OR2 : 9
XOR2 : 1
FlipFlops /Latches : 26
FD : 26
IO Buffers : 15
IBUF : 9
OBUF : 6
Total memory usage is 72480 kilobytes

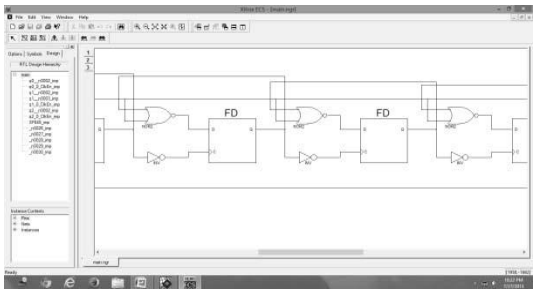

Fig.5 RTL schematic diagram

PWM Generator were synthesized using Xilinx ISE software. Device Utilization and No of Logic Blocks of each topology were noted down and compared with each other. It was seen that number of logic blocks used in FPGA for design of PWM Generator is minimum in case of Counter based PWM Generator.

PWM pulses from control circuit: Depending on input Frequency output signal's width changes and so that speed of the motor also changes. Output waveforms on DSO for gate pulses of MOSFETS from hardware.

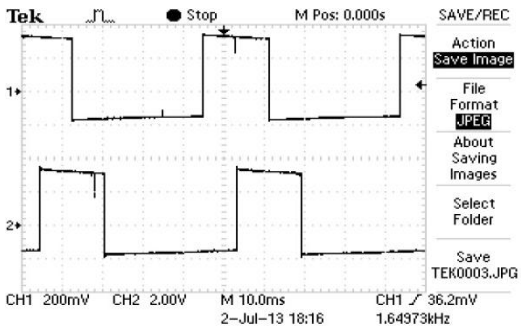

Fig.6 Gate pulses for Q1 and Q6

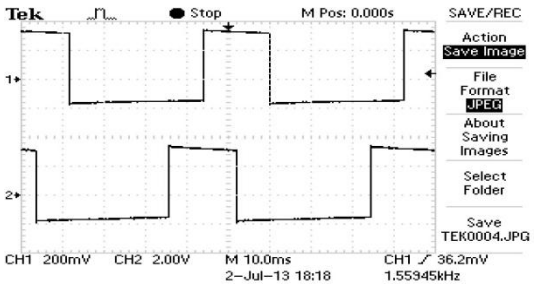

Fig.7 Gate pulses for Q2 and Q4

The output voltage waveform of the inverter circuit is shown in Fig. 8. and motor load is connected to inverter. The pulse width modulated (PWM) inverter for variable speed drive of induction motor circuit drives small induction motors up to about 0.5 horse power, 440 volts . The frequency may be adjusted from 20 Hz to 60 Hz. So, the motor speed can be varied from 505 rpm to 1640 rpm.

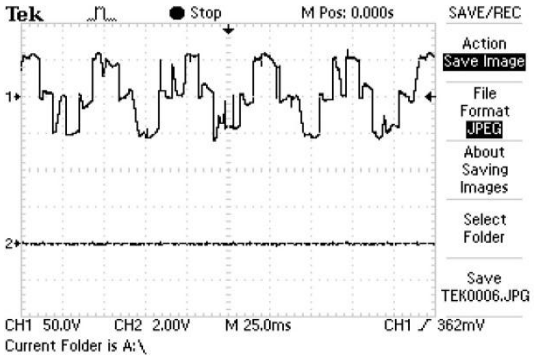

Fig.8 output line (V_{RY})voltage Waveforms of inverter for motor load

Laboratory Test Arrangement

Performance test and results of variable frequency drive of three-phase induction motor are expressed as follows:

Supply voltage	230 volts
Supply frequency	50 Hz
Motor rating	0.5 hp
Number of poles	4
Normal speed	1440 rpm
Maximum speed	1640 rpm
Minimum speed	505 rpm

Hardware Results

Readings are taken from hardware. Fig 8 shows that the speed increases with increase in voltage.

Speed v/s voltage

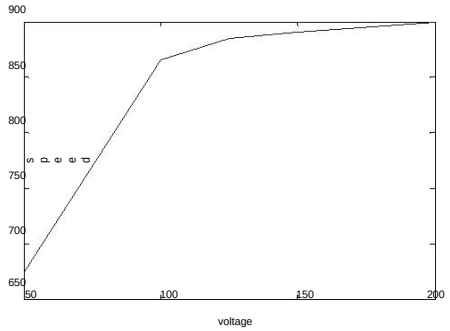

Fig. 9 Graph between voltage and speed

Speed v/s frequency: Fig.10 indicate that if we increase the frequency the speed also increases.

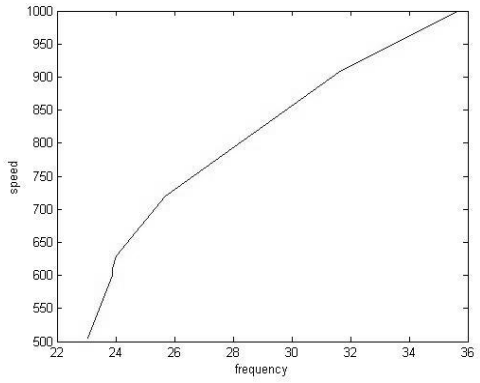

Fig.10 Graph between frequency and speed

Photo of Laboratory arrangement-

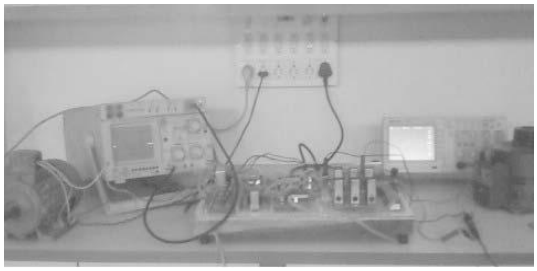

Fig.11 Photo of Laboratory arrangement

V. CONCLUSION

In this three phase inverter system with the VLSI technology various advantages such as ease in manufacturing, simple design methods are possible. VLSI chip (FPGA) has the advantages of micro controller and discrete design both. In this system output frequency can be changed from 20 to 100 Hz and thus the system can be universally used. FPGAs can be programmed number of times so as to have flexibility to change

the design during the design process also, just by changing the code in process the design entry through VHDL. This device can be reconfigured for various types of outputs. Various Reports (Synthesis, Map, Place & Route, and Timing) are generated. This reports gives the systematic view and density of IC used (FPGA) along with the delay and other timing constraints.

The performances of the proposed method have been experimentally tested for different value of speed of three phase induction motor from 500 rpm to 1500 rpm for different values of frequency and voltage. The experimental results show the effectiveness of the proposed method.

Future scope:

There are certain features that can be added in this system. Automatic Speed control of Induction motor can be obtained by using sensor and feedback network.

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