

## **Design and Analysis of Double Gate MOSFET Devices using High-k Dielectric**

**Asha Balhara\* and Divya Punia**

*Department of E.C.E., B.P.S. Women University, Khanpur Kalan, Sonapat, India.  
\*E-mail id: ashabalhara89@gmail.com*

### **Abstract**

Double gate MOSFET is one of the most promising and leading contender for Nano regime devices. In this paper an n-channel symmetric Double-Gate MOSFET using high-k ( $\text{TiO}_2$ ) dielectric with 80nm gate length is designed and simulated to study its electrical characteristics. ATHENA and ATLAS simulation tools from SILVACO are used in simulating electrical performance and analyzing the effectiveness of double gate MOSFET. High-k gate technology is emerging as a strong alternative for replacing the conventional  $\text{SiO}_2$  dielectrics gates in scaled MOSFETs for both high performance and low power applications. High-k oxides offer a solution to leakage problems that occur as gate oxide thickness' are scaled down. Non-ideal effect of a MOSFET design such as short channel effects are investigated. The most common effect that generally occurs in the short channel MOSFETs are channel modulation, drain induced barrier lowering (DIBL). It is observed in the results that the device engineering would play an important role in optimizing the device parameters.

**Keywords-** MOSFET-metal oxide semiconductor field effect transistor; DG-MOSFET-double-gate MOSFET; SG-MOSFET-single gate MOSFET; SCE-short channel effects; High-k; DIBL-drain induced barrier lowering;  $\text{TiO}_2$ .

### **Introduction**

Double-gate (DG) metal oxide semiconductor field effect transistor (MOSFET) and related multiple-gate device architectures are nowadays widely identified as one of the most promising solutions for Nanoscale integration [7]. With one extra gate, the gate to channel coupling is doubled resulting in good reduction of SCE's [5]. These devices present an excellent  $I_{\text{on}}/I_{\text{off}}$  trade off, very good control of short-channel effects and potentially higher channel conductivity [7] as compared to planar

MOSFET devices with a single gate. When the gate length becomes comparable of depletion region then short channel effects are seen but in DG-MOSFET we are able to reduce these effects. Because of having two gates in DG-MOSFET both gates control the channel from both sides and have better electrostatic control over the channel. So we can perform more scaling of gate length. Due to better control on short channel effects DG-MOSFET is better alternative of conventional bulk MOSFET and it has higher current density, higher sub-threshold swing at low supply voltages. Thus we are able to maintain the device performance in term of higher current density and low leakage by using DG-MOSFET [5].

In recent times DGMOSFET device structures have drawn more attention of the researchers due to their inherent capability of suppressing the short channel effects. Due to two-channel formation in symmetrical DGMOSFET, it shows steep sub-threshold swing, high drive current and transconductance [5].

In order to prevent direct gate tunneling in very thin oxides envisaged for the end-of-the roadmap nodes, the  $\text{SiO}_2$  is replaced by alternative materials with higher permittivity and greater physical thickness. However, the introduction of these high-k dielectrics poses several problems, such as bi-dimensional electrostatic effects which may have a dramatic impact on the device performances when the gate dielectric thickness becomes comparable to the device gate length [7].

In this paper section II contains a description about High-k dielectric ( $\text{TiO}_2$ ) while section III gives a brief introduction of Double-gate MOSFET structure. Section IV would describe the design and simulation of N-channel DGMOSFET device with all the results and analysis discussed in section V.

## HIGH-k DIELECTRIC MATERIALS

Using an insulator with higher dielectric constant is one of the solutions to continue scaling in nanometer regime with suppressing the SCEs. The alternative insulator should have the following properties [2] : (i) chemical and electrical stability on silicon, (ii) uniform oxide thickness during fabrication, (iii) high breakdown voltage, (iv) thermal stability up to  $1000^\circ\text{C}$ , (v) pinhole free and negligible defects, (vi) low charge trapping and ionic impurities, (vii) high life time under normal operating conditions, (viii) low interface state density for high carrier mobility, (ix) small gate-leakage current (x) low hot-carrier degradation, (xi) low diffusivity of boron and phosphorous at typical processing conditions. Some of these properties depend on the material as well as on the processing technology. At first Campbell *et al.* introduced  $\text{TiO}_2$  as the potential high-k gate dielectric [2]. Later various research groups work on the feasibility of other alternative high-k dielectric (e.g.  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{HfO}_2$ ,  $\text{ZrSi}_x\text{O}_y$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{Yb}_2\text{O}_3$ ) for submicron MOSFET. The various dielectric materials are shown with their properties in table1. All these high-k materials have some practical limitations [2]. In this paper study is laid upon using titanium oxide as high-k dielectric for the DGMOSFET structure. So, Titanium oxide ( $\text{TiO}_2$ ) is briefly discussed below with some of its advantages.

**Table 1 High-k dielectric materials and their properties [2].**

Gate dielectric Material	Dielectric constant (k)	Energy bandgap Eg (eV)	Conduction band offset ΔEc (eV)	Valence band offset ΔEv (eV)
SiO <sub>2</sub>	3.9	9	3.5	4.4
Al <sub>2</sub> O <sub>3</sub>	8	8.8	3	4.7
TiO <sub>2</sub>	80	3.5	1.1	1.3
ZrO <sub>2</sub>	25	5.8	1.4	3.3
HfO <sub>2</sub>	25	5.8	1.4	3.3
Ta <sub>2</sub> O <sub>5</sub>	25	6	1.5	3.4
Y <sub>2</sub> O <sub>3</sub>	13	6	2.3	2.6
Yb <sub>2</sub> O <sub>3</sub>	27	4.3	2.3	0.9

**Titanium Dioxide (TiO<sub>2</sub>) as gate dielectric.**

TiO<sub>2</sub> has been used as an alternative gate dielectric material for deep submicron MOSFET’s earlier in 1995[2].

Advantages: The dielectric constant of TiO<sub>2</sub> is 80. The bandgap of the material is 3.5eV for amorphous films and 3.2eV for crystalline films. These band gaps are good for semiconductor but higher bandgap is required to act as an effective insulator [2].

The TiO<sub>2</sub> has low energy band offset with respect to Si. TiO<sub>2</sub> has EOT of less than 10Å. Transistors made with TiO<sub>2</sub> shows near ideal behavior but they have challenges with mobility. It has been shown that the low field effective mobility is approximately 160cm<sup>2</sup>/V-s, which is about a three order lower than the mobility in SiO<sub>2</sub> based MOSFET’s. This mobility reduction is due to interface trap state and surface roughness at TiO<sub>2</sub>/Si interface. The electron traps in TiO<sub>2</sub> is due to oxygen vacancy. An empirical relationship between the effective mobility and the interface state density [2] which is given by equation 1,

$$\frac{\mu}{\mu_0} = \frac{1}{1+\alpha D_{it}} \dots\dots\dots (1)$$

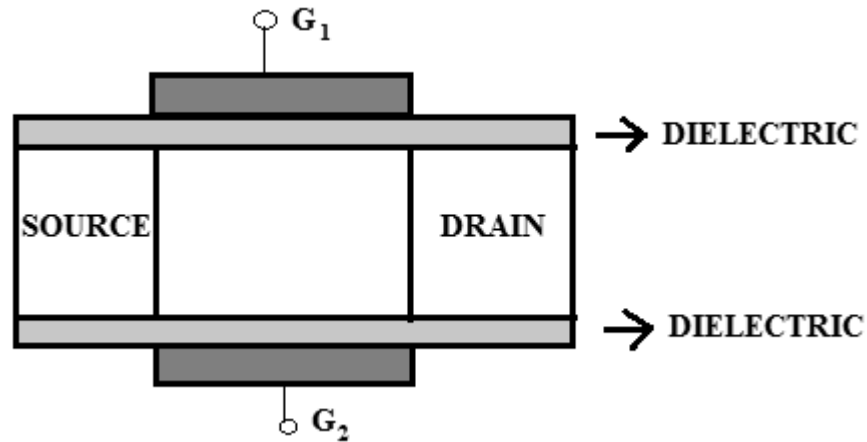
where D<sub>it</sub> is the concentration of charged states at the bias condition and α is a constant. So the effective mobility is inversely related with D<sub>it</sub>[2].

In Si/SiO<sub>2</sub> interface bond strain causes fixed charge which is about 0.1% of the interface atoms (10<sup>10</sup>-10<sup>11</sup>cm<sup>2</sup>). So for strained-Si/TiO<sub>2</sub> leakage occurs from these defects as well as from low conduction band discontinuity. Therefore, ultra-thin SiO<sub>2</sub> can be incorporated between TiO<sub>2</sub> and strained-Si layer to reduce the defect states at the interface. Therefore if TiO<sub>2</sub> is grown on (100) Si substrate D<sub>it</sub> decreases and the mobility increase [2].

Mobility can also be increased by growing TiO<sub>2</sub> gate dielectric stack on Si substrate. The device speed can be improved by 20-80% at a constant gate length by using high mobility strained-Si at the channel region. TiO<sub>2</sub> reduces gate leakage and Si enhances the device speed. Hence TiO<sub>2</sub> is our choice of high-k dielectric gate material [2].

### DOUBLE-GATE MOSFET STRUCTURE

In DG-MOSFET structure we use two gates namely top gate ( $G_1$ ) and bottom gate ( $G_2$ ). The intimate coupling between the gates and the channel makes DG MOSFET technology the most scalable of all MOSFET designs. The DG-MOSFET is electrostatically superior to a single-gate MOSFET because two gates are used to control the channel from both sides. This allows additional gate length scaling by nearly a factor of two. The two gates together control roughly twice as much current as a single gate, resulting in stronger switching signals [1]. Due to double gate structure, gate to channel coupling gets doubled and hence SCE's can be suppressed easily [5].



**Figure 1: Double-gate MOSFET structure using high-k dielectric.**

Figure 1 shows a general structure of a double gate MOSFETs. Here we are using polysilicon gate technology and high-k dielectric ( $\text{TiO}_2$ ) as gate oxide to suppress the short channel effects.

#### ***Types of DG-MOSFET***

Depending upon the way the gate voltages are applied, DG-MOSFETs may be categorized as following [5]:

#### ***Symmetric DG-MOSFET***

A DG-MOSFET is said to be symmetric when both gates have the same work function and a single input voltage is applied to both gates [4].

#### ***Asymmetric DG-MOSFET***

An asymmetric DG-MOSFET either has synchronized but different input voltages to both of the identical gates, or has the same input voltage to two gates but gates having different work functions [5].

The name of “symmetric” and “asymmetric” essentially depicts presence or absence of symmetry of the electric field inside the channel of the DG-MOSFET [5].

**Design & Simulation**

In this work we had designed an n-channel polysilicon gate symmetric DG-MOSFET with 80nm gate length on ATHENA process simulator considering the standard Silicon Integrated chip processing technology and its electrical performance is characterized using ATLAS device simulator. TiO<sub>2</sub> is used as gate oxide material and spacers are also used on both sides to reduce fringing field effect.

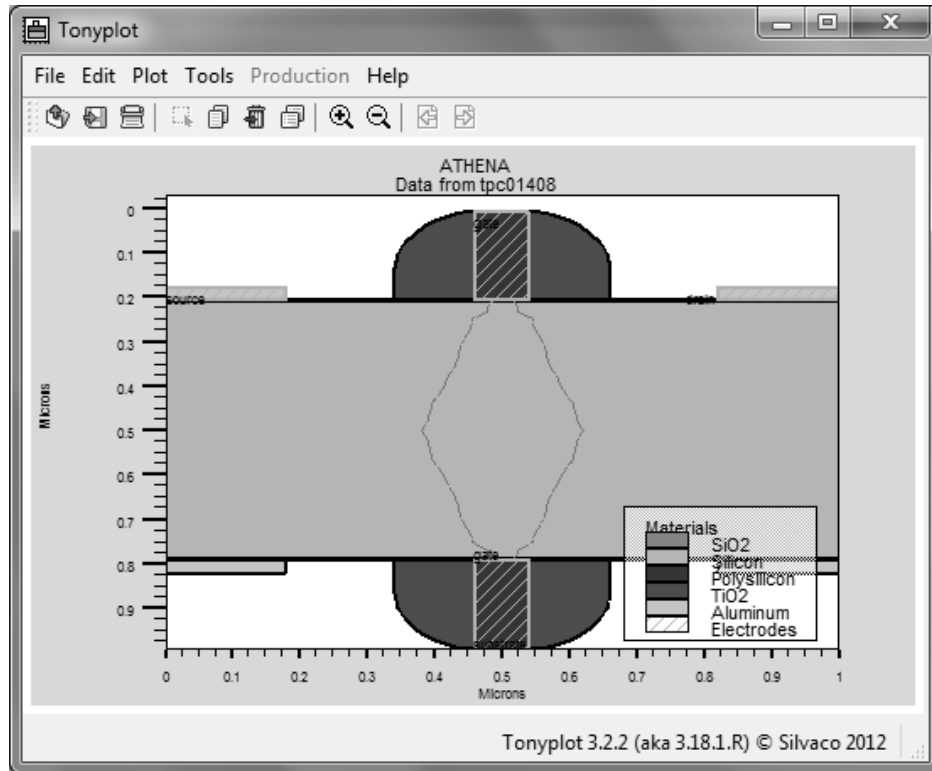
The specifications of the Silicon substrate considered for the design are p-type Boron doped substrate with doping concentration of  $1 \times 10^{18}$  atoms cm<sup>-3</sup> and <100> orientation. The design structure of DGNMOSFET using TiO<sub>2</sub> gate dielectric with Polysilicon gate is considered to explore the advantages of TiO<sub>2</sub> over SiO<sub>2</sub> dielectric. The simulated structure, which are based on fully scaled 80 nm gate length MOSFET's proposed in the ITRS, have gate length of 80 nm, with effective oxide thicknesses (EOT) of 2nm. The dielectric constant of TiO<sub>2</sub> gate dielectric was considered to be 80. Steep retrograde channel doping is used with surface doping concentration of  $8 \times 10^{12}$  cm<sup>-3</sup>. The complete summary of DG-NMOSFET process flow is given below in table 2.

**Table 2 Summary of DG-NMOSFET design features process flow.**

PROCESS	DG-NMOSFET
Initial substrate doping, N <sub>a</sub>	Boron, B = $1 \times 10^{18}$ cm <sup>-3</sup>
Retrograde well	Boron, B = $8 \times 10^{12}$ cm <sup>-2</sup> E = 100keV
Gate oxide thickness, t <sub>ox</sub>	2.0nm
Source/drain implant	Arsenic, As = $9.5 \times 10^{11}$ cm <sup>-3</sup> E = 10keV
Halo Implantation	Boron, B = $3 \times 10^{13}$ cm <sup>-2</sup> E = 20keV / 30°
Spacer deposition	100nm
Source/Drain implant	Arsenic, As = $6.6 \times 10^{17}$ cm <sup>-2</sup> E = 82.75keV
Final Rapid Thermal (RTA)	1000°C/1 sec

**RESULTS & DISCUSSION.**

The results of fabrication & simulation of 80nm NMOS can be viewed in the TONYPLOT as shown below.



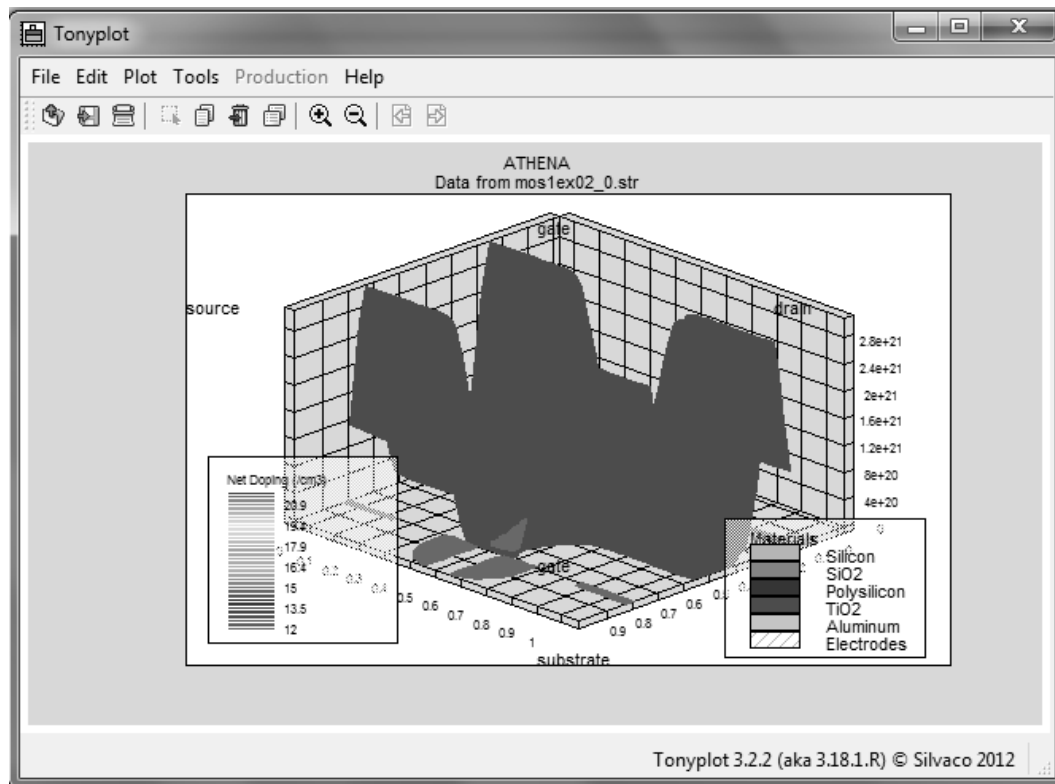
**Figure 2:** Simulated structure of symmetric DG- NMOSFET using  $\text{TiO}_2$  with 80nm gate length.

The simulated device structure (figure 2) is a symmetric N-channel DGMOSFET with following parameters mentioned below in table 3:

**Table 3: Device parameters taken for process simulation of device design using ATHENA simulation tool.**

PARAMETERS	DG-NMOS with $\text{TiO}_2$
Sheet resistance ( $\Omega/\text{square}$ )	1624.97
Channel concentration ( $\text{atoms}/\text{cm}^3$ )	$5.06249\text{e}+017$
Gate oxide thickness, $t_{\text{ox}}$ ( $\mu\text{m}$ )	$0.00208031 \mu\text{m}$ (2.08031nm)
Gate length ( $\mu\text{m}$ )	.08
Gate width ( $\mu\text{m}$ )	.2
Channel length ( $\mu\text{m}$ )	.05
Channel width ( $\mu\text{m}$ )	.6

The simulated DG-NMOSFET structure with source/drain junction depth and net doping concentration is shown below in figure 3.



**Figure 3: DG-NMOSFET structure showing the junction depth.**

## CONCLUSION

Symmetric N-channel DG-MOSFET structure with 80 nm gate length was designed and simulated to study the effect of high-k dielectric ( $\text{TiO}_2$ ), additional gate and oxide thickness on the device performance. It was found that some of the parameters like threshold voltage, sub-threshold swing and DIBL were reduced while drain current was increased upon applying high-k dielectric and additional gate on planar MOSFET device structure. The sub-threshold leakage current was found to be decreased with increasing threshold voltage; this reduces the power consumption and thus improves the device performance. The reduction in gate leakage and sub-threshold swing projects the high-k Double-Gate MOSFET structure to be a strong alternative for future Nanoscale MOS devices. It can also be concluded from the analysis that as device was scaled down, the threshold voltage of the device decreases. Hence, to adjust the threshold voltage and other short channel effects within the permissible limits device engineering can be employed.

## References

- [1] George James T, Saji Joseph and Vincent Mathew, "Effect of counter-doping thickness on Double-Gate MOSFET characteristics", Journal of

- Semiconductor Technology and Sciences, Vol.10, No. 2, pp. 130,132, June 2010.
- [2] M. H. Chowdhury, M. A. Mannan and S. A. Mahmood, “*High-k Dielectrics for Submicron MOSFET*”, IJETSE International Journal of Emerging Technologies in Sciences and Engineering, Vol-2, No.2, pp-8-10, July 2010.
- [3] Shashank N Sensors & Nanotechnology Group, S Basak Birla Institute of Technology and Science, India, R K Nahar, Sensors & Nanotechnology Group, Central Electronics Engineering Research Institute Council of Scientific and Industrial Research (CSIR), India, “*Design and Simulation of Nano Scale High-K Based MOSFETs with Poly Silicon and Metal Gate Electrodes*”, International Journal of Advancements in Technology, IJoAT, Vol 1, No 2, pp-2 October 2010.
- [4] Syafeeza Binti Ahmad Radzi, Electronics and Telecommunication “*Simulation of 0.18 micron mosfet and its characterization*”, M.Tech. Thesis under faculty of Electrical Engineering University Technology Malaysia, pp- 47, 55, 71-76, October 2005.
- [5] Vinay K. Yadav and Ashwani K.Rana, “*Impact of channel-doping on DGMOSFET parameters in Nano Regime-TCAD simulation*”, International Journal of Computer Applications, Vol 37, No. 11, pp.36-40, January 2012.
- [6] Wikipedia, the free encyclopedia, available at, [http://en.wikipedia.org/wiki/sheet\\_resistance](http://en.wikipedia.org/wiki/sheet_resistance).
- [7] X. Loussier, D. Munteanu and J.L. Autran, “*Impact of high-permittivity on speed performances and power consumption in Double-Gate based CMOS circuits*”, Journal of Non-Crystalline Solids, vol. 353, pp.639-644, 2007.