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Noise Tolerance Dynamic CMOS Logic Design with Current Mirror Circuit

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Abstract

Dynamic CMOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. These circuits requires less number of transistors as compare to CMOS logic circuits Dynamic logic circuits are much affected by noise as compared to static CMOS circuit. This is due to the fact that dynamic logic circuits have lower value of switching threshold voltage, which is equal to the threshold voltage of the pull down NMOS devices. On the other hand, switching threshold voltage of static CMOS logic circuit is around half the supply voltage. Our work introduces a novel noise-tolerant design technique using circuitry exhibiting a negative differential resistance effect.

Keywords: Dynamic logic, keeper logic, domino logic.

INTRODUCTION

Noise is a major issue in design of dynamic CMOS logic circuits. Noise is refers to any phenomenon that causes the voltage at a node to deviate from its nominal value. In deep submicron region various noise sources are related to cross talk, leakage current, charge sharing and variations in the supply voltage. Noise sources in dynamic logic circuits can be broadly classified into two basic types: i) gate internal noises, including charge sharing noise, leakage noise, and so on, and ii) external noises, including input noise, power and ground noise, and substrate noise. Power and ground bouncing noise is caused by the resistive and inductive parasitic of on-chip power and ground distribution networks, off-chip bonding wires, and pins of package. The package parasitic impedances typically play the most important role in the generation of mode transition noise. Dynamic logic circuits are much affected by noise as compared to static CMOS circuit. This is due to the fact that dynamic logic circuits have lower value of switching threshold voltage, which is equal to the threshold

voltage of the pull down NMOS devices. On the other hand, switching threshold voltage of static CMOS logic circuit is around half the supply voltage.

Dynamic vs. Static Logic:

Static Logic always has a path from power or ground to the output. In the Static CMOS logic style each logic stage contains pull up and pull down networks which are controlled by input signals. The pull up network contains p channel transistors, whereas the pull down network is made of n channel transistors. The networks are so designed that the pull up and pull down networks are never 'on' simultaneously. This ensures that there is no static power consumption. Dynamic Logic relies on capacitance of gates or other structures to hold state. Noise sources in dynamic logic circuits can be due to gate internal noises which includs charge sharing noise, leakage noise, and so on, and due to external noises, which includes input noise, power and ground noise, and substrate noise. Charge sharing noise is caused by charge redistribution between the dynamic node and the internal nodes of the pull down network. Charge sharing reduces the voltage level at the dynamic node causing potential false switching of a dynamic logic gate. Leakage noise refers to the possible charge loss in the evaluation phase due to sub-threshold leakage current. They are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. Power and ground noise is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package. Substrate noise can affect the signal integrity of a logic gate through substrate coupling.

Domino Logic:

Domino logic offers a simple technique to eliminate the need for complex clocking scheme, by utilizing a single phase clock. A Domino logic module consists of a φn block followed by a static inverter. The introduction of the static inverter has the additional advantage of the output having a low-impedance output, which increases noise immunity and drives the fan-out of the gate. The buffer furthermore reduces the capacitance of the dynamic output node by separating internal and load capacitance. The buffer itself can be optimized to drive the fan-out in an optimal way for high speed. Fig 1 shows domino logic NAND gate. When clk=0, the output is precharged to high logic state and inverter ouput will low. The output of first inverter is connected to the input of subsequent stage, thus subsequent logic stage will be turn off during this precharge stage. The output will discharge when gate is evaluated, making inverter output high conditionally. In domino cascade logics, each state evaluates and causes the next stage to evaluate similarly.

Here in fig 1 and fig 2 the output of first dynamic stage drives one of the input of second dynamic stage. During the precharge phase both outputs are pull up by respective PMOS precharge transistors. During the evaluate phase, the output of the first stage will conditionally discharge. However some delay will be incurred due to finite pull down time. Since the evaluation in second stage is done concurrently, first stage output can discharge to 0 but the output of second stage at the end of evaluation

will be erroneously low shown in fig 3 "Timing simulation of domino logic NAND gate". Thus the clocking scheme and circuit structure must be develop to overcome this problem.

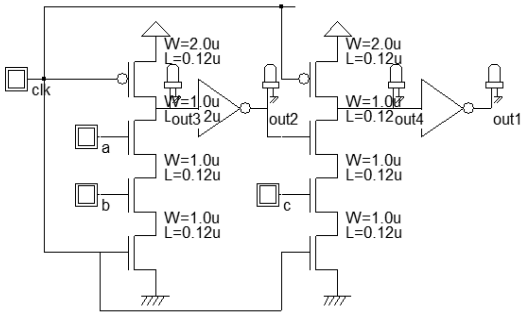

Fig: 1. Domino logic NAND gate

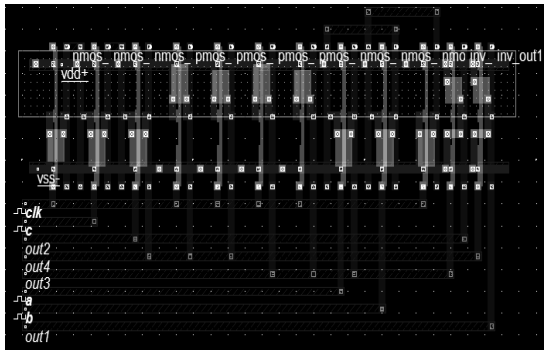

Fig: 2. Layout design of domino logic NAND

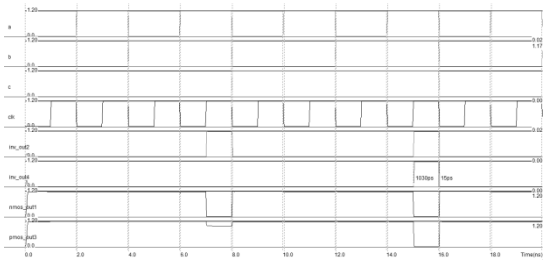

Fig: 3. Timing simulation of domino logic NAND gate

Noise Tolerable Layouts:

Noise sources in dynamic logic circuits can be due to gate internal noises which includes charge sharing noise, leakage noise, and so on, and due to external noises, which includes input noise, power and ground noise, and substrate noise. Charge sharing noise is caused by charge redistribution between the dynamic node and the internal nodes of the pull down network. Charge sharing reduces the voltage level at the dynamic node causing potential false switching of a dynamic logic gate. Leakage noise refers to the possible charge loss in the evaluation phase due to sub-threshold leakage current. They are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. Power and ground noise is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package. Substrate noise can affect the signal integrity of a logic gate through substrate coupling. To offer extremely large resistance a simple circuit of constant current source is use called as current mirror circuit. The current mirror uses the principle that if the gate to source potential of two identical MOSFETs is equal, the channel current flowing through them is equal. A noise tolerable current mirror-based keeper technique as shown in Fig. 4 is domino logic circuit NAND with current

mirror. It consists of a replica transistor whose width is a safety factor times the total NMOS pull down logic width. Fig 5 shows layout of domino logic circuit NAND with current mirror. The gate of this transistor is connected to the source and the leakage current is mirrored to the dynamic node through the PMOS current mirror transistors. Although this technique provides excellent tracking of delay, the contention is still high because the keeper is strongly ON during the beginning of the evaluation phase. Fig 6 shows timing simulation of Domino logic circuit NAND with current mirror.

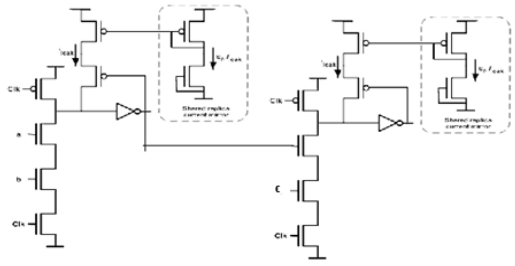

Fig: 4. Domino logic circuit NAND with current mirror.

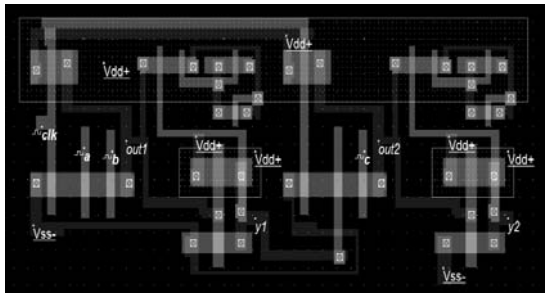

Fig: 5. Layout of Domino logic circuit NAND with current mirror.

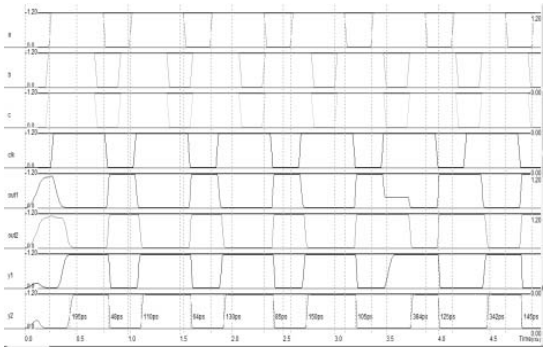

Fig: 6. Timing simulation of Domino logic circuit NAND with current mirror.

CONCLUSION

A layout of two input domino logic circuit NAND gate is designed using the proposed technique. A noise injection circuit (NIC) is used to apply noise pulses of certain amplitude and duration to one of the node. Simulations were done with microwind layout tool. The parameters used for comparison are leakage current, power consumption, delay analysis etc.

The dynamic power dissipation with noisy signal calculated is 97uW with the average current though design is 0.763mA. The noisy signal of 49MHz frequency of amplitude 0.164V can be reduce to 67MHz frequency of amplitude of 0.07V.

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