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Harmonic Reduction using Proposed Multilevel Inverter

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Abstract

This paper presents the analysis and control of a load connected photovoltaic generation system. The model contains a detailed representation of the solar array, load side multilevel neutral point clamped voltage source inverter. The simple structure of multilevel converter enables the voltage stress across the power semiconductor devices to be decreased. The use of medium voltage rated semiconductor devices for high voltage, high power application. The PQ control approach has been presented for the multilevel inverter. One of the most common control strategies applied to decentralized power generator is based on power direct control employing a controller for the dc link voltage to regulate the injected current to the utility network. The proposed models were implemented in Matlab/ Simulink environment.

Keywords: Neutral point clamped inverter, Harmonics, Sinusoidal pulse width modulation.

1. Introduction

The multilevel inverters have drawn tremendous interest in the power industry. They present a new set of features that are well suited in reactive power compensation. It is easier to produce a high power, high voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled with increasing the number of voltage levels .The unique structure of multilevel voltage source inverters

allows them to reach high voltages with low harmonics. As the number of voltage levels increases the harmonics content of the output voltage waveform decreases significantly. One of the most common control strategies structures applied to decentralized power generator is based on power direct control employing a controller for the dc link voltage and a controller to regulate the injected current to the utility network. The system components and power control scheme are modeled in terms of dynamic behaviors.

Neutral Point Clamped topology to generate better output performance presented in[1]. He proposed of multilevel topology to higher number of voltage levels using the similar principle of clamping the intermittent levels with diodes. The first practical multilevel topology is the neutral-point-clamped topology first introduced by Nabae, et al., in 1981. He explained about NPC VSI in[2]. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels. He explained harmonic distortion in[3]. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. He explained types of multilevel inverter in[4]. In[5] he explained about how double the power rating of voltage source inverter for a given semiconductor device. In[6] he explained to obtain high quality sinusoidal output voltage with reduced harmonics. He proposed system is an effective replacement for the conventional method which produces high switching losses. In**[7]** improved MPPT converter with current compensation method for small-scaled PV-applications. The proposed method implements maximum power point tracking (MPPT) by variable reference current which is continuously changed during one sampling period. In[8] focused on various Maximum Power Point control algorithm to lead the operating point of the PV panel to optimum point. This paper proposed a diode clamped multi level inverter to reduce the harmonics.

2. Constructional Features

Photovoltaic cells (PV) generate electricity from solar energy. A number of photovoltaic cells will be connected together in an "Module", encapsulated in glass be mounted as required. In most cases, a number of panels (modules) will be connected together to form an "Array". Panels of a similar type are connected in series to give a higher voltage. Panels can be connected in parallel to give an increased current. The photovoltaic with multilevel inverter is connected to load. Fig. 1 shows the block diagram of photovoltaic with multilevel inverter. The literature reveals several models of different photovoltaic generators and the parameters involved in the calculation of voltage and current. This paper presents two diodes configuration[7]. [8]focused on various Maximum Power Point control algorithm to lead the operating point of the PV panel to optimum point..

The model of the PV generator, must find the electrical equivalent to that source. Several models of PV generator parameters involved calculation of V& I. The current generated by the module

$$I= I_{ph}-I_{d1}-I_{d2}-I_{RP} \quad (1)$$

V and I represents the output voltage and current of PV, I_{ph} the light-generated current of the solar array , I_{RP} is current in resistance R_{sh} , R_s is series resistance , R_{sh} is shunt resistance.

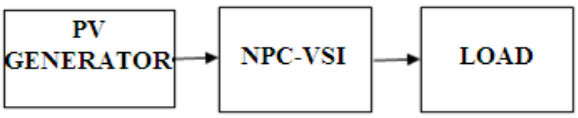

Fig. 1: Block diagram of photovoltaic with multilevel Inverter.

2.1 Multilevel Inverter

The multilevel inverters constructing the output waveforms with multiple voltage steps, the output waveforms clearly resemble the desired sinusoidal waveforms, the output harmonic distortion is improved. Multilevel converter structures enable the voltage stress across the power semiconductor devices to be decreased with the increase number of voltage levels, enabling the use of medium voltage rated semiconductor devices to construct the converters for high voltage, high power applications.

2.2 Neutral Point Clamped Voltage Source Inverter

Neutral Point Clamped Voltage Source Inverter is the type of multilevel inverter. The diode-clamped inverter as also called the neutral-point clamped (NPC) inverter because when it was first used in a three-level inverter the mid-voltage level was defined as the neutral point level. The ability of the NPC topology to generate better output performance in terms of harmonic content prompted the development of multilevel topology to higher number of voltage levels [1]. Such multilevel structures are known as ‘diode clamped multilevel inverters’. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels [3].The diode clamped inverter provides multiple voltage levels from a series bank of capacitors [4]. The voltage across the switches has only half of the dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device[5].

Neutral point clamped multi-level inverter has a wide application prospect in high-voltage and adjustable speed drive systems due to its low stress on switching devices, low harmonic output, and simple structure.

3. Analysis of Diode-clamped Multilevel Topology

This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress. For topologies with more than three levels the clamping diodes are subject to increased voltage stress.

3.1 Structure of Three Level Diode Clamped Multilevel Inverter

The three-level neutral point-clamped voltage source inverter is shown in Fig. 4.6. It contains 12 unidirectional active switches and 6 neutral point clamping diodes. The middle point of the two capacitors "*n*" can be defined as the neutral point [6]. The major benefit of this configuration is each switch must block only one-half of the dc link voltage ($V_{dc}/2$). In order to produce three levels, only two of the four switches in each phase leg should be turned on at any time. The dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_a and C_b, they are same in rating.

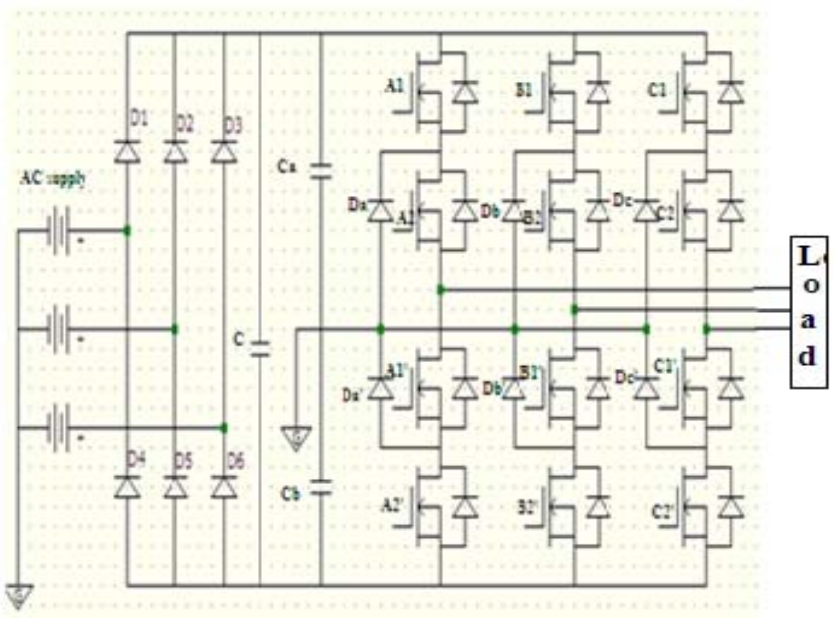

Fig. 2: Three Level Diode clamped multilevel inverter.

The diodes are all same type to provide equal voltage sharing and to clamp the same voltage level across the switch, when the switch is in off condition. Hence this structure provides less voltage stress across the switch.

Principle of Operation One Leg Bridge

3.2 Operation of one leg in Diode clamped multilevel inverter is explained. To produce a staircase-output voltage, consider one leg of the three-level inverter. The steps to synthesize the three-level voltages are as follows.

1. For an output voltage level $V_{ao}=V_{dc}$, turn on all upper-half switches A1and A2. 2. For an output voltage level $V_{ao}=V_{dc}/2$, turn on one upper switch A2 and one lower switch A1'. 3. For an output voltage level $V_{ao}=0$, turn on all lower half switches A1'and A2'.

The voltage levels and their corresponding switch states follows, state condition 1 means the switch is on, 0 means the switch is off. There are two complementary switch pairs in each phase. These pairs for one leg of the inverter are (A1, A1'), (A2, A2'). If one of the complementary switch pairs is turned on, the other of the same pair must be off. The phase voltage waveform of the three-level inverter V_{ao}. The m-level converter has an m-level output phase-leg voltage and a (2m-1)-level output line voltage.

4. Modulation Topologies for Multilevel Inverter

4.1 Sinusoidal pulse with modulation

This Fig. shows the sinusoidal pulse width modulation control for three level neutral point clamped voltage source inverter. Fig. 3 shows the waveform of sine-triangle intersection. And two carriers together with modulation signal have been used to obtain SPWM control. Fig. 4,5 shows the gate pulses for A1, A1', A2, A2' Switches.

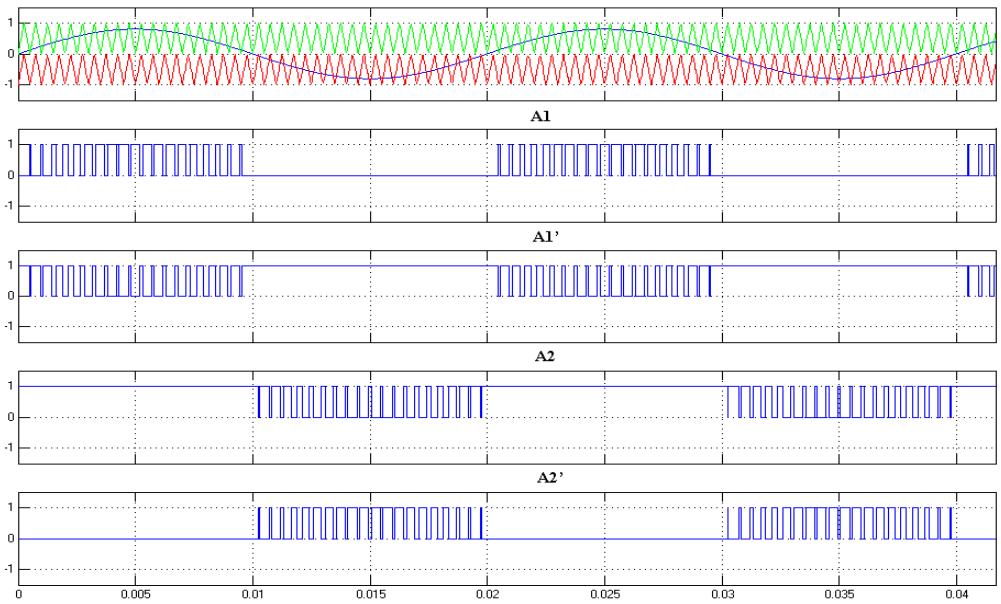

Fig. 3: Career signal together with modulation signal,
Gate pulse for A1, A1', A2, A2'switches

A single reference sine wave (V_a) is compared with two carriers waves to generate pulses. The pulses generated by comparing V_a. When the compensator current is controlled indirectly varying the converter output voltage, it is called indirect current controlled. By controlling the phase angle of the inverter output voltage, the dc capacitor voltage V_{dc} can be changed. Thus, the amplitude inverter output can be controlled. Phase angle control method is an example for indirect control.

5. Results and Discussion

5.1 Simulation Model and Result

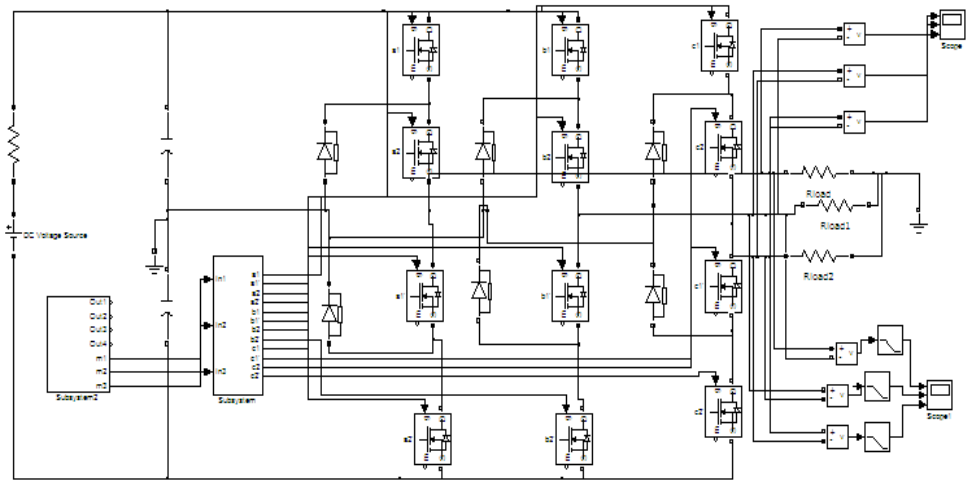

Fig. 8: Simulink model of Multilevel inverter with load.

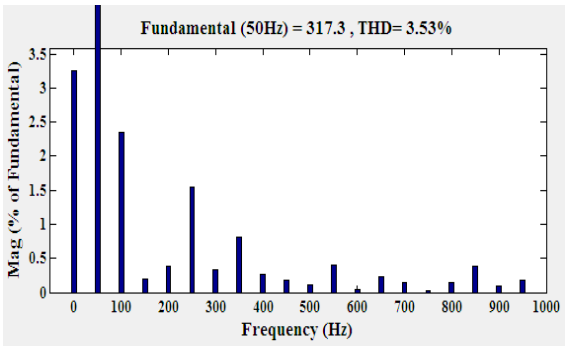

Fig. 9: Harmonics of MLI with PQ control

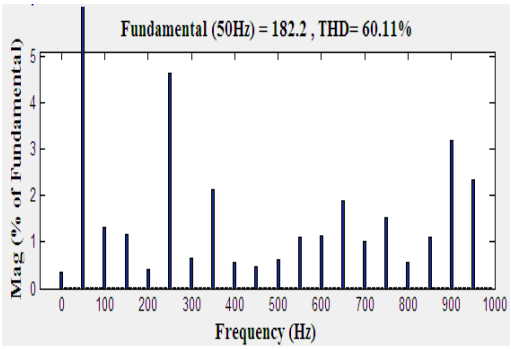

Fig. 10: Harmonics of MLI without control

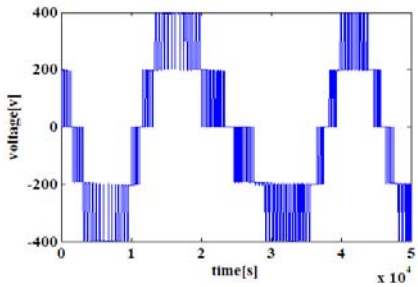

Fig. 11: MLI output line to line voltage V_{ab} waveform of without filter

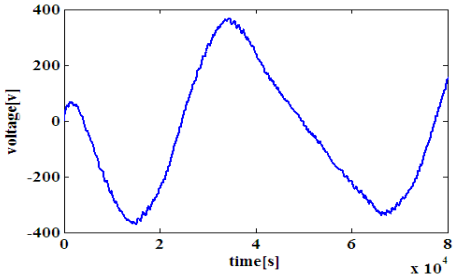

Fig. 12: MLI output line to line voltage V_{ab} waveform of filter

6. Conclusion

This paper aims to reduce the harmonics at the output voltage. And control the voltage of the solar panel in order to obtain the maximum power possible from a PV generator, the solar insulation and temperature conditions. The results obtained with this solution confirm the good performances of the proposed solution. The results obtained promises to use the diode clamped multilevel inverter in high voltage and great power applications as electrical power applied to decentralized power generator is based on Power direct control. The topology is simulated in MATLAB. The harmonics are reduced in the diode clamped multilevel inverter and the experiments are carried out to test the performance of the circuit.

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