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Simulation of Five-Level Inverter with Sinusoidal PWM Carrier Technique Using MATLAB/Simulink

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Abstract

Nowadays numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. The multilevel inverter topologies began with the three level converters. The elementary concept of a multilevel converter is to achieve higher power to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. However, the output voltage is smoother with a three level converter, in which the output voltage has three possible values. In this paper the method of minimization of THD is proposed which is based on multilevel inverter. A sinusoidal pulse width modulation scheme is developed for the multilevel inverter. In this paper, different five level inverter topologies and SPWM technique has been applied to formulate the switching pattern for five level inverter that minimize the harmonic distortion at the inverter output. Simulation result are discussed.

Keywords— Multilevel Inverter, THD, sinusoidal pulse width modulation.

I. Introduction

Power electronics devices contribute important part of harmonics in all kind of applications, such as power rectifiers and thyristor converters. Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having

large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The unique structure of multi- level inverter allows them to reach high voltages and therefore lower voltage ratinFg device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave.

Even updated PWM techniques used to control modern static converters such as machine drives, power factor compensators or active power filters, do not produce perfect sinusoidal waveforms, which strongly depend on the semiconductors switching frequency. Normally, with voltage or current converters, as they generate discrete output waveforms, forcing the use of machines with special isolation, and in some applications large inductances connected in series with the respective load are required. In other words, neither the voltage nor the current waveforms are as expected. Also, it is well known that distorted voltages and currents waveforms produce harmonic contamination, additional power losses, and high frequency noise that can affect not only the power load but also the associated controllers. All these unwanted operating characteristics associated with PWM converters can be overcome with multi-level converters.

Plentiful multilevel converter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. This paper reviews state of the art of multilevel power converter technology along with the fundamental multilevel converter structures and modulation paradigms.FFT analysis can be carried out further and the total harmonic distortion in the supply system can be calculated. Finally, the possible future developments of multilevel converter technology are noted.

II. Theoretical Background

A. Multilevel inverter Structure

The unique structure of voltage source inverters allows them to reach high voltages with low harmonics without the use of series-connected synchronized switching devices or transformers. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter can be implemented in many different ways. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms. More complex structures effectively insert converters within converters. The voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices. Several multilevel

inverter topologies have been developed; i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. Referring to the literature reviews, the cascaded or H-bridge multilevel inverter with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications. The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and lower
2. $\frac{dv}{dt}$.
3. They draw input current with very low distortion.
4. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
5. They can operate with a lower switching frequency.

B. Multilevel inverter Controller

The sinusoidal PWM technique is very popular for industrial converters. Shows the general principle of SPWM, where an isosceles triangle carrier wave of frequency f_c is compared with the fundamental frequency f sinusoidal modulating wave, and the points of intersection determine the switching points of power devices.

Carriers used in multilevel inverter may be vertically shifted or horizontally shifted. Advantage of horizontally shifted carriers scheme is that, each modules are switched on and off with a constant number of times by period, independently of magnitude of generated voltage. But vertically shifted carrier scheme can be more easily implemented on any digital controller. Vertically shifted scheme comes with three variant.

The detailed classification is given in the table below.

1. All carriers are in phase (PH disposition)
2. All carries above the zero reference are in phase, but in opposition with those below (PO disposition)
3. All carriers are alternatively in opposition (APO disposition)
4. All carriers are shifted by 90°.

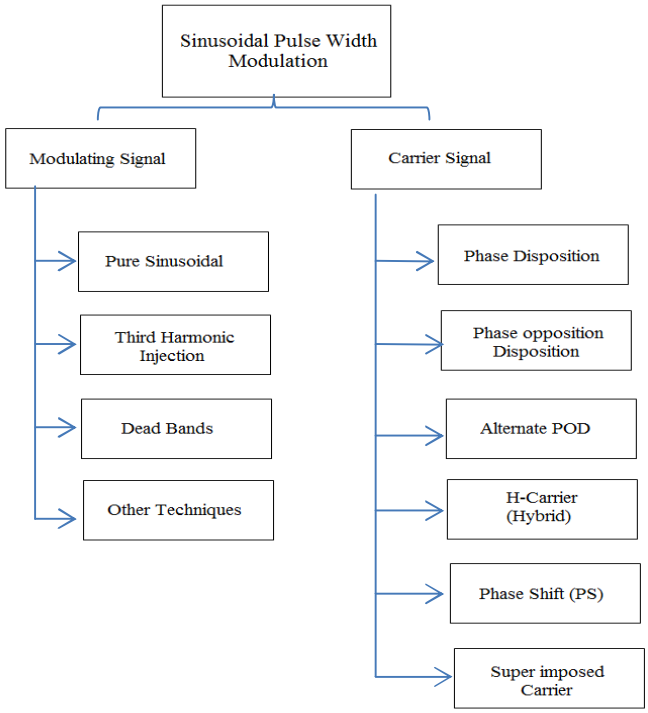

Figure. 1 Modulation techniques for Multilevel Inverter

III. SYSTEM STRUCTURE& ANALYSIS

A. *Implementation of SPWM Technique*

Digital implementation SPWM technique is based on classical SPWM technique with carriers and reference sine waveform. Only difference between them is, in digital SPWM a table consisting of values of sine waveform sampled at certain frequency is used. As result reference wave form in digital SPWM represents a sample and hold waveform of sine wave forms. This sampling of sine waveform comes in two variants;

a) Symmetrical sampling
b) Asymmetrical sampling.

In symmetrical sampling, reference sine waveform is sampled at only positive peak of the carrier waveform and sample is held constant for the complete carrier period. This introduces the distortion in modulating signal and phase shift between modulating signal and fundamental component of output voltage. Here sampling frequency is equal to carrier frequency. The phase shift is given by π/m_f

Where,

$$m_f = \frac{f_c}{f_m}$$

f_c = Carrier frequency.
f_m = Reference Sine wave frequency.

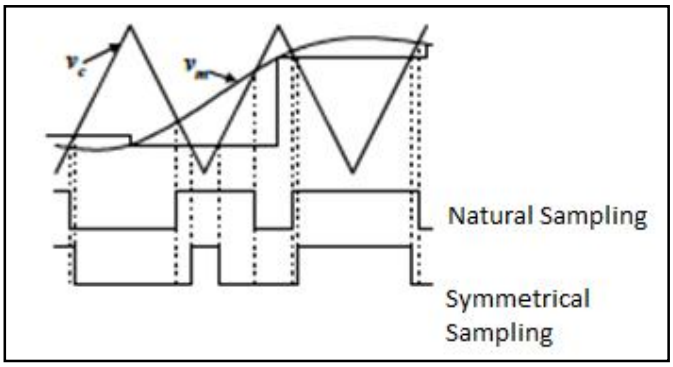

Figure 2: Natural sampling, Symmetrical Sampling

In asymmetrical sampling, the reference signal is sampled at positive as well as negative peak of carrier frequency and held constant for half the carrier period. Here sampling frequency is twice the carrier frequency. Asymmetrical sampling is the preferred method, since each switching edge is the result of new sample and give better performance as shown in Fig. The phase shift is by, $\pi/2mf$

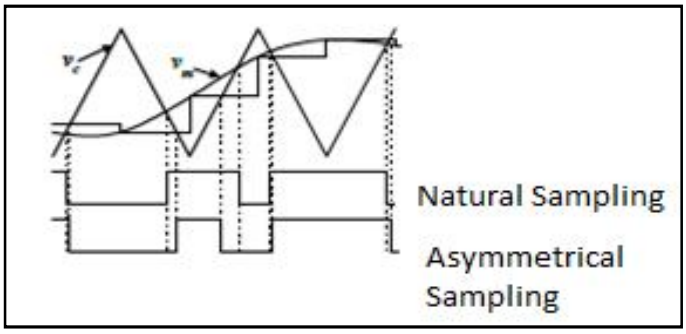

Figure 3: Natural sampling asymmetrical sampling

Comparing natural SPWM and digital SPWM, digital SPWM has following disadvantages,

1) Digital SPWM method sample the signal input at the beginning of the switch cycle, before the actual switching edge reflects this value later in the cycle.

2) This introduces a delay in out-put waveform. A delay of π/mf and $\pi/2mf$ is introduce is symmetrical and asymmetrical sampling method respectively, where mf is frequency modulation ratio.

3) This delay in response is significant when the ratio of switch frequency to reference frequency (the pulse number) is small. It leads to a frequency response roll-off which obeys a Bessel Function, similar to the familiar sine function roll-off for Pulse Amplitude Modulation (PAM).

4) Another unwanted effect of digital SPWM is odd harmonic distortion of the

synthesize Waveform. The severity of these effects is a function of the ratio of the modulating and carrier frequencies.

B. ***Alterative Phase Opposition Disposition (APOD)***

This technique requires each of the $(m-1)$ carrier waveforms, for an m-level phase waveform, to be phase displaced from each other by 1800 alternately as shown in Figure 2.3. The most significant harmonics are centered as sidebands around the carrier frequency f_c and therefore no harmonics occur atf_c.

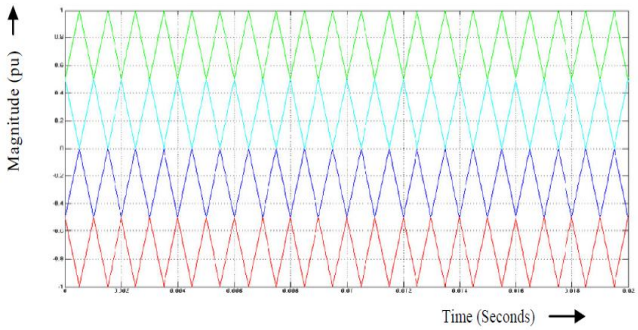

Figure 4: Alterative Phase Opposition Disposition

C. ***Phase Opposition Dispositions (POD)***

The carrier waveforms are all in phase above and below the zero reference value however, there is 1800 phase shift between the ones above and below zero respectively as shown in Figure the significant harmonics, once again, are located around the carrier frequency f_c for both the phase and line voltage waveforms. The three disposition PWM techniques that are APOD, PD and POD generate similar phase and line voltage waveforms. Furthermore, for all of them, the decision signals have average frequency much lower than the carrier frequency.

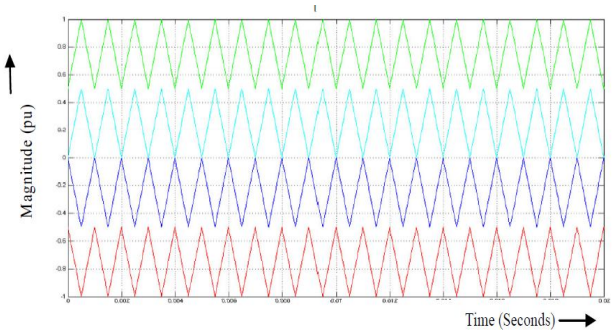

Figure 5: Phase Opposition Disposition

D. ***HCarrier (Hybrid):***

This technique, as mentioned earlier, combines the previously presented ones

(disposition) and the well known phase shifted multicarrier technique. The bands used for modulation are only two, however, each time the level of the power converter is increased, and more triangular carriers are introduced and phase shifted accordingly. The two carriers above zero have the same peak to peak value and the same frequency . However, there is phase shift between them. The same applies for the two carriers below zero. In the case that the number of converter levels is higher, the carriers are phase shifted accordingly, that is for a level system and for a 9 level system and so on and so forth. It is important to note that the significant harmonics are concentrated around multiples of of the carrier frequency f_c. For instance, for a 5 level converter, the harmonics are located around , for a level around and for a level around .The gap between the fundamental and the first significant harmonics increases accordingly as shown in Figure

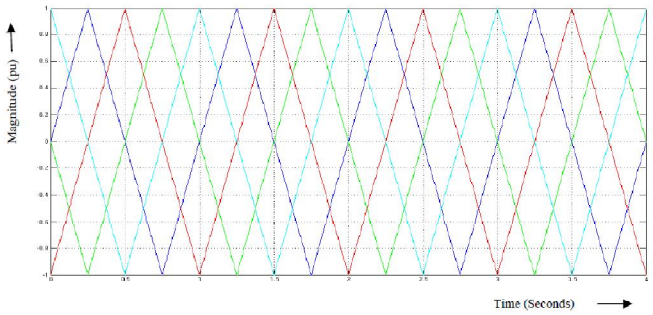

Figure 6: Hybrid carrier

IV. SIMULATION AND RESULTS

A. *Main Power circuit of five level inverter*

The main power circuit of a five level inverter is shown in the figure. Firstly a sinusoidal signal of 50 Hz frequency is compared with four reference carrier signals to generate gating cycles. Then they are given to two cascaded H bridge inverter to generate output voltages.

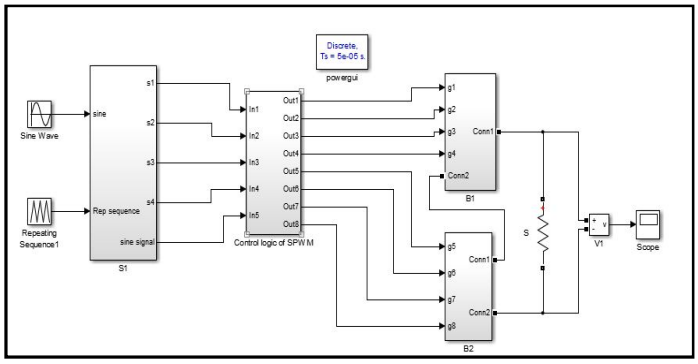

Figure 7: Five level inverter in Matlab/Simulink

B. ***Alterative Phase Opposition Disposition (APOD)***

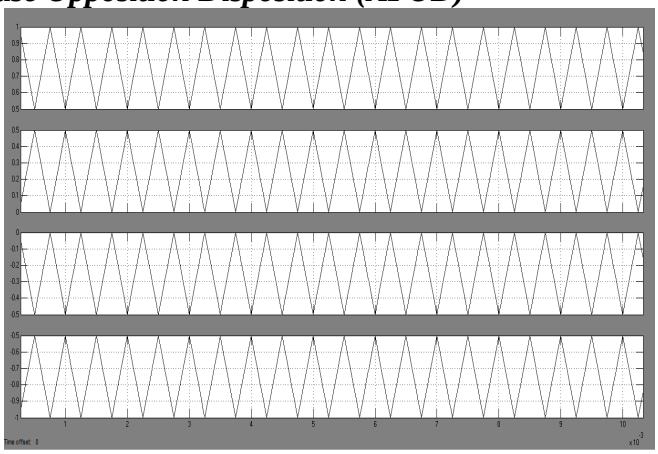

Figure 8: Alterative Phase Opposition Disposition in Matlab/Simulink

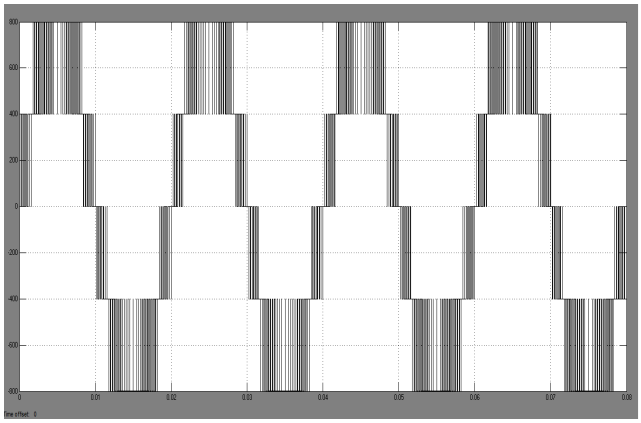

Figure 9: Five level inverter with APOD in Matlab/Simulink

C. *Phase Opposition Dispositions (POD)*

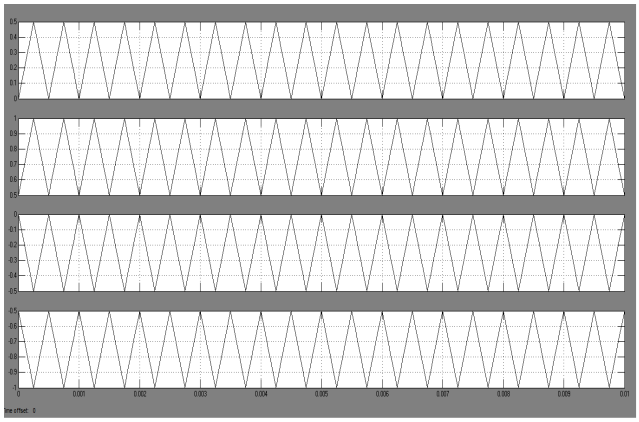

Figure 10: Phase Opposition Disposition in Matlab/Simulink

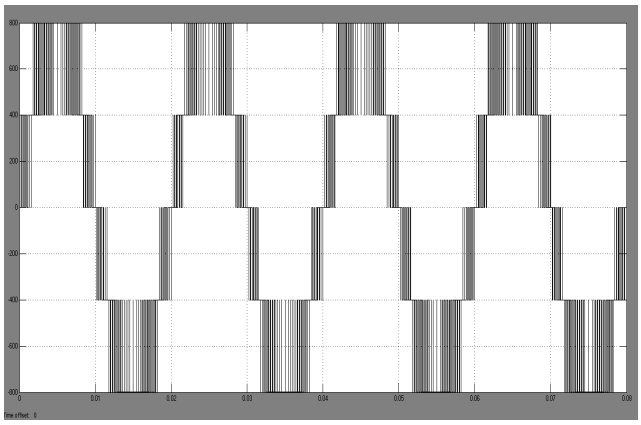

Figure 11: Five level inverter with POD in Matlab/Simulink

D. ***Hybrid Carrier (Hybrid):***

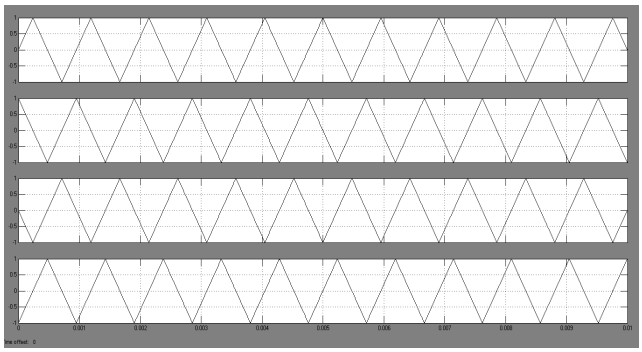

Figure 12: Hybrid carrier in Matlab/Simulink

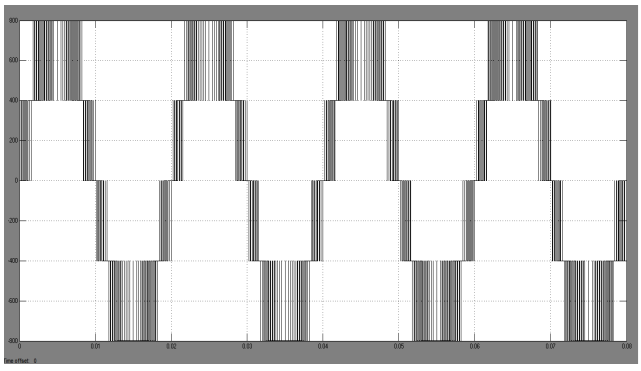

Figure 13: Five level inverter with Hybrid carrier in Matlab/Simulink

CONCLUSION

The paper mainly speaks about the effective ways by which minimization in harmonic

destortion and shaping voltage wave to sinusoidal can achieved by various SPWM techniques.

The performance of any power converter depends on the modulation technique employed and so the multilevel inverters. Several works on the modulation techniques for the five level inverters were implemented but for higher level inverters, the modulation techniques are still mostly unexplored because of large number of inverter switching states and they increase the computational difficulties. The various modulation techniques were simulated using the MATLAB/SIMULINK environment and the output parameters were presented. The analysis is done richly with respect to the fundamental output voltage levels, output total harmonics distortion levels, different modulation indices for multilevel configuration with the different control techniques.

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