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Power Factor Correction with AC-DC Buck Converter

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Abstract

In this Paper the improved buck power factor correction (PFC) converter topology is proposed. This topology is easier to achieve the simple structure compared with the conventional buck PFC converter. Dead zones in ac input current of traditional buck PFC converter can be eliminated by adding an auxiliary switch and two diodes. The improved buck PFC converter is to force that operates in critical conduction mode (CCM) and improved constant ON-time control is proposed and utilized. To meet the IEC61000-3-2 class C standard within the universal input voltage range With optimal control parameters, nearly unit power factor can be achieved and the input current harmonics can be minimized. Moreover, the efficiency of the proposed converter is not deteriorated compared to the conventional buck converter.

***Index Terms*— PowerFactorCorrection (PFC), Buck Converter, MOSFET, MAT LAB/Simulink**

I. Introduction

Some special power products such as lighting equipments power factor correction (PFC) is a good method for providing an almost sinusoidal input current. The boost converter is the most popular topology for PFC application due to its inherent Current shaping ability .However with universal input usually a 400Vdc output voltage is required for the boost PFC.the boost PFC cannot achieve high efficiency at low line. Input because it works with large duty cycle in order to get high-voltage conversion gain. Second, the voltage across the main switch of the buck converter is almost clamped to the input voltage.Thererefore, the buck PFC converter can achieve relatively high efficiency with in the universal input voltage range. When the input voltage is higher than the output voltage, the proposed converter operates in buck mode, which is same as the conventional buck converter. When the input voltage is lower than the output voltage, the proposed converter operates in buck-boost mode. Hence, there are no dead zones in the input current.[1] The detailed operation principle is illustrated in Section II and the circuit parameters design considerations are presented in Section III.Finally, the experimental results based on a 100-W prototype will be given in Section I

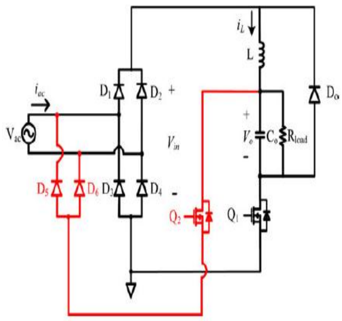


Fig1.Proposed improved buck PFC converter

In this paper, an improved buck converter is proposed as shown in Fig1.Compared with the conventional buck PFC converter, an auxiliary switch and two diodes are added in the improved buck PFC converter. [2]The proposed converter has two different operation modes in line period. When the input voltage is higher than the output voltage, the proposed converter operates in buck mode, which is same as the conventional buck converter.

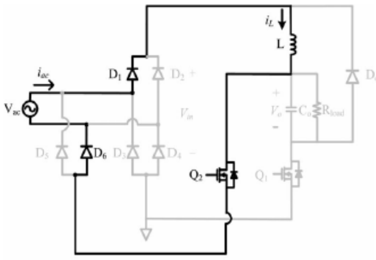
II. PRINCIPLE OF OPERATION

A. Positive Buck-Boost Operation Mode

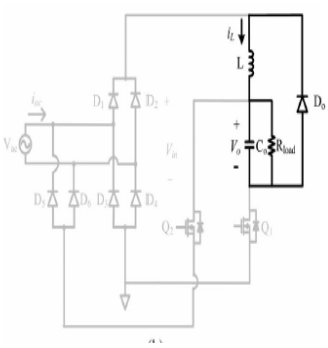
When the input voltage Vac is in positive half cycle and then magnitude of Vac smaller Than Vo,the proposed converter operates buck-boost mode. During this mode, Switch Q_1 keeps OFF and switches Q2 keeping switching .[3]There are two stages When the proposed converter operates under this mode

Stage 1:

When switch Q2 is ON, The proposed converter operates in stage 1. The equivalent circuit of this stage is shown in fig 2(a).The inductor L is change by Vac through D_1 and D_6, and i_L increases during this stage



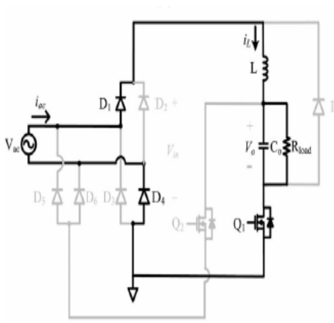
(a)



(b)

Stage 2:
When switch Q2 is OFF, *the* proposed converter operates in stage2. The equivalent circuit of this stage is shown Fig 2(b). The inductor L is discharged by Vo through D0 and i_L decreases during this stage

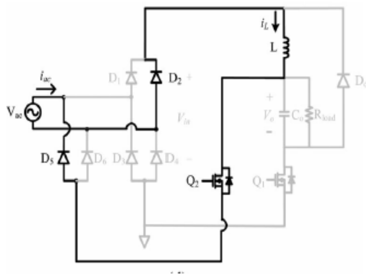
B. Positive Buck Operation Mode
When the input voltage Vac is in positive half cycle and the Magnitude is larger than V_O, the proposed converter operates in buck mode. [4]During this mode, switch Q2 keeps OFF and switch Q1 keeps switching. There are two stages when the proposed converter operates under this mode.



(c)

Stage 3:

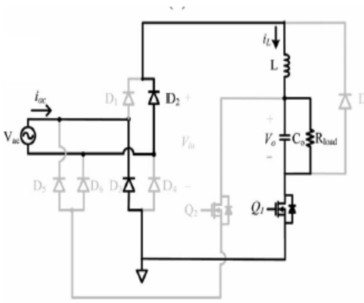
When switch Q1 is ON, the proposed converter Operates in stage3.The equivalent circuit of this stage is shown in fig 2(c).The inductor L is change by Vac-Vo through D1 and D4and Il increases during this stage.



(d)

Stage4:

When switch Q1 is OFF, the proposed converter operates in stage 4. The equivalent circuit of this stage is same As that of stage2,as shown in fig.2(b).The inductor L is discharge by Vo and Do and i_L decrease during this stage discharged by *Vo* through *Do* , and *iL* decreases during this stage.



(e)

Fig 2.Equivalent circuits of the proposed converter in eight stages.

When the input voltage Vac is in negative half cycle, there also exit two operation modes of negative buck-boost operation mode and negative buck operation mode of the proposed converter. The negative operation processes can also be separated into four operation stages define as stages 5-8 and the equivalent circuit include Fig2 (b),(d) and (e).The negative half cycle operation processes of the proposed converter are similar to those of the positive half cycle .For simplicity, the negative operation processes are not depicted in detail here

III. CONTROL STRATEGIES OF PROPOSED SYSTEM

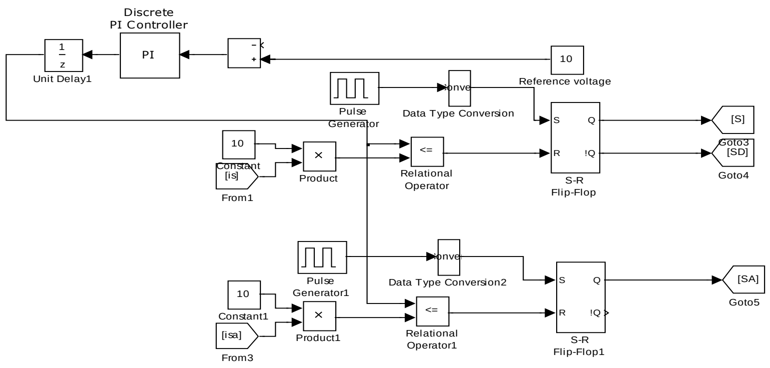


Fig3.control strategies of proposed system

An improved COT control is applied for the proposed buck PFC converter to force it that operates in CCM as shown in fig 3.The output voltage is detected with a level shift circuit formed by a high-voltage transistor Q_2 and the resistorsRa_1~Ra_4.some Key wave forms are shown in fig4. Usually, V boundary is set to reflect the output voltage Vo with the same ratio as that V_in reflects Vin .Vph is high logic.

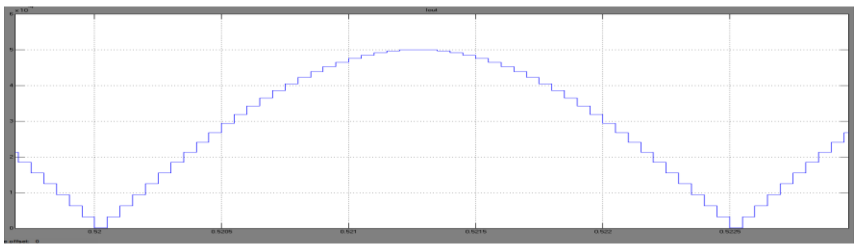


Fig4.Control strategies circuit current wave form

When V_in is higher than $V\mathrm{boundry}$ and is low logic when V_in is lower than $V\mathrm{boundry}$. The detected output signal $V\mathrm{FB}$ is sent to the negative input of the error amplifier Uf . The error between $V\mathrm{FB}$ and the set reference $V\mathrm{ref}$ is amplified by the compensation networks Cf and an amplified error signal $V\mathrm{comp}$ is achieved. The dc voltage signal V_comp applied to control the conduction period $T\mathrm{ON}$ is achieved from $V\mathrm{comp}$ through a control networks formed by resistors $R1$ and $R2$ and switch $S1$. Switch $S1$ is controlled by the control signal $V\mathrm{ph}$.

$$V^{1}_{COMP} = \begin{cases} Vcomp & |Vin > Vo \\ K.\ Vcomp & |Vin < Vo \end{cases}$$

The zero-crossing point of the inductor current *iL* is detected by the auxiliary winding of the inductor *L*. This inductor current zero-crossing detection signal V_{ZCD} can be applied in both buck-boost modes. When the inductor current *iL* falls t zero, the output voltage auxiliary winding V_{ZCD} starts to fall. Once V_{ZCD} falls to zero, the output of comparator $Uc2$ jumps from low level to high level. [5]-[8]This level transition sets the driving signal from low level to high level.

IV. SIMULATION RESULTS

A. Conventional circuit

A input and 80 Vdc output is built up to verify the proposed buck PFC converter. The schematic of the prototype is shown in Fig. 4 with the key parameters. [6]The improved Constant ON Time Control(COT) control shown in Fig. 5 is applied for the prototype and the control circuit is realized with discrete components. The coefficient k is set to 1/4 by the network of R1 and R2. For comparison, a 100 W prototype of the traditional buck PFC converter is also built up.

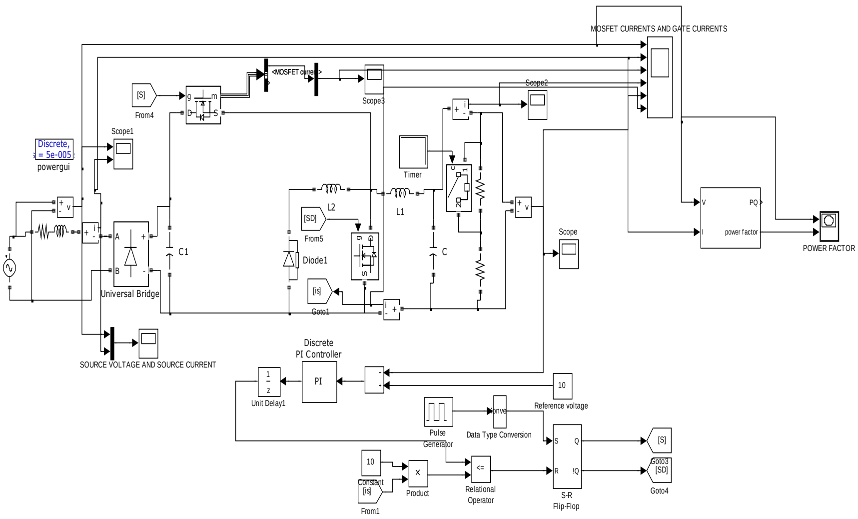


Fig 5 Simulation diagram for Conventional BUCK Converter for PFC

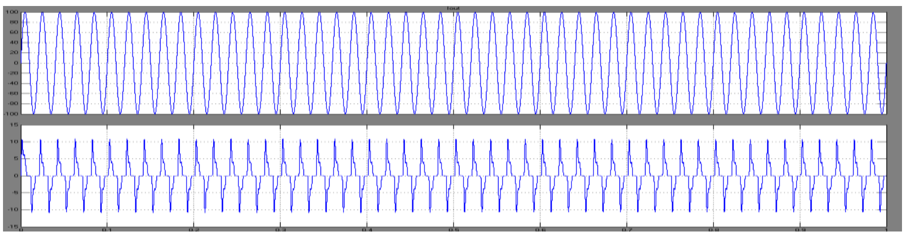


Fig6.Input voltage and current

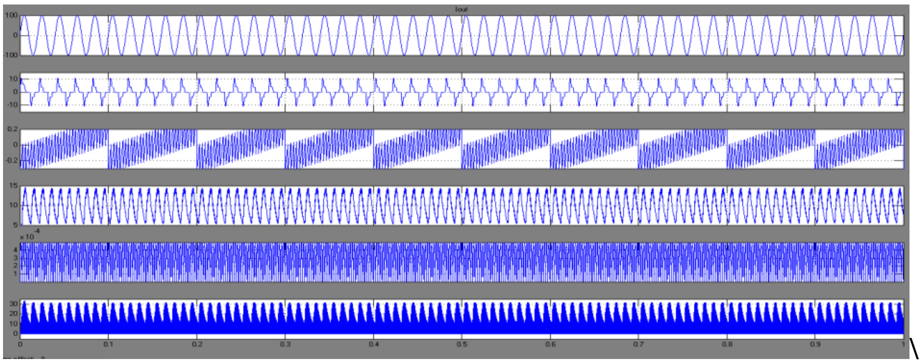


Fig7. Key waveforms in the improved COT control diagram

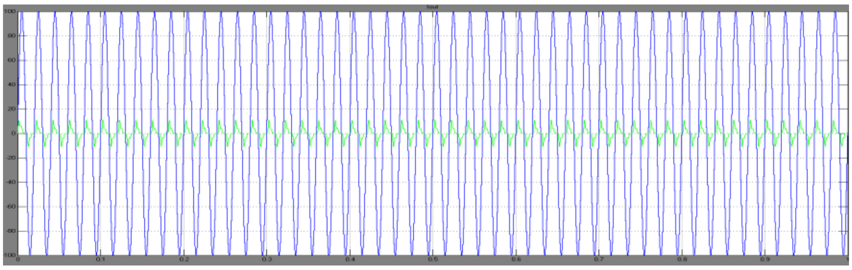


Fig8. Measured input voltage and input current waveforms of buck PFC converter.

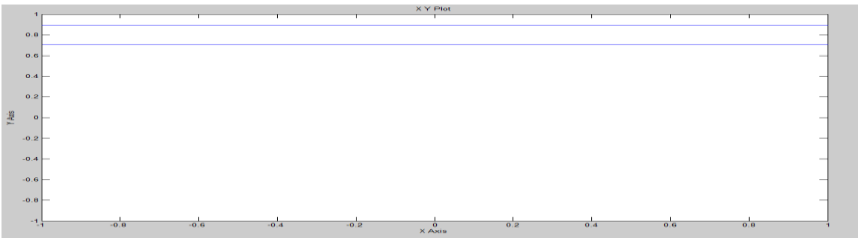


Fig9. Measured conventional power factor wave form

Measured input voltage and input current waveforms of the conventional buck PFC converter with full load at 90 Vac input are shown in Fig. 8

B. Proposed Circuit

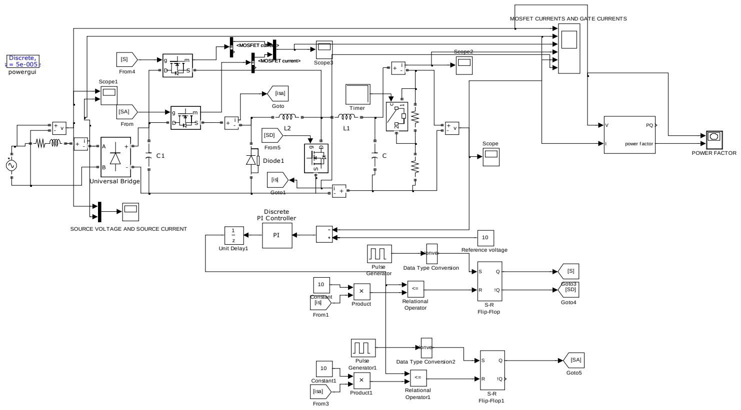


Fig 10.Simulation diagram for Proposed BUCK Converter for PFC

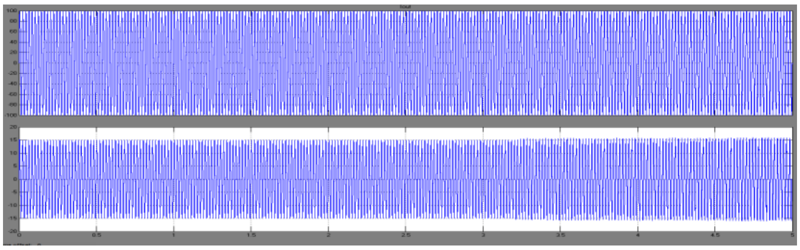


Fig11.Input voltage and current

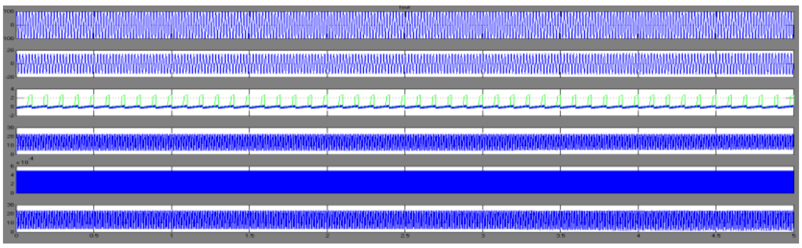


Fig12. Key waveforms in the improved COT control diagram

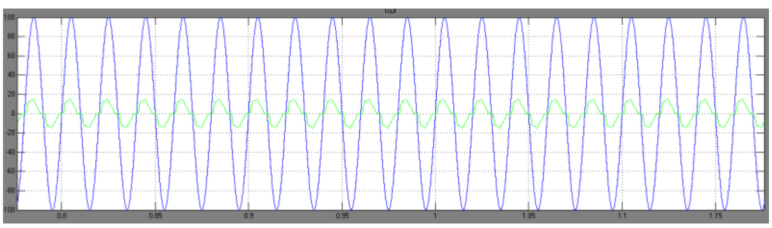


Fig13.Measured input voltage and input current waveforms of buck PFC converter

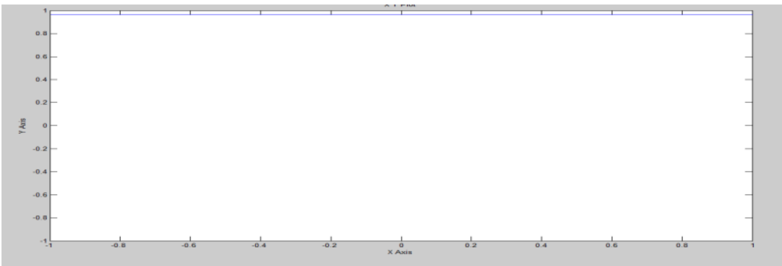


Fig14. Measured Proposed Buck Converter power factor wave form

Measured input voltage and input current waveforms of the proposed buck PFC converter with full load at 90 Vac input are shown in Fig. 9 the input current waveforms fit well with the calculation results as shown in Fig. 10.Measured PF at different input voltage with full load of the buck PFC converter and the proposed converter is shown in Fig. 11. Obviously, the proposed converter can improve the PF greatly especially at low line voltage.

V. CONCLUSION

The proposed buck PFC converter topology in this paper is easy to achieve as the structure of the topology is simple. To operate in CRM, an improved COT control is proposed. Nearly unit PF can be achieved and the input current harmonics can meet the IEC61000-3-2 class C standard within the universal input voltage range, whereas the efficiency is not deteriorated compared to the conventional buck converter. However, the cost and size increase little compared to the whole cost and size.. In conclusion, this proposed converter is very suitable for industrial applications.

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