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Optimized Magnetic Flip-Flop Combined With Flash Architecture for Memory Unit Based On Sleep Transistor

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Abstract

The portability in the electronic circuits is achieved by the use of battery. So its make designs for low power consumption.Normally Non–Volatile Memories of STTMRAM is mainly used to designing process .Because STTMRAM have more advantages i.e., low power, infinite endurance and high speed. But STTMRAM have main disadvantage is high writable energy produced when buildup of MFF.so it's achieve high power consumption. To overcome these disadvantage of STTMRAM using the technique are swapped MOS technique. The MOS is swapped means" Exchange of Transmission". And then removal of NOR flash memory means modified the memory unit based on sleep transistor to achieved the result of reduce power consumption and also reduce the circuit complexity

Index terms: swapped MOS design, MFF, STTM RAM, sleep transistor.

I. INTRODUCTION

The number of flip flop or register is used for compute the advanced microprocessor. The NVM (Non-Volatile Memory) are not need power in standby mode and also easily sored to retain the data value. But the volatile memories need power in standby mode to provide high power consumption. The Spin Transfer Torque Magneto

resistive RAM (STTMRAM) has been combined of both SRAM and DRAM advantages. MRAM stored only the magnetic storage value. We know that DRAM refreshes all cells in their chips. So it is need greater power consumption.

But MRAM never requires a refresh. This means that not only does it retain its memory with the power turned off but also there is no constant power-draw. But one disadvantage of MRAM is provided the read processes are not completed incorrectly and also consume more power. So we can select the spin transfer torque combined with MRAM to the process of both write and read process for maintained at low power consumption.

STTMRAM have more advantages i.e., low power, infinite endurance and high speed. An existing system, we design of ultralow power MFF by using STTMRAM. But STTMRAM have main disadvantage is high writable energy produced when buildup of MFF.so it's achieve high power consumption.

In existing system consists of the blocks as following CMOS D-latch, STTMRAM with Magnetic Flip-Flop and enable circuit. In our proposed system we are going to implement the design as Swapped MOS design our proposed design replacing the blocks are Magnetic Flip-Flop and enable circuit by sleep transistor. Hence the complexity will be reduced and also reduce the power consumption can be obtained.

II. PROPOSED METHOD

The following flow chart describes the entire architecture of this paper fig 1. First create the design of STTMRAM memory based on sleep transistor. After complete the creations of STTMARAM is built properly by using swapped MOS technique. Now these improvise design for our proposed work. This design based on sleep transistor is used for write and read operation during process with low power consumption and also reduces circuit complexity. Then finally create the layout for proposed design using T-Edit of TANNER EDA.

A). STTMRAM

The spin transfer torque MRAM (STTMRAM) have data is stored as magnetic storage elements. These magnetic storage elements as magnetic tunnel junction (MTJ), this MTJ consist of two layers are fixed layer and free layer. The MTJ operation is based on these two layers. The STTMRAM have many advantage such as low power, high speed and without limitation of storage data. STTMRAM design memory based on sleep transistor. Sleep Transistor is circuits designed to minimize power consumption and heat dissipation.This sleep transistor avoids unwanted current received of circuit. Because it receive the current when data is needed. So easily reduce the power consumption.

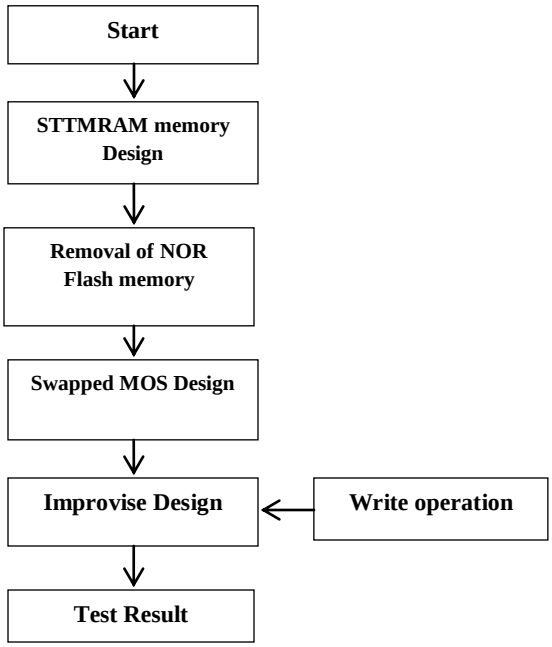

Fig1 Flow Chart for Overall Design

B). NOR Flash Memory

Flash memory stores information in an array of memory cells made from floating-gate transistors. Flash memory stores information in an array of memory cells made from floating-gate transistors. One limitation of flash memory is that, although it can be read or programmed a byte or a word at a time in a random access fashion, it can only be erased a "block" at a time. This NOR flash memory does not needed of error correcting code. Here using the NOR flash memory long erase and write times. It is possible to need more power, so this memory is removed to avoiding the power consumption.

C). Swapped MOS Design

The swapped MOS design is considered as reduce the high writeable energy and reduce circuit complexity. The swapped MOS is derived of two terminal exchanges current or voltage flows of one MOS terminal to other MOS terminal. The two ends are accepted to exchange one stream of source against other stream. And also this Swapped MOS reduce internal current due to its exchange of source. Hence during low power process, stored the data and also retain data become easier.

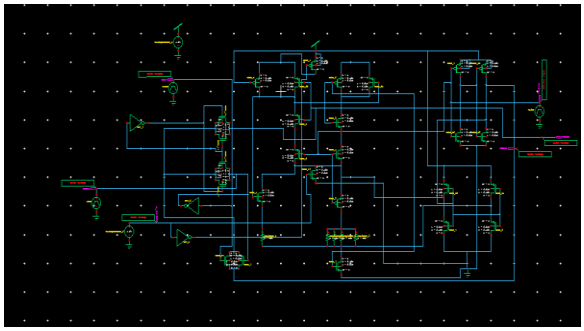

Fig2 Overall Designs

Before using the MFF for data storage process, but high number of bits associated the MFF, unselected cells of leakage current. In this design using of NMOS switches for neglecting of leakage current. Because here use the NMOS switches are two reference cells for even and odd bits is respectively. So t in the number of leakage current in the unselected cells is definitely neglected.The fig2 overall design are compare with existing circuit reduce the circuit complexity and power consumption are reduced.

D). Improvised Design

The removal of NOR flash memory for reduced the power consume. And then Swapped MOS design is based to improvise the design. Here improvise the design is already control of power consume so now applied the process of write operation to achieved of less power consume. And then here unwanted usages of circuit in existing circuits are combined with flash memory removed to reduce also the circuit complexity and improvise the speed performance.

III RESULT AND DISCUSSION

To compare the proposed output with normal CMOS DFF reduce the power consumption <780 and also reduce circuit complexity <64 and maintain the average power as <11. When voltage of write value is high (1) read the value from input of data. When voltage of write value is low (0), output of read value also low shown in fig3.

The fig4 as power consumption output waveform. The fig5 show the full layout of overall design in schematic diagram. As shown in Table 1 size of the proposed work is about <64 which is less than of existing work. Here using the number of transistor are minimum to achieving the lower area overhead (less circuit complexity).

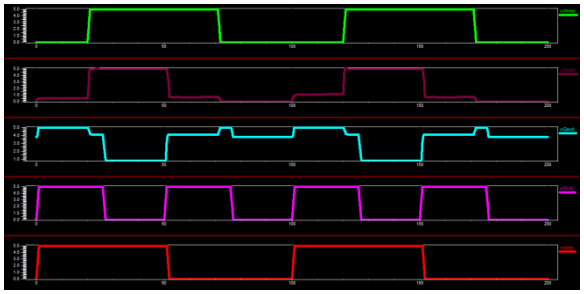

Fig3 Output Waveform

Table 1 power comparison of Flip-Flops

	Proposed System	Existing System
Lekage Power (active mode)(nw)	780	820
Lekage Power (standby mode)(nw)	0	0
Area (micro meter^2)	<64	78

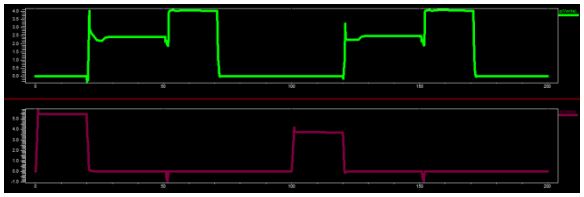

Fig4 Power Consumption Output Waveform

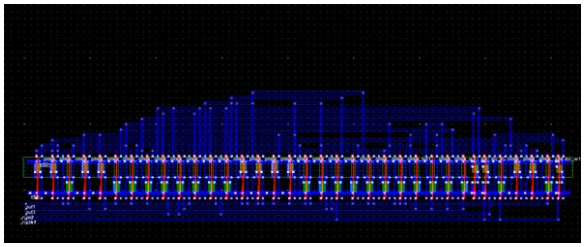

Fig 5 Layout Design

IV CONCLUSSION

In STTMRAM have one main disadvantage is high writeable energy is needed when we design of MFF. This writeable energy consumes more power hence high power consumption is occurring. The optimized design of Magnetic Flip-Flop is based on sleep transistor to reduce the power consumption. Another advantage of this technique as solves the long distortion problem during data transition and reduces the circuit complexity. For this design held in CMOS design methodology and used in Tanner

EDA as simulation tool to show the performance analysis. Then finally create the layout for overall proposed design using of T-Edit in TANNER EDA.

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