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Hybrid Converter Topology For Power Factor Correction In DC Drives Applications

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Abstract

This paper deals with a hybrid converter topology power factor correction (PFC) for DC drives which is fed through a diode bridge rectifier from a single phase AC mains. In this project both buck and boost converter topologies are combined together and operated alternatively according to the rectified DC input voltage level. DC drives are mostly operating with variable load and variable speed. So, active PFC method is suitable for DC drives fed from the AC supply. In active PFC method, the buck and boost converters are most popularly used. Both are having their own limitations. The limitations are eliminated in this paper by adding two auxiliary switches (one for buck operation and another one for boost operation) and two auxiliary diodes. In this paper buck PFC converter performance is improved by implementing constant ON-time control which is utilized to force it to operate in critical conduction mode (CCM). By selecting suitable control parameters, nearly unity power factor can be achieved within the nominal input voltage range. The proposed converter for drives is designed and modeled in MATLAB-2010-SIMULINK environment and its performance is evaluated. The simulated results are presented to demonstrate an improved power quality at AC mains of the DC drives system.

Index Terms— AC-DC, critical conduction mode (CCM), DC drives,

I. INTRODUCTION

A C to DC converter is an integral part of any power supply unit in all the electronic equipment and also used as an interface between the utility with most of the power electronic equipment. Generally to convert AC into DC, bridge rectifier is used. To

reduce the ripple in the DC output voltage, a large filter capacitor is used at the output side of the rectifier. This filter will reduce the input power factor and distort the input current waveform. In addition to the low power factor lower order harmonics influence the input supply waveforms.

To improve the power quality, various PFC schemes have been introduced. The various methods of power factor correction can be classified as:

1. Passive Power Factor Correction techniques
2. Active Power Factor Correction techniques.

In Passive Power Factor Correction techniques, an LC filter is inserted between the AC mains line and input port of the diode rectifier of AC/DC converter. It is illustrated in fig.1.

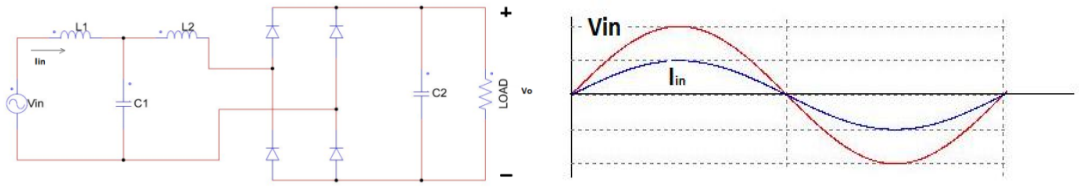

Fig.1. Passive PFC

Switched mode power supply (SMPS) technique is used to shape the input current in phase with input voltage (fig.1). There are different topologies for implementing Active Power Factor Correction techniques. Basically in this technique power factor correcting unit is used for tracking the input current in phase with the input voltage such that the input power factor comes up to unity. Active Power Factor Correction techniques have many advantages when compared with Passive Power Factor Correction techniques such as high power factor, reduced harmonics, smaller size and light weight.

The drawbacks of Active Power Factor Correction techniques are the complexity and relatively higher cost.

The active PFC techniques can be classified as

1. PWM power factor correction techniques.
2. Resonant power factor correction techniques
3. Soft switching PFC techniques

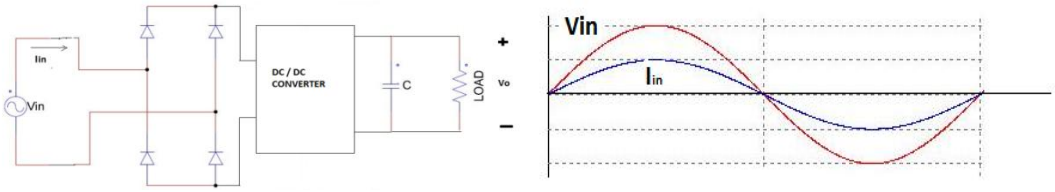

Fig. 2. Active PFC

In PWM technique, switching frequency of active power switch is constant but turn-on and turn –off mode is variable.

Different topologies of PWM techniques are

1. Buck type
2. Boost type
3. Cuk type
4. Fly-back type.

THE proposed PFC converter consists of both buck and boost configurations. This converter consists of two switches one for buck mode and the other one for boost mode. The boost converter is most popular topology for PFC applications due to its current wave shaping ability. But it has some limitations due to higher DC output voltage, high peak currents in the inductor and more conduction & switching losses. The power factor is high at high voltage gain in boost converter. So it is operated with large duty cycles.

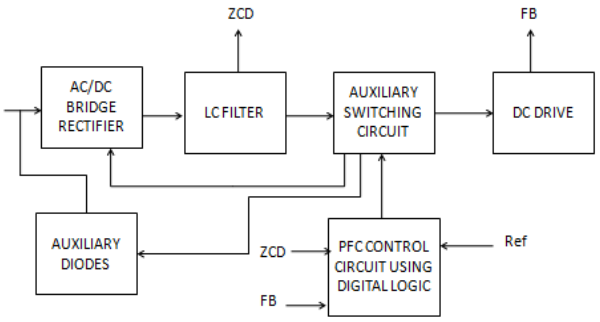

Fig. 3. Block diagram

The buck converter has some merits. The output voltage is regulated to a lower value than boost converter. The voltage stress across the switch is reduced. The large duty cycles will not allow the high inrush currents. Therefore, the efficiency of the buck converter is relatively high. In this proposed PFC converter the demerits in both buck and boost topologies are eliminated. The rectified output of the bridge converter is a positive sine wave i.e. the voltage increases from zero to maximum and again reduced to zero and so on. The input voltage is boosted up when the input voltage is less than a boundary level. If the input voltage increases the boundary level, then the buck converter is operated and the pulse to boost converter is not given.

II. PRINCIPLE OF OPERATION

A. Power Circuit

It consists of 4 power diodes and connected as a bridge formation. At positive half cycle diode D1 & D2 conduct and at negative half cycle diode D3 & D4 conduct. The output of bridge rectifier follows the sine wave for 0 to π radians and repeat again. So the output is unidirectional but has ripple content. The diodes are selected according to the maximum current flowing through them.

The filter consists of an inductor and a capacitor. The capacitor will improve the output voltage profile i.e. it will reduce the voltage ripples. The inductor is used to make the current continuous and as well as to provide the reactive power compensation which is drawn by the filter capacitor. The value of the capacitor and inductor is selected according to the type of converter topology and the loading capacity of the system.

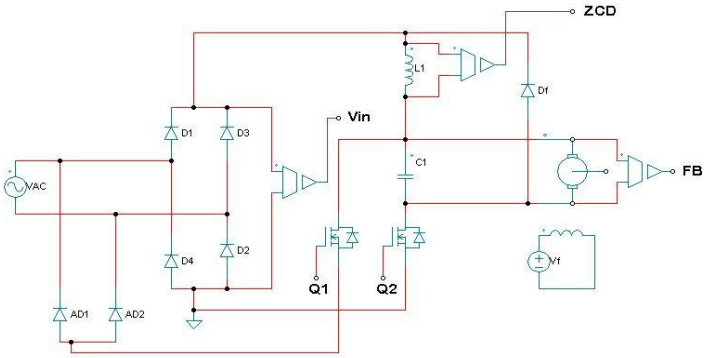

Fig. 4. Power Circuit

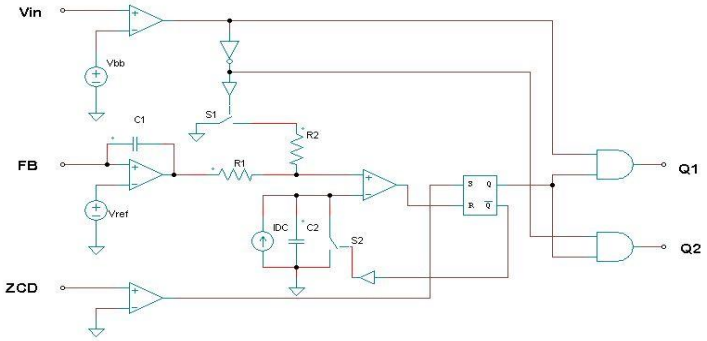

Fig. 5. PFC Control Circuit

The input power factor is improved by using two MOSFETs (Q_1, Q_2) and two diodes (D_5, D_6). Among the two switches one switch (Q_2) is connected in boost configuration and another switch (Q_1) is connected for buck configuration. The two diodes (D_5, D_6) are additional support to enhance the operation of the switches for input wave shaping.

B. PFC Control Circuit

The rectified voltage is compared with a reference voltage to turn-ON buck converter or boost converter (if rectified voltage is less than the ref. voltage then boost converter is operated, if rectified voltage is more than the ref. voltage then buck converter is operated.)

By using a zero crossing detector the zero current in the inductor is sensed and any one of the converters (buck / boost) is turned on according to the rectified voltage level.

Output voltage is fed back to the PFC control circuit to maintain within the limits.

The inductor voltage is sensed and feed to a Zero Crossing Detector. The ZCD sense the zero current occurrences and produce the pulse and it is given to a R-S flip-flop. Control pulses are generated by comparing the saw-tooth waveform with the square wave which is produced by the o/p voltage feedback signal and buck/boost mode selection signal with the help of a transistor and voltage divider. The 'Q' output of the flip-flop is given to the two AND gates which are used to select the buck or boost converter to operate.

The constant ON-time control is achieved with the help of an R-S flip flop. The pulse is maintained in high level up to the reset will become high.

III. SIMULATION AND RESULTS

The proposed circuit is constructed and simulated in MATLAB (2010a). The simulation diagram and simulated results are presented here.

The same DC motor is fed through ordinary bridge rectifier, buck PFC converter and boost PFC converter also for the performance comparison.

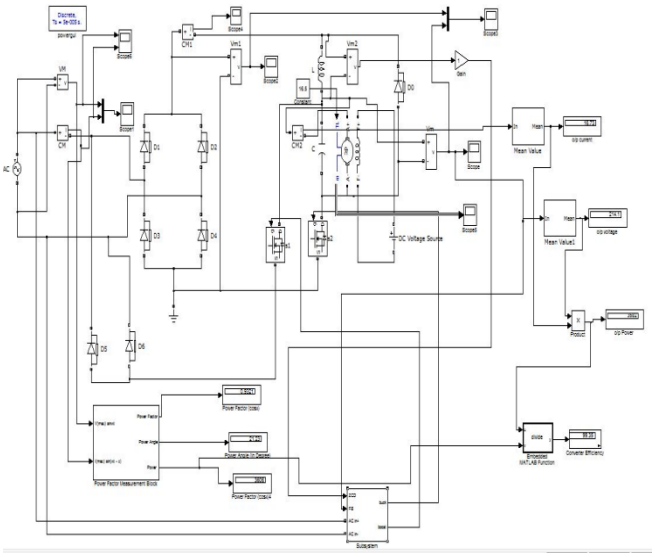

Fig.6. Power circuit simulation diagram in MATLAB

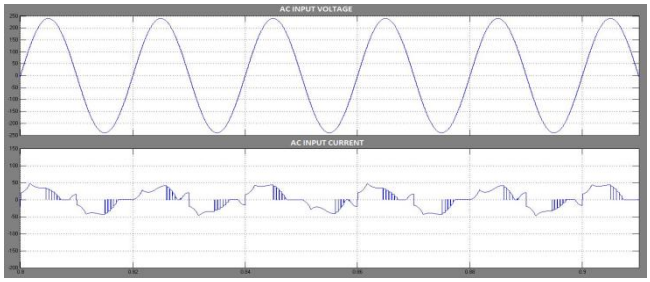

Fig.7. Input voltage and current wave form for 5Hp motor

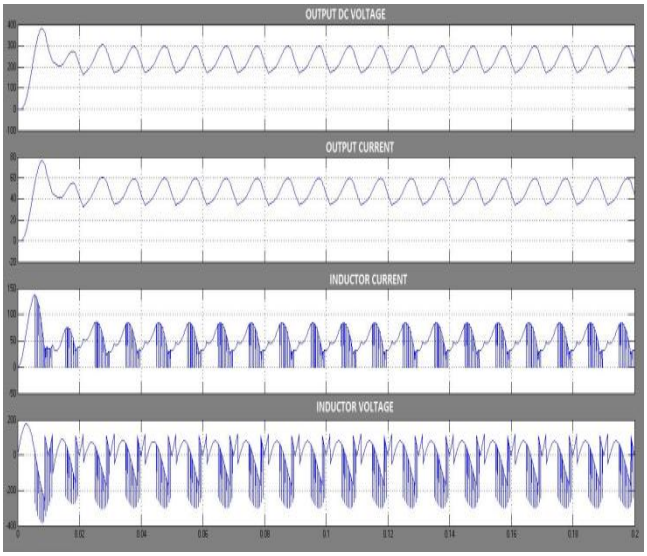

Fig.7. Output voltage & current, Inductor voltage & current wave form for 5Hp motor

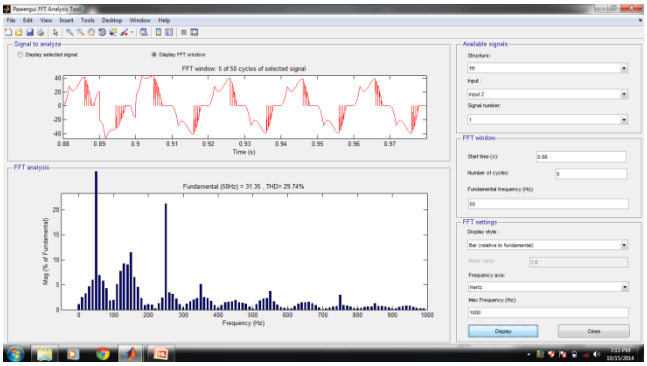

Fig.8. THD for 5Hp motor in MATLAB

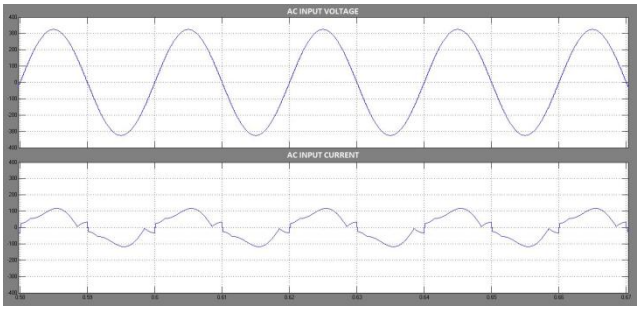

Fig.9. Input voltage and current wave form for 20Hp motor

The resistive load is connected in different topologies and the results are tabulated in the following table. The load resistance value is 5ohms.

Sl. No.	Converter	PF	THD (%)	Max. i/p current (A)	Load current (A)	η (%)
1	Bridge	0.855	31.80	85	48.06	94.5
2	Buck	0.901	47.42	47	40.28	97.12
3	Proposed	0.9503	32.74	82	48.73	99.1

The DC motor load is connected in different topologies and the results are tabulated in the table given below. For the first 3, the motor rating is 5HP and for 4th one is 20HP.

Sl. No.	Converter	PF	THD (%)	Max. i/p current (A)	Load current (A)	η (%)
1	Bridge	0.5911	104.21	100	17.87	99.1
2	Buck	0.8497	48.15	36	17.6	99.18
3	Proposed	0.9321	29.74	44	16.73	99.35
4	Proposed	0.9809	19.48	118	55.4	99.34

From the above table, it is understood that the proposed converter is more suitable for higher power ratings. The power factor improvement is satisfactory but the THD has be reduced. The peak current rating of the device is also reduced in the proposed converter topology. In an ordinary bridge rectifier, the peak current through the device in steady state is 5.6 times of the average DC load current. So, the device rating is selected to withstand the peak current. In the proposed converter the input peak current is reduced considerably to 2.63 times of the average DC load current. So, the diode and switch current rating is reduced and thereby the power loss in the device is reduced. It will improve the performance of the system.

In the proposed converter the THD has to be reduced. The work may be extended to reduce the THD value with in IEEE standards and also some modifications in design has to be done to make this work more worthy for low power ratings.

IV. CONCLUSION

The low Power factor in AC supply system will reduce the power system efficiency. The usage of converter will reduce the PF and produce harmonics in the supply current which will reduce power quality. To improve the power quality power factor correction & harmonics reduction is a challenging task to the electrical engineers. In this paper various methods to improve the power factor are analyzed and the proposed converter is designed and simulated.

From the study, it is concluded that the power factor can be improved in the proposed converter topology with resistive and DC motor loads. The control circuit is simple and cost effective. Moreover the THD has to be improved by making some modification in the design.

Future scope

Hardware implementation is to be carried out to confirm the simulation results.

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