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A Versatile FPGA based Commutation Sequence Generator for BLDC Motors

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Abstract

Recent trends in Radio Telescopes deploy BLDC motors for their 2-axis rotation. BLDC motors implement electronic commutation by avoiding carbon brushes and mechanical commutation. Resolvers mounted on rotor shaft of BLDC motors form good sensor feedback and work in-conjunction with RDC and FPGA interface to implement speed and position control. Brushes in DC torque form an important source of arcing and generation of considerable EMI interference noise. Such EMI interferences reduce the S/N of signals obtained from faint radio sources in Radio Telescope. Also BLDC motors gain importance as drive sources in focal plane instruments of Radio Telescopes, avoid brushes and uses electronic commutation. This approach helps in attaining enhanced sensitivity and S/N ratio. Complete FPGA based Sequence Generator is described here. FPGA based controller scheme used to provide stator voltage to BLDC motor, speed and position control of telescope. By avoiding brushes and arcing in mechanical commutation EMI interference is reduced. The focus motor of telescope gains an importance by providing better S/N from this approach. Complete hardware and software aspects of FPGA controller scheme for BLDC motor control is covered. FPGA accepts shaft position information from a syncro mounted on motor shaft and interfaced through RDC to FPGA.

Keywords: BLDC, DC, EMI, FPGA, MOSFET, PWM, RDC, VHDL.

Introduction

BLDC motors consist of a permanent magnet rotor with 3-phase stator windings. These motors are gaining more popularity compared to brush DC motors because of their superior performance [1]. The electronic commutation forms relevant features

like better speed versus torque characteristics, noiseless operation and high speed ranges. Resolvers are commonly used as position sensors on the motor shaft. The speed and position control of the telescopes which incorporate BLDC motors for their rotation have been described in this paper.

Fundamentally resolvers produce signals proportional to the sine and cosine of their rotor angles. A reference signal applied to the stator of the resolver and the two secondary rotor coils generate sine and cosine modulated signals of the reference wave. These sine and cosine modulated signals as shown in Fig.1 form input to a resolver to digital converter of analog devices. A ratio metric tracking convertor in AD2S83 generates the shaft angle in digital representation. Here we report a Xilinx based FPGA sequence generator, which enables the generation of 3-phase voltages that need to be supplied to the stator of BLDC motors, as a function of the resolver position.

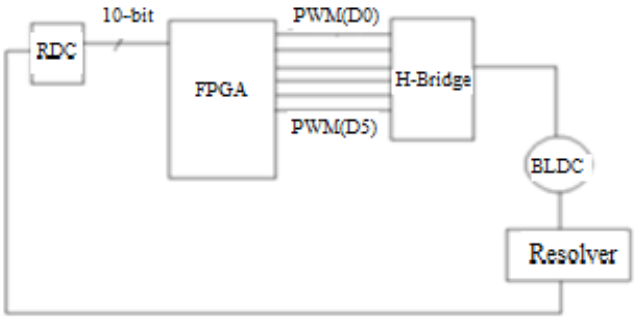

Figure 1: Hardware scheme of connection of BLDC, FPGA and H-Bridge

Winding Energizing Sequence with Reference to Resolver Position

BLDC motors have a 3-phase stator coil and a single/multi pole pair rotor. To rotate the BLDC motor, the stator windings should be energized in a particular sequence. In order to determine which winding will be energized, rotor position is sensed by using resolver mounted on the rotor. The shaft position obtained from RDC is converted to 6 states of commutation, with an increment of angles of 60 degrees. The stator energizing sequence is shown in Fig. 2 and the six states of energizing the stator coils are depicted in Table-1. Fig. 3 shows the coil excitation waveforms.

Table I : The Six States And Coil Current Directions

State	**A**	**B**	**C**
State 1	Positive	Nil	Negative
State 2	Positive	Negative	Nil
State 3	Nil	Negative	Positive
State 4	Negative	Nil	Positive
State 5	Negative	Positive	Nil
State 6	Nil	Positive	Negative

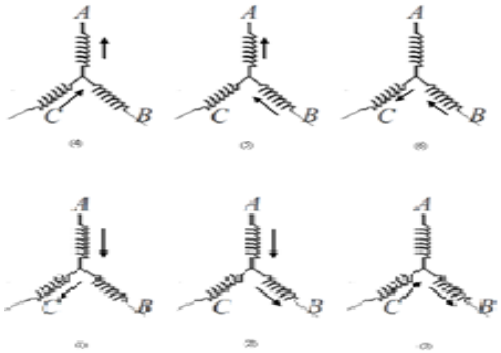

Figure 2: The sequence of energizing BLDC stator coils

The H-bridge arrangement of MOSFETs and the 3-phase stator coil connection is shown in Fig. 3.

H-Bridge Configuration with MOSFETS

The six states and the MOSFET 'on' transistors are shown in Table 2. The commutation pulses generated from FPGA are given to the 6 MOSFET gates as shown in Fig. 3. The bridge outputs as connected to the 3-phase BLDC stator coils A, B and C is also shown in the Fig. 3. FPGA port bit assignments are shown in Table 3.

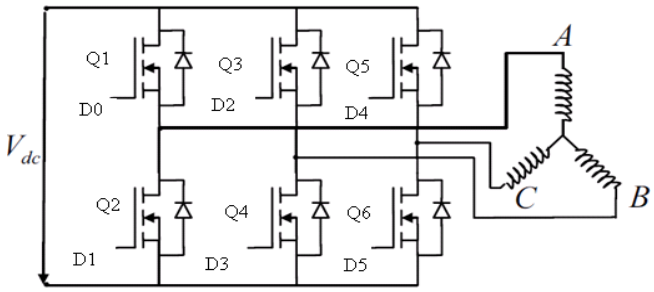

Figure 3: Three phase Inverter Bridge for BLDC driving

Table 2 : Active MOSFETS

State	Active MOSFETS
1	Q1,Q6
2	Q1,Q4
3	Q5,Q4
4	Q5,Q2
5	Q3,Q2
6	Q3,Q6

Table 3: Port Bit Assignments

Port bit	MOSFET
D0	Q1g
D1	Q2g
D2	Q3g
D3	Q4g
D4	Q5g
D5	Q6g

Table 4: Six States a Hex Control Codes

State	D5	D4	D3	D2	D1	D0	Hex Control Code
1	1	0	0	0	0	1	21
2	0	0	1	0	0	1	09
3	0	1	1	0	0	0	18
4	0	1	0	0	1	0	12
5	0	0	0	1	1	0	06
6	1	0	0	1	0	0	24

The 6 states and the hex control code for the H- Bridge are shown in Table 4.

Speed Control Scheme

The speed of the BLDC motor is determined similar to DC motors by the average voltage supplied to the motor coils. The timings of the six states need to follow that of DC motor. The relation between motor rpm, number of poles and frequency of the power supply is governed by:

$$N = 120*f/P$$

Where,
N - Rpm of the motor
f - Frequency of the stator power supply
P- Number of stator poles.
Frequency of output voltage is varied by changing the duration of the six state pulses.

A. BLDC Motor Speed-Controller

The speed controller obtains input from demanded speed. The speed of the motor is fed back and the difference between demanded speed and actual motor speed forms the error in speed. The speed of the motor is directly proportional to the supply voltage. The error in speed varies the average voltage sent to the motor.

B. BLDC Motor Position -Controller

The position of the motor is fed back and the difference between the demanded position and the actual position of the motor shaft represent the telescope position for that axis, which forms the error in position. This error is fed to the speed controller as input demand.

C. Current Controller

The difference in demanded current to the actual current drew by the motor forms the servo of the current loop. This error finally alters the PWM duty cycle to vary the average voltage applied to the motor, according to the demand in order to minimize the position and speed error.

D. Cascaded Controller

The outermost loop forms the position loop. The second stage is the speed loop and the inner most loop is the current/torque loop. The final error output determines the duty cycle of the PWM voltage generated as applied to the H-Bridge power supply.

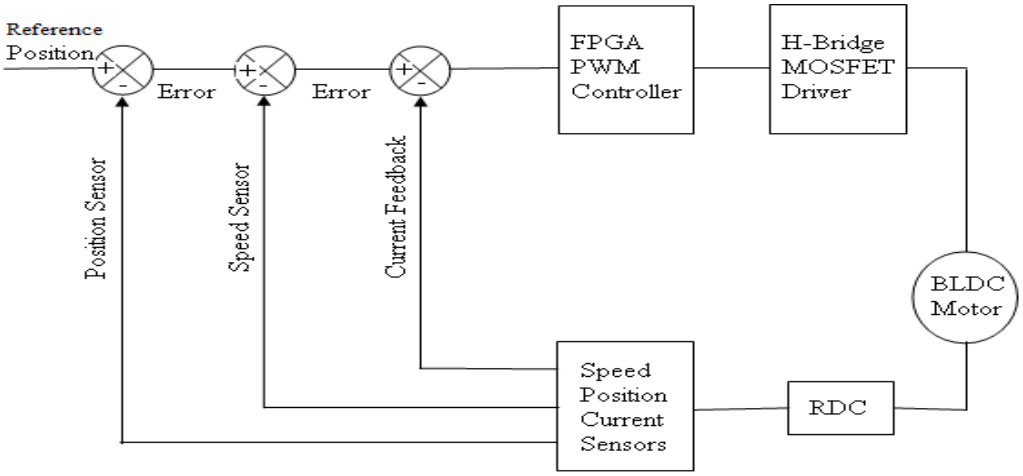

Figure 4: Cascade Feedback Control System

Hardware Implementation

FPGA receives resolver output from BLDC motor and generates the gate pulses which drive the MOSFET switches. In accordance with the required reference speed, a voltage is generated which is applied to the controller.

PWM technique is one of the most popular speed control techniques for BLDC motor. Here it is possible to adjust output voltage of inverter by controlling duty cycle of switching pulses of inverter [2]. The disadvantages of analog methods are that they are prone to noise and change with voltage and temperature. Also they suffer changes due to component variation [3]. Analog methods are less flexible as compared to digital methods. PWM signals are generated from the Spartan-3 processor by writing VHDL program to control the inverter switches.

As the motor rotates, resolver signals are produced in accordance with rotor position. Three phase voltages are produced from the gates of MOSFET switches after they receive the decoded signals from FPGA. These voltages are fed as input to the motor and it rotates. The digital controller works well with real motors.

The functionality of the various circuits of the BLDC motor was implemented using VHDL programming. These programs were simulated before FPGA implementation to verify the performance of the program. The VHDL code that imitates the functionality of the motor was downloaded into a Xilinx Spartan-3 FPGA. The Spartan-3 starter kit was used. These waveforms are observed in an oscilloscope.

Results

Conclusion

Implementation of commutation sequence generator for BLDC motor through FPGA is discussed. It is observed that FPGAs are more powerful than microcontrollers and work with complex algorithms with relative ease. The controller works well with BLDC motor. Using FPGAs gives us flexibility of implementing different algorithms quickly and without complications.

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