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Synchronization of Grid Voltage with Distributed Generation Systems under Unbalanced Situations by Fuzzy

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Abstract

The matrix association of appropriated era frameworks, basically wind and Photo voltaic (PV) frameworks are turning out to be extremely demanding. The transmission framework administrators (TSOs) are especially stressed over the low voltage ride through prerequisites (LVRT) by using fuzzy logic controller. Cures by establishment of STATCOMs and element voltage controllers (DVRs), disseminated era plants have propelled control capacities for existing force converters, To Improve their execution under defective and bended situations and, consequently, to satisfy these necessities. Keeping in mind the end goal to accomplish agreeable results with such frameworks, it is important to depend on precise and quick network voltage synchronization, which can work under unequal and twisted conditions. This paper examines the synchronization capacity of three propelled synchronization frameworks: the decoupled twofold synchronous reference outline stage bolted circle (DDSRFPLL), the double second request summed up integrator (DSOGIPLL), and the three stage improved (3PhEPLL), intended to work under such conditions. Here fuzzy logic is used for controlling compared to other controllers the MATLAB Systems tool has proved that the combined system will at the same time inject maximum power. PLLs have been picked because

of their connection with dq0 controllers so as to assess their precision and execution highlights.

Keywords: Electric variable measurements, electrical engineering, frequency estimation, frequency-locked loops, harmonic analysis, monitoring, synchronization.

I. INTRODUCTION

The force offer of renewable vitality based era frameworks should achieve 20% by 2030, where wind and Photo voltaic (PV) frameworks are thought to be the most exceptional case of reconciliation of such frameworks in the electrical system.

The expanded infiltration of these advancements in the electrical system has fortified the current worry among the transmission framework administrators (TSOs) about their impact in the network steadiness; as an outcome, the matrix association guidelines are turning out to be increasingly prohibitive for conveyance era frameworks in all nations.

In the real lattice code prerequisites (GCRs), unique requirements for the operation of such plants under matrix voltage deficiency conditions have picked up an incredible significance. These prerequisites decide the shortcoming limits among those through which a matrix associated era framework might stay associated with the system, offering ascend to particular voltage profiles that determine the profundity and freedom time of the voltage lists that they should withstand. Such prerequisites are known as low voltage ride through (LVRT) and are portrayed by a voltage versus time trademark. In spite of the fact that the LVRT prerequisites in the diverse principles are altogether different, the main issue that era frameworks must manage the cost of when a voltage hang happens is the impediment of their transient reaction, with a specific end goal to keep away from its defensive disengagement from the system.

Arrangements taking into account the improvement of assistant frameworks, for example, STATCOMs and element voltage controllers (DVRs), have assumed a conclusive part in upgrading the deficiency ride through (FRT) capacity of appropriated era frameworks. In like manner, propelled control functionalities for the force converters have likewise been proposed. Regardless, a quick location of the deficiency adds to enhancing the impacts of these arrangements; subsequently, the synchronization calculations are vital. In specific nations, the TSOs likewise give the dynamic/responsive force example to be infused into the system.

In this paper, three enhanced and propelled matrix synchronization frameworks are concentrated on and assessed: the decoupled twofold synchronous reference outline PLL (DDSRF PLL), the double second request summed up integrator PLL (DSOGI PLL), and the three-stage improved PLL (3phEPLL).

II. THREE GRID SYNCHRONIZING SYSTEMS

A number of the positive-arrangement recognition calculations depend on SRF PLLs. Regardless of having a decent reaction under adjusted conditions, their execution gets to be deficient in unequal broken networks (95% of cases), and their great operation is profoundly molded to the recurrence soundness, which is contradictory with the possibility of a powerful synchronization framework. Numerous creators have talked about various propelled models, which can conquer the issues of the traditional PLL, utilizing recurrence and sufficiency versatile structures which can manage uneven, broken, and symphonious contaminated matrices. In the system of these topologies, three PLL structures are assessed.

1. Decoupled Double Synchronous Reference Frame PLL

The DDSRF PLL was developed for improving the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counterclockwise and another one clockwise, in order to achieve an accurate detection of the positive and negative-sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF PLL is shown in Fig. 1.

Under unbalanced grid voltage condition, the fundamental positive-sequence voltage vector looks as a dc voltage on the dq^{+1}axes of the positive sequence SRF and as ac voltages at double the fundamental generation frequency on the dq^{-1} axes of the negative sequence synchronous reference frame.

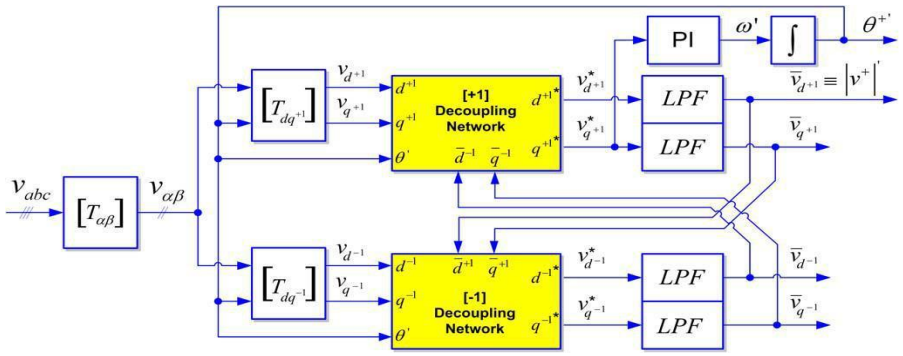

Fig.1. DDSRF-PLL block diagram.

In difference, the negative sequence voltage vector will cause a dc component on the negative sequence SRF and an AC oscillation on the positive sequence SRF. These dc components collect evidence about the amplitude and phase angle of the positive and negative sequence components of the grid voltage vector.

2. Duel Second Order Generalized Integration PLL

The working principle of the DSOGI PLL for assessing the positive and negative sequence components of the grid voltage vectors is based on using the instantaneous symmetrical method on the $\alpha\beta$ stationary reference frame. It can be observed that, the ISC method is applied by the positive sequence. To implement the ISC method, it is

necessary to have a set of signals, express the input voltage vector on the *αβ* stationary reference frame composed with additional set of signals, which are in quadrature and lagged with respect to $v_\alpha - v_\beta$.

In the DSOGI PLL, the signals to be delivered to the ISC method are achieved by using a dual second order generalized integrator (DSOGI), which is an adaptive band pass filter based on the generalized integrator. At its output, the DSOGI delivers four signals, namely, v'α and v'β, which are filtered versions of vα and vβ respectively, and qv'α and qv'β, which are the in quadrature versions of v'α and v'β.

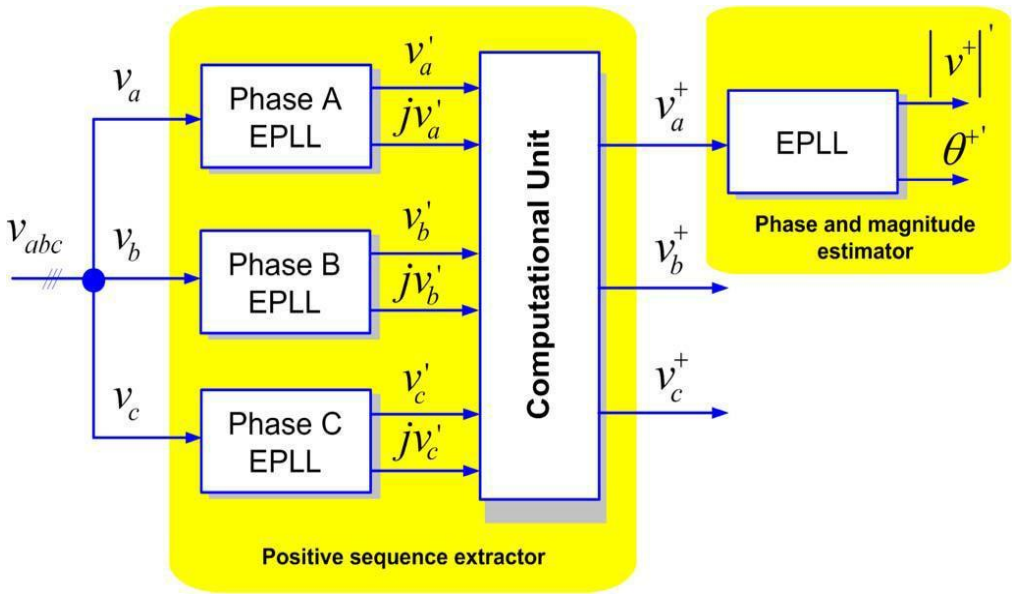

Fig.2.3 phEPLL block diagram.

A conventional synchronous reference frame PLL is applied on the estimated positive-sequence voltage vector, v'αβ, to create this synchronization system frequency adaptive. In particular, the v+αβ voltage vector is converted to the rotating SRF, and the signal on the q-axis, v+q, is applied at the input of the loop controller. As a concern, the fundamental grid frequency (ω') and the phase angle of the positive-sequence voltage vector (θ+')are estimated by this loop. The assessed frequency for the fundamental grid component is fed back to adapt the center frequency ω' of the DSOGI.

3. Three Phase Enhanced PLL

The enhanced phase-locked loop (EPLL) is a synchronization system that has verified to provide good response in single phase synchronization systems. An EPLL is basically an adaptive bandpass filter, which is able to adjust the cutoff frequency as a function of the input signal. Its configuration was later adapted for the three-phase order to sense the positive sequence vector of three-phase signals, obtaining the

3phEPLL that is represented in Fig. 2.
In this case, each phase voltage is processed individually by an EPLL. This block filters the input signal and generates two output sinusoidal signal having the same amplitude and frequency, $v'n$ and $jv'n$, the second one being 90◦ with respect to $v'n$. The output signals establish the input for the computational unit. Due to these in quadrature signals, using the ISC method the rapid positive sequence voltage component, *v+abc*, can be estimated.

III. DISCRETE IMPLEMENTATION

The performance of the different structures under test is really dependent on their final digital implementation, particularly on the discretization approach made to their continuous equations. This implementation is critical and should be studied in detail as a straightforward implementation can give rise to additional delays in the loop that hinder the good performance of the PLL.

A. DDSRF-PLL Discretization

The discrete model of this PLL can be easily obtained since the continuous representation of several parts does not change in the discrete domain. This is the case for the transformation blocks $T_{\alpha\beta}$, T_{dq}^{+1}, and T_{dq}^{-1}, whose description can be found in general scope literature.

1. Positive and Negative Sequence Decoupling Networks:

The decoupling network constitutes one of the most important contributions of this synchronization method. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain. It is just necessary to consider one sample delay of θ', vd'^{-1}, vq'^{-1} ,vd'^{+1}, and $v'q^{+1}$ in order to avoid algebraic loops.

2. Phase and Magnitude Estimator Discretization:

In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop. However, this does not affect the discretization of the phase and magnitude estimator since v^*_{d+1} and v^*_{q+1}.

$$\begin{bmatrix} v_{d+1}^{*}[n+1] \\ v_{q+1}^{*}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} \times \begin{bmatrix} v_{d-1}^{*}[n+1] \\ v_{q-1}^{*}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_{d-1}[n+1] \\ v_{q-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} \quad (1)$$

The discrete controller and the integrator can be built using a backward numerical approximation.

$$W'(z) = \frac{\left(k_p \pm k_i \ T_s\right) z - k_p}{z-1} \cdot V^*_{q+1}(z) + w_{ff}$$
$$\theta^{+'} = \frac{T_s z}{z-1} W'(z)$$

The frequency and phase can then be represented, considering v*q+1 as the error to be minimized. In this equation, a feed forward of the nominal frequency is given by means of ωff.

Finally, sample-based representation gives rise to (3), which are the expressions to be implemented

$$\begin{aligned} w'[n+1] &= w'[n] - k_p \ v^*_{q-1}[n+1] + \left(k_p + k_i \ T_s\right) v^*_{q-1}[n+1] \\ \theta^{+'}[n+1] &= \theta^{+'}_{s}[n] + T \ w'[n+1] \end{aligned} \tag{2}$$

In these equations, a frequency feed forward has been introduced as an initial condition to ω'.

3. LPF Block Discretization:

The amplitudes of the dq positive and negative sequence components are the outputs of the decoupling networks. However, four infinite impulse responses (IIR) LPFs extract the ripple from each sequence estimation in order to reinforce the performance of the PLL in case of harmonic pollution. A first order filter with a cutoff frequency ω_f, equal to half of the grid frequency; hence, the same transfer function has been implemented in this paper for evaluation purposes in

$$\begin{aligned} y[n] &= \frac{1}{T_s \ w_f + 1} \ x[n] + \frac{T_s \ w_f}{T_s \ w_f + 1} \ u[n] \\ x[n+1] &= y[n] \end{aligned} \tag{3}$$

B. DSOGI-PLL Discretization

1) DSOGI-QSG Block Discretization:

As was previously mentioned in Section II, the DSOGI-based quadrature signal generator (QSG) of Fig. 4 consists of two independent and decoupled second-order generalized integrators (SOGIs). Therefore, each SOGI based quadrature signal generator can be discretized individually, thus facilitating its mathematical description. In Fig. 7, the block diagram of the implemented SOGI is shown.

$$A = \begin{bmatrix} 0 & 1 \\ -w'^2 & -k w' \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ k w' \end{bmatrix} \quad C = \begin{bmatrix} 0 & 1 \\ w' & 0 \end{bmatrix} \quad x_n = A x_n + B v \quad y_n = C x_n$$
$$x_n = \begin{bmatrix} x \\ x_2 \end{bmatrix} \quad y_n = \begin{bmatrix} v' \\ qv' \end{bmatrix} \tag{4}$$

The discretization of this system has been performed using trapezoidal integrators, as they offer a better discovery of the phase, which is important when dealing with sinusoidal signals.

$$A' = \gamma \begin{bmatrix} 4 + 2T_s\, k\, w[n] - T_s^2\, w'[n]^2 & 4T_s \\ -4T_s\, w'[n] & 4 - 2T_s\, k\, w[n] - T_s^2\, w'[n]^2 \end{bmatrix}$$
$$B' = \gamma \begin{bmatrix} 2T_s\, k \\ 4k\, w'[n] \end{bmatrix}$$
$$C' = \gamma \begin{bmatrix} -2T_s^2\, k\, w'[n]^2 & 4T_s \\ 2T_s\, w'[n]\,(2 + T_s\, w'[n]) & 2T_s^2\, w'[n] \end{bmatrix}$$
$$D' = \gamma \begin{bmatrix} 2T_s\, k\, w'[n] \\ k\, T_s^2\, w'[n]^2 \end{bmatrix}$$
$$\gamma = \frac{1}{4 + 2T_s\, k\, w'[n] + T_s^2\, w'[n]^2} \tag{5}$$

In these matrices, *Ts* is the sampling time of the discrete system, $\omega'[n]$ is the estimated frequency magnitude, which comes from the estimation made at the SRF-PLL block at each computation step, and *k* is the SOGI gain.

$$x[n+1] = A' x[n] + B' v[n]$$
$$y[n] = C' x[n] + D' v[n] \tag{6}$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure.

The resulting discrete system is the best option as it reduces the need of using additional delays for breaking algebraic loops that appear using other methods which do not consider the SOGI QSG as a whole.

2) SRF PLL Discretization:

The frequency and phase detection is obtained by means of the SRF PLL shown in Fig. 8.

$$W'(z) = \frac{(k_p + k_i T_s) z - k_p}{z - 1} \cdot V_{q+1}^{*}(z) + w_{ff}$$

$$\theta^{+'} = \frac{T_s z}{z - 1} W'(z)$$

The discretization of the controller and the integrator is performed using the backward numerical approximation.

It can be noticed that the previous equations in (9) are equal to (2), as, in both cases, an SRF PLL is implemented. Likewise, the sample based representation of (9) can be written as shown in

$$w'[n+1] = w'[n] - k_p v_q^{*}{}_{-1}[n+1] + (k_p + k_i T_s$$

$$) v_q^{*}{}_{+1}[n+1] \; \theta^{+'}[n+1] = \theta^{+'}[n] + T_s w'[n+1]$$

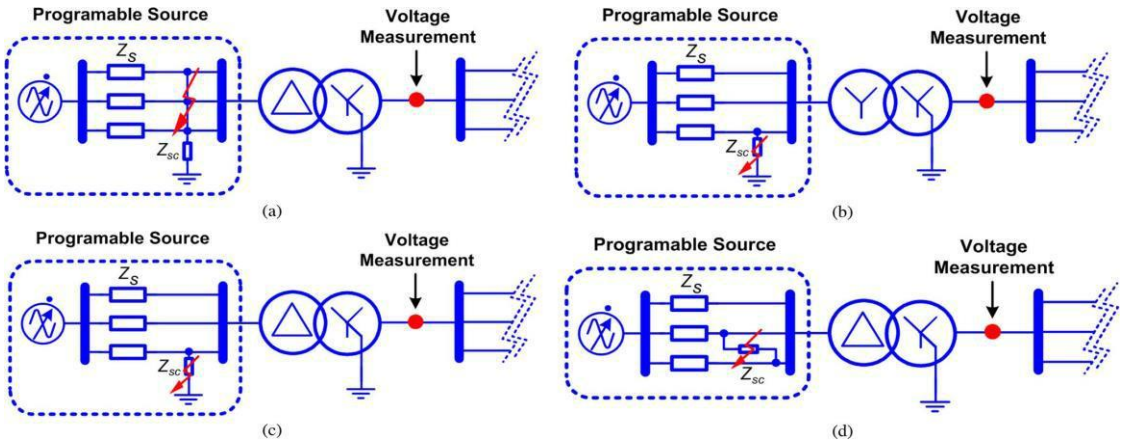

Fig.4. Generation of grid voltage sags in the experimental setup. (a) Generation of a Type “A” voltage sag. (b) Generation of a Type “B” voltage sag. (c) Generation of a Type “C” voltage sag. (d) Generation of a Type “D” voltage sag.

C. 3phEPLL Discretization

This three phase grid synchronization system activities the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three-phase voltages.

1) QSG Block—EPLL Discretization:

The block diagram of the EPLL implemented in this paper is presented in Fig. 9. According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in

$$A' = k\, e(t) \quad \cos\theta'(t)$$
$$w'(t) = -k_i \quad e(t) \sin\theta'(t)$$
$$\theta(t) = w'(t) + \frac{k_p}{k_i} w'(t)$$

The discrete state space variable representation was described by using a forward Euler approximation to reach satisfactory results; therefore, the same method has been implemented.

$$e[n+1] = u[n+1] - v'[n]$$
$$A'[n+1] = A'[n] + T_s\ k\, e[n]\ \cos(\theta'[n])$$
$$w'[n+1] = w'[n] - T_s\ k\, e[n]\ \sin(\theta'[n])$$
$$\theta'[n+1] = \theta'[n] + T_s\, w'[n] - T_s\ k_p\ e[n] \sin(\theta'[n])$$

Finally, after the state variables are calculated, the EPLL output can be obtained by (13), generating the two quadrature signals.

$$v'[n+1] = A'[n+1] \cos(\theta'[n+1])\ qv'[n$$
$$+1] = -A'[n+1] \sin(\theta'[n+1])$$

2) Computational Block Unit:
The description for this block is the same in both discrete and continuous domains.

3) Phase and Magnitude Detection Block:

$$v_a^+[n] = \frac{1}{3} v'_a[n] - \frac{1}{6}\left(v'_b[n] + v'_c[n]\right) + \frac{1}{2\sqrt{3}}\left(jv'_b[n] - jv'_c[n]\right)$$
$$v_c^+[n] = \frac{1}{3} v'_c[n] - \frac{1}{6}\left(v'_a[n] - v'_b[n]\right) + \frac{1}{2\sqrt{3}}\left(jv'_a[n] - jv'_b[n]\right)$$
$$v_b^+[n] = -\left(v_a^+[n] + v_c^+[n]\right)$$

This element is based on another EPLL, which is responsible for estimating the phase and the magnitude of the positive sequence fundamental component. Its discretization is equal.
However, for the phase and magnitude detection block, the outputs are the positive sequence magnitude and phase, which correspond directly with the states θ' and A', respectively.

IV. FUZZY LOGIC CONTROL

The Fuzzy logic control consists of set of linguistic variables. Here the PI controller is replaced with Fuzzy Logic Control. The mathematical modeling is not required in FLC. FLC consists of

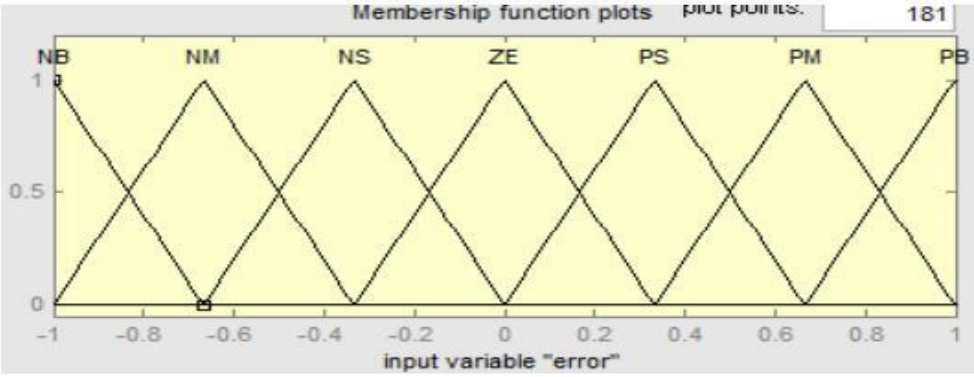

Fig.5. Membership functions

1. Fuzzification

Membership function values are assigned to linguistic variables. In this scaling factor is between 1 and -1.

2. Inference Method

There are several composition methods such as Max-Min and Max-Dot have been proposed and Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator.

3. Defuzzificaion

A plant requires non fuzzy values to control, so Defuzzificaion is used. The output of FLC controls the switch in the inverter. To control these parameters they are sensed and compared with the reference values. To obtain this the membership functions of fuzzy controller. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output.

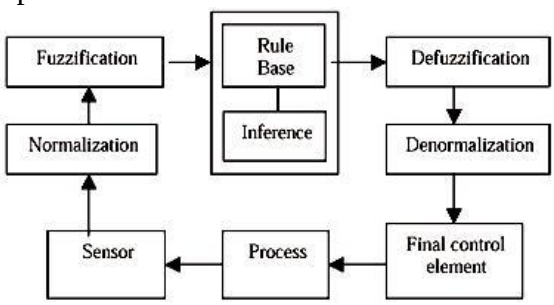

Fig.6: Fuzzy logic Controller

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C]$$

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

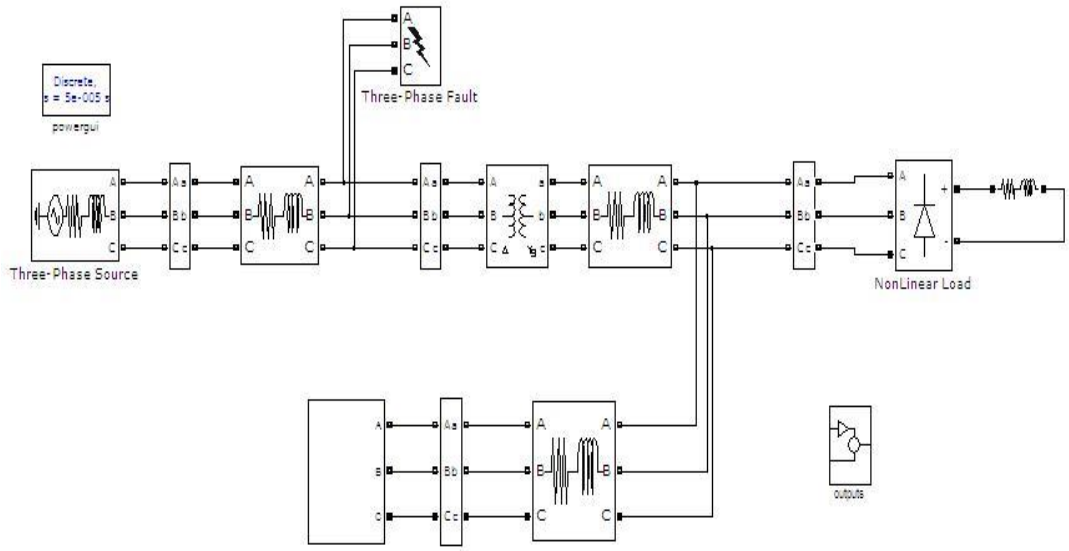

Fig.7 shows the common programable source for Decoupled double synchronus reference frame phase locked loop (DDSRFPLL), Duel second order gendralized integration phase locked loop (DSOGIPLL) and Three phase enhanced phase locked loop(3PEPLL).

V. TESTING IN SIMULATION

The results show that accurate synchronization is possible by using three grid synchronizing systems and also the response is very fast, where the three phase voltage waveforms experience transients due to the appearance of voltage sags, frequency variations, and harmonic pollution.

A. Behavior in Case of Voltage Sags

1) Type "A" Sag Test:

This kind of voltage sag appears as a consequence of three-phase faults that give rise to high short circuit currents and, hence, to a balanced voltage drop in the network. As Fig. 9 shows, the DDSRF PLL and the DSOGI PLL produce a good response, as both systems achieve a very fast detection (20ms) of the positive-sequence components (less than two cycles). The response of the 3phEPLL, depicted in Fig. 9(m), also shows a good response, but with a larger transient in the positive-sequence estimation.

2) Type "B" Sag Test:

This kind of fault permits the behavior of the PLLs under test in the presence of zero sequence components at the input. The Clarke transformation used in DSOGI PLL and DDSRF PLL to extract the $\alpha\beta$ components enhances the response of this synchronization system when the faulty grid voltage presents zero-sequence components. Their responses, as shown in Fig. 9, are fast and accurate.

B. Frequency Changes (50–60 Hz)

These results are obtained with the DDSRF and the DSOGI PLL, as can be seen in Fig. 10(a)–(d).

The low overshooting in the amplitude estimation in both cases [see Fig. 10(a) and (c)] assists the good phase and frequency detection, as shown in Fig. 10(b) and (d). Likewise, the response of the 3phEPLL shows a similar settling time, as shown in Fig. 10(e); however, the initial oscillation in the amplitude estimation of the voltage contributes to slightly delay the stabilization of the frequency magnitude, as displayed in Fig. 10(f).

***C. Polluted Grids* (*THD* = 5%)**

The 3phEPLL behaves as a band pass filter for the input signal, something that permits filtering the input without adding extra filters. As can be seen in Fig. 11, the 3phEPLL offers the best filtering capability among the PLLs under test by fuzzy logic controller, with a clear and undistorted estimation of the magnitude and phase of the input.

The response of the DDSRF PLL, depicted in Fig. 11, which has a first-order filter at the output, is even better than the one provided by the DSOGI PLL, due to the latter's low pass filtering behavior. Although the DSOGI PLL also behaves as well as a band pass filter, the tuning of its parameters, which permits a faster stabilization of the estimated signal in the previous tests, plays against its immunity in front of harmonics, as shown in Fig. 11, giving rise to small oscillations in the positive sequence estimation by fuzzy.

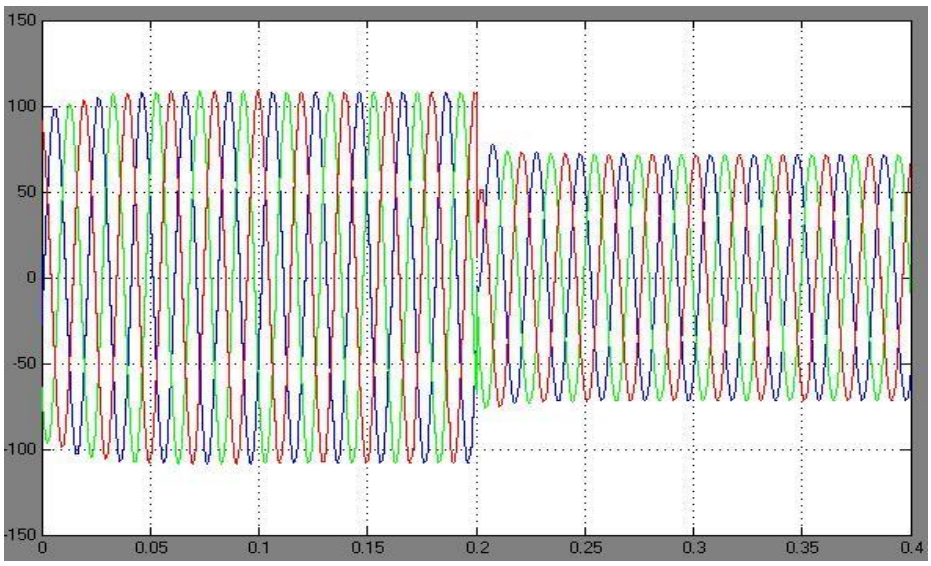

Fig.9 (a) Three phase faults

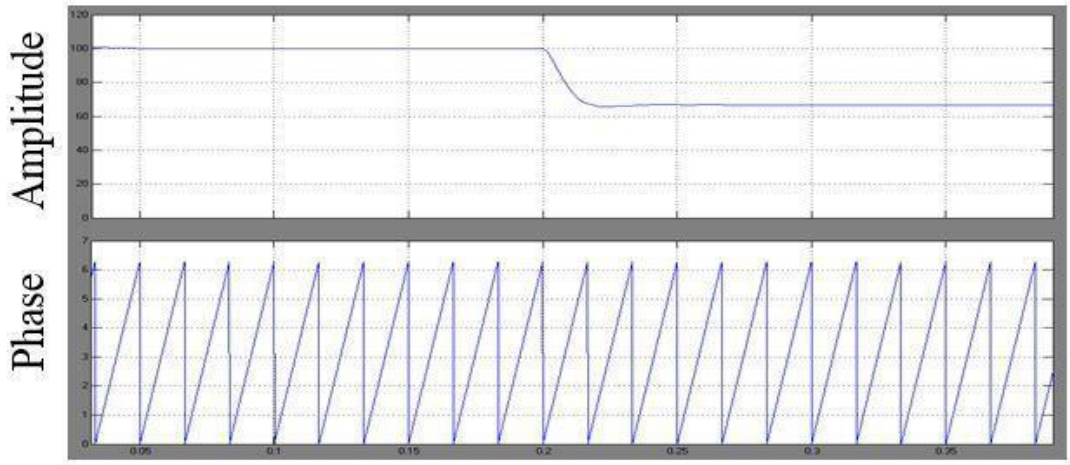

Fig.9 (b) Amplitude and phase detection for DDSRFPLL

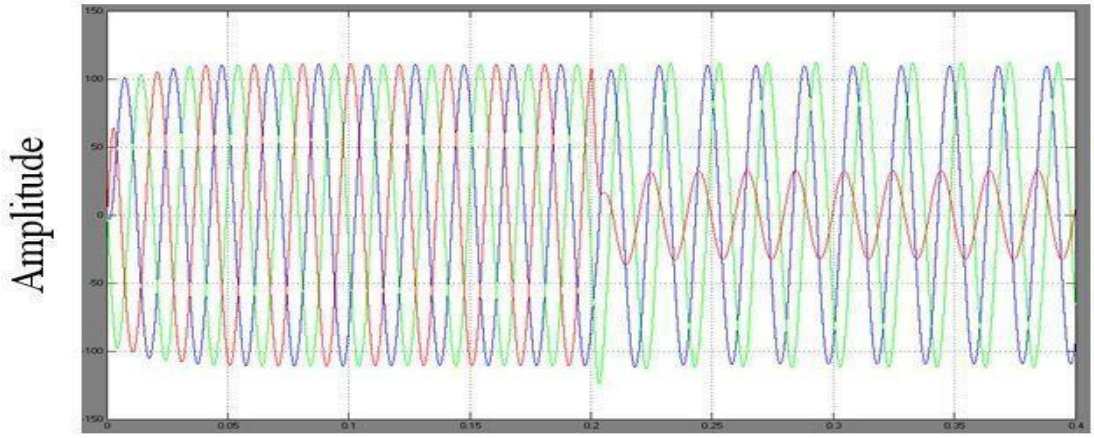

Fig.9(c) Double line to ground fault

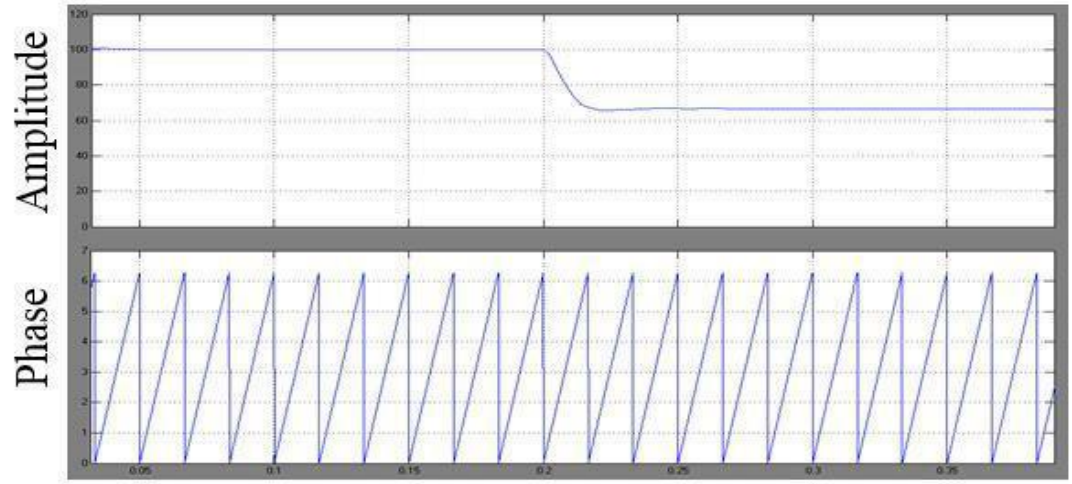

Fig.9 (d) Amplitude and phase detection DSOGIPLL

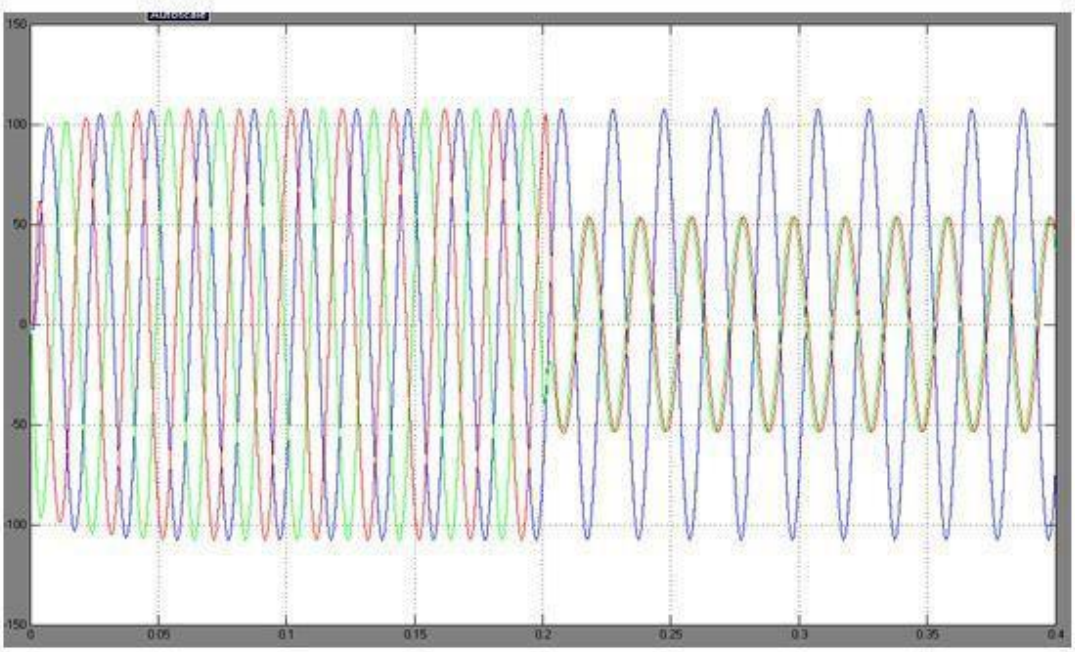

Fig.9 (e) Double line to ground fault

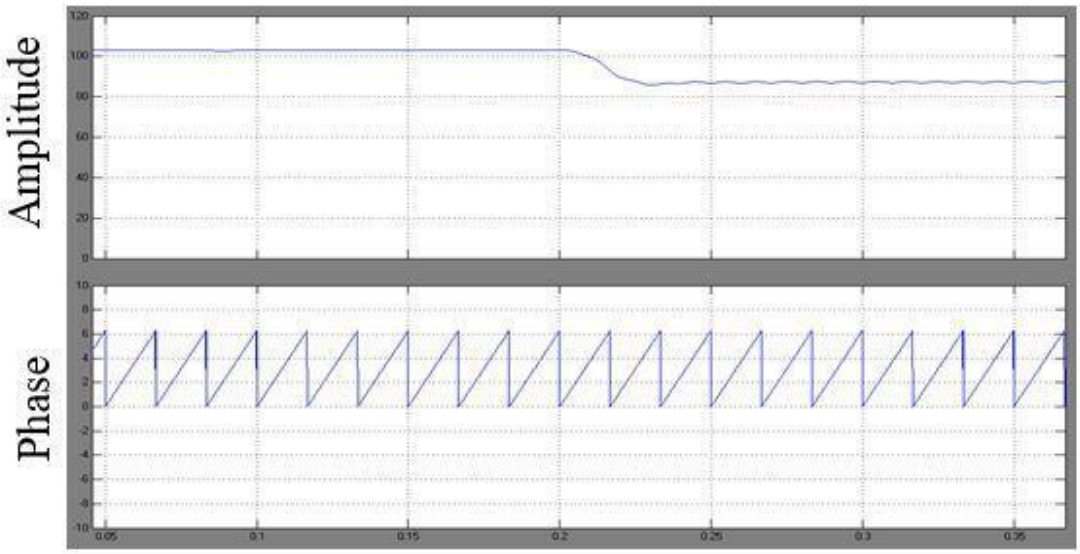

Fig.9 (f) Amplitude and phase detection for 3PEPLL

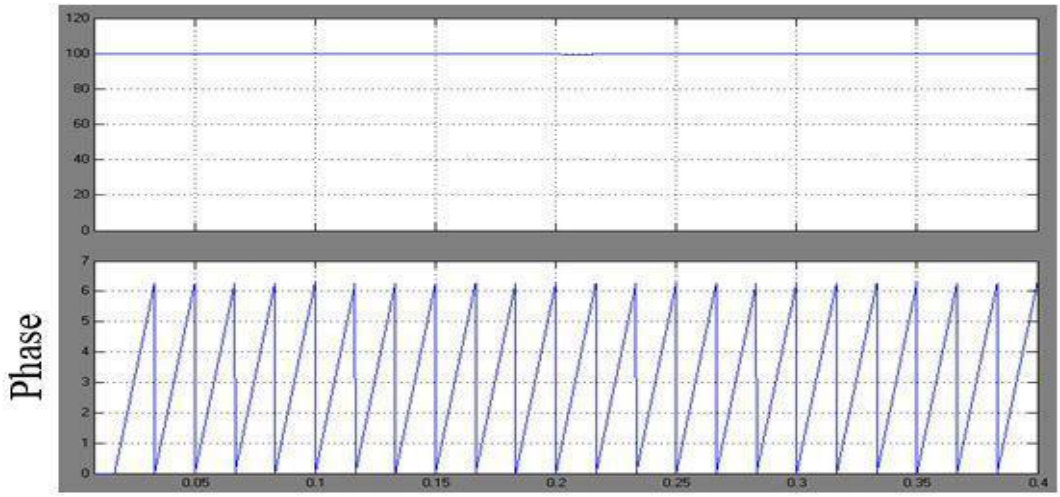

Fig.10 (a) Frequency jump for DDSRFEPLL

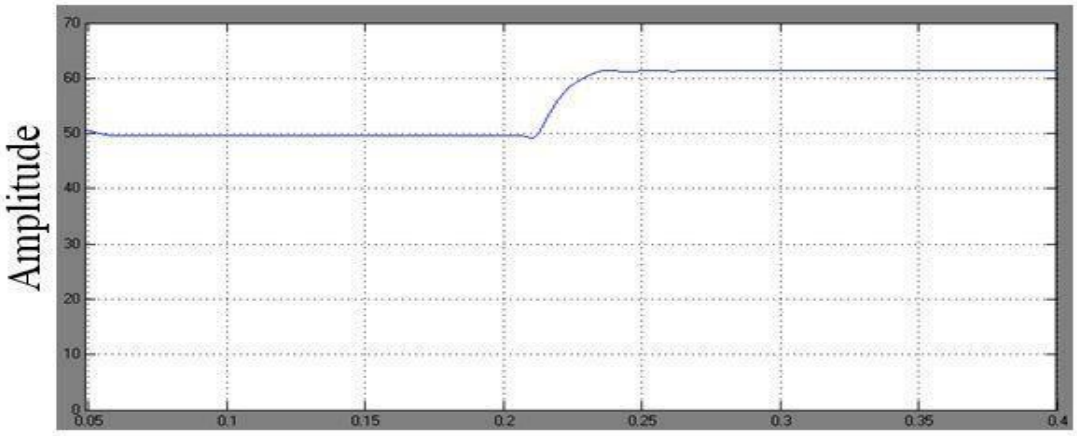

Fig.10 (b) Frequency detection for DDSRFEPLL

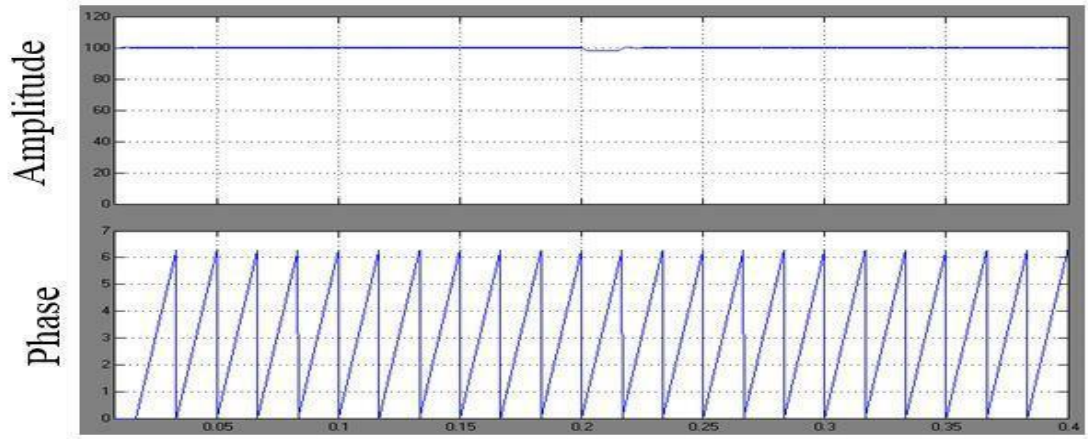

Fig.10 (c) Amplitude and phase for frequency jump DSOGIEPLL

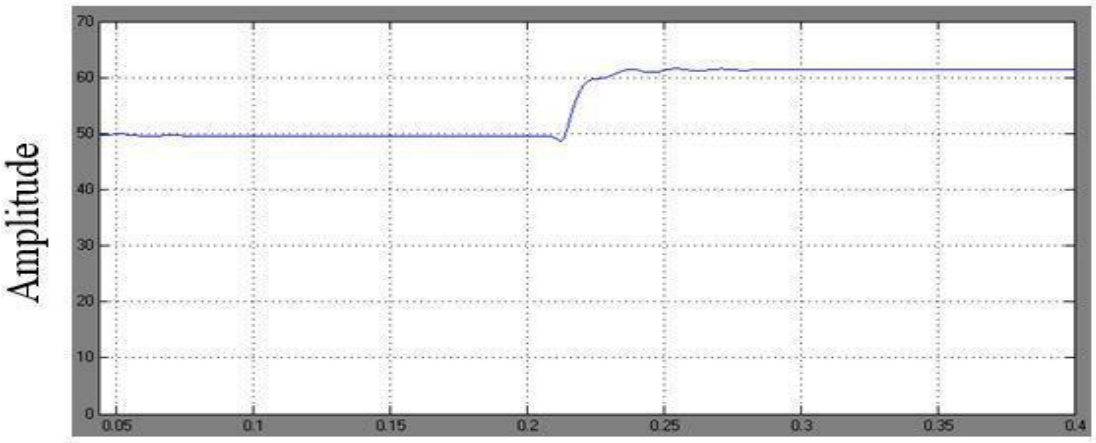

Fig.10(d) Frequency detection for DSOGI

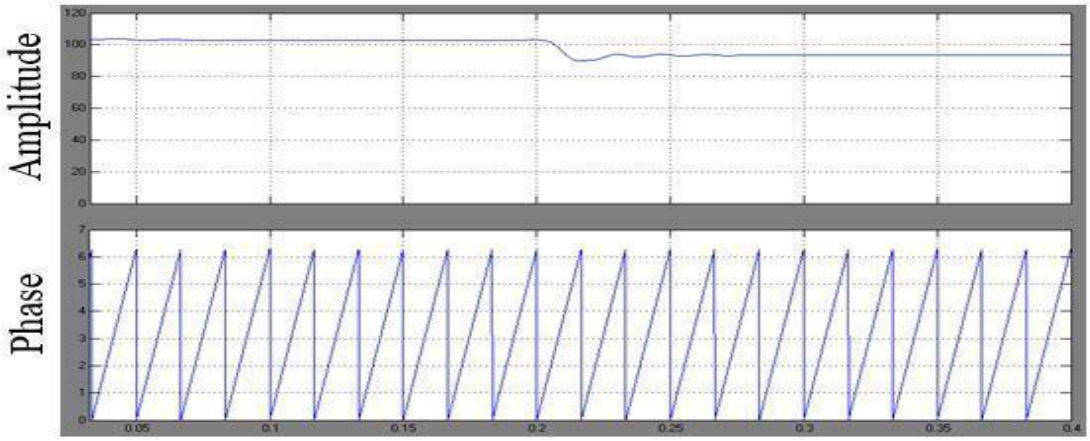

Fig.10(e) Amplitude and phase detection for 3EPLL

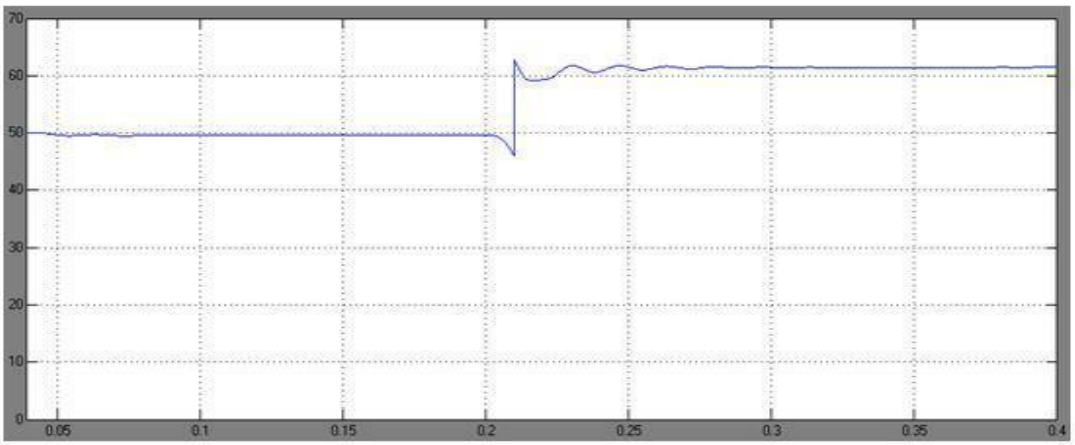

Fig.10 (f) Frequency detection for 3EPLL

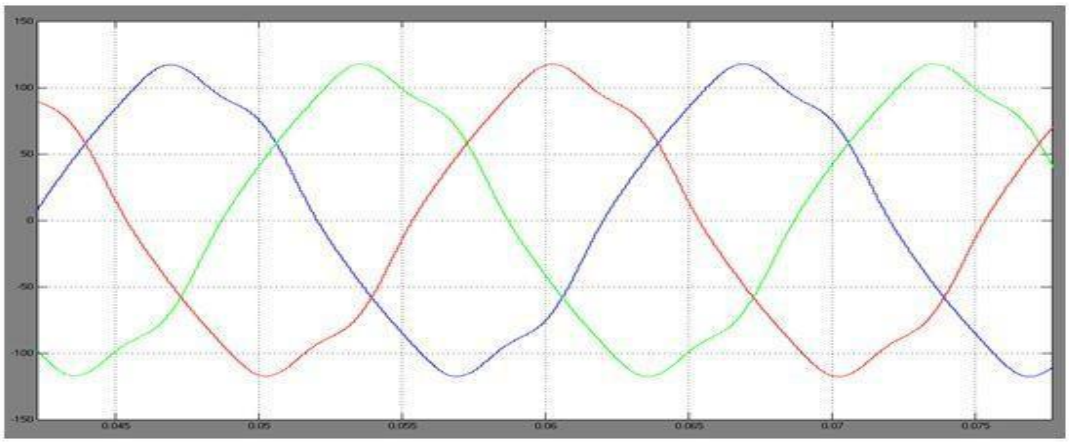

Fig.11(a) Polluted grid input

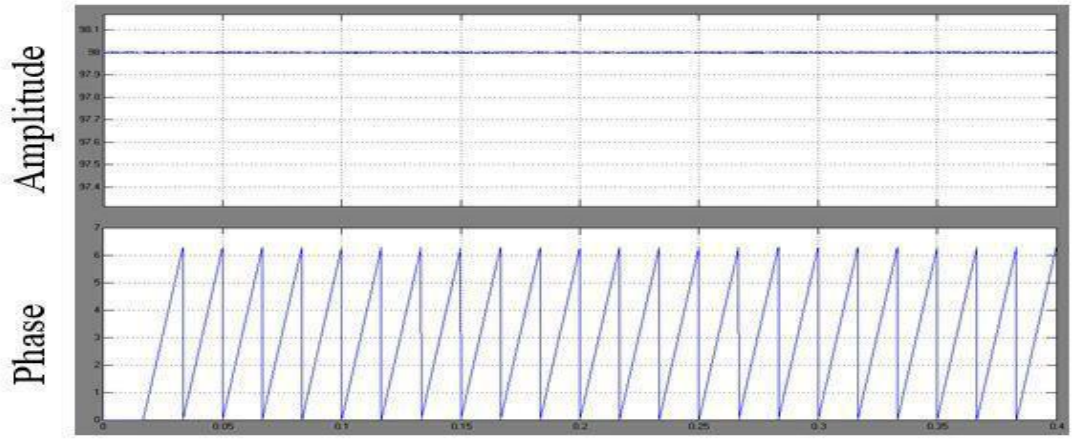

Fig.11 (b) Amplitude and phase for DDSRFPLL

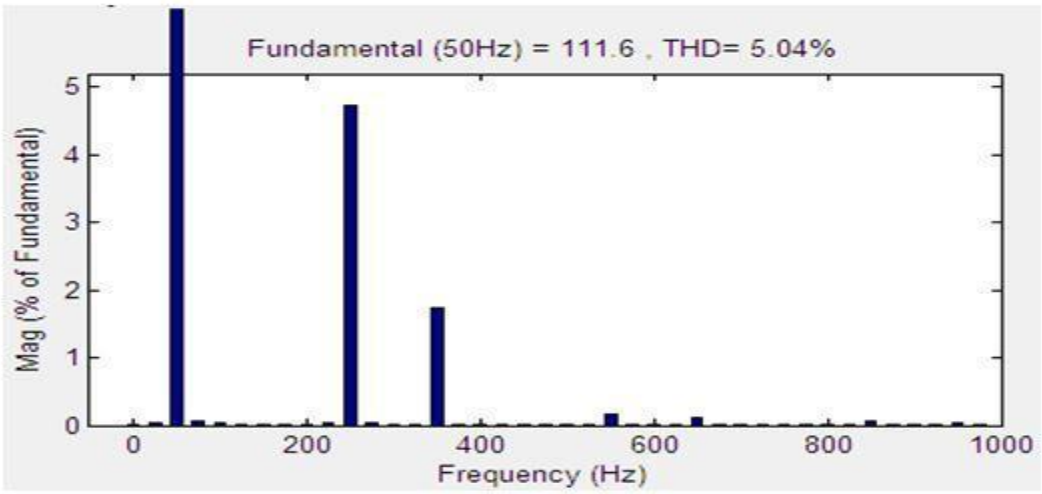

Fig.11(c) THD for DDSRFPLL

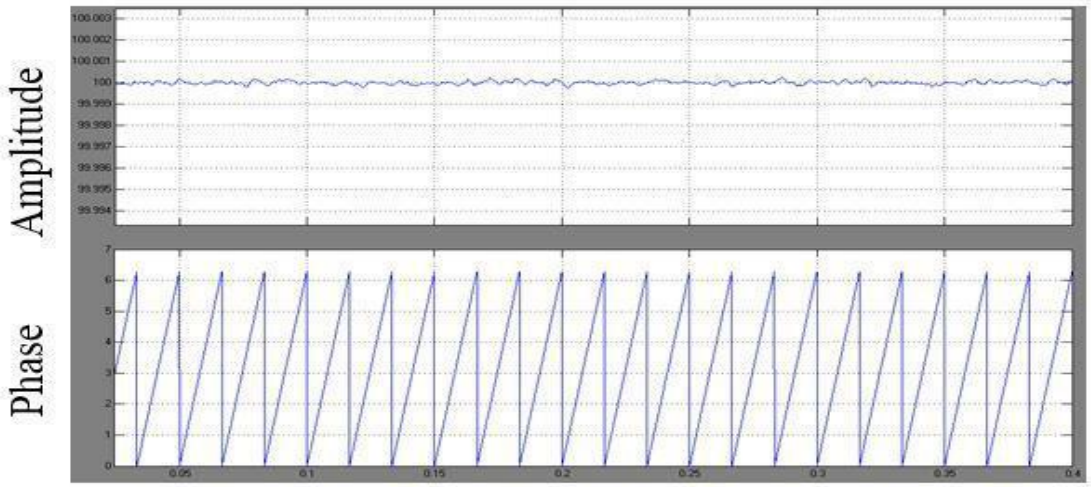

Fig.11(d) Amplitude and phase for DSOGIPLL

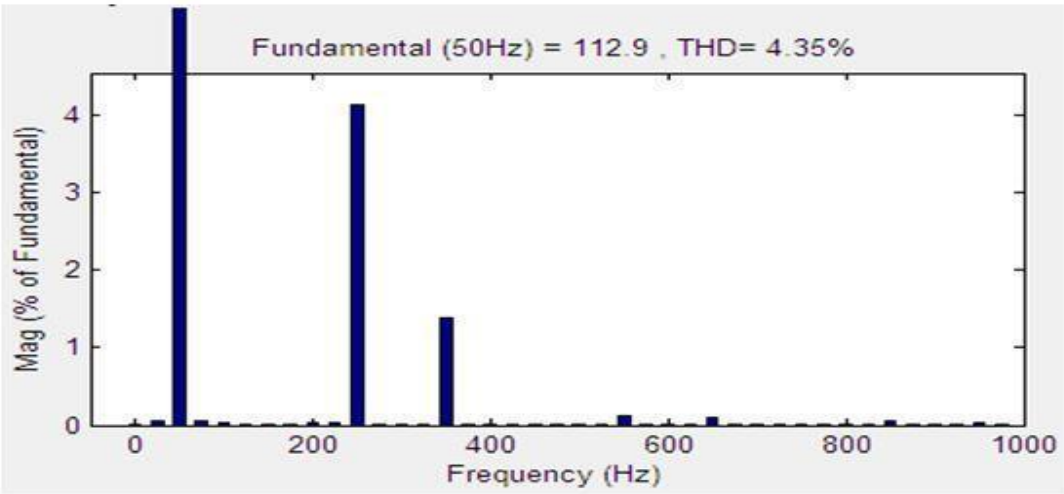

Fig.11 (e) THD for DSOGIPLL

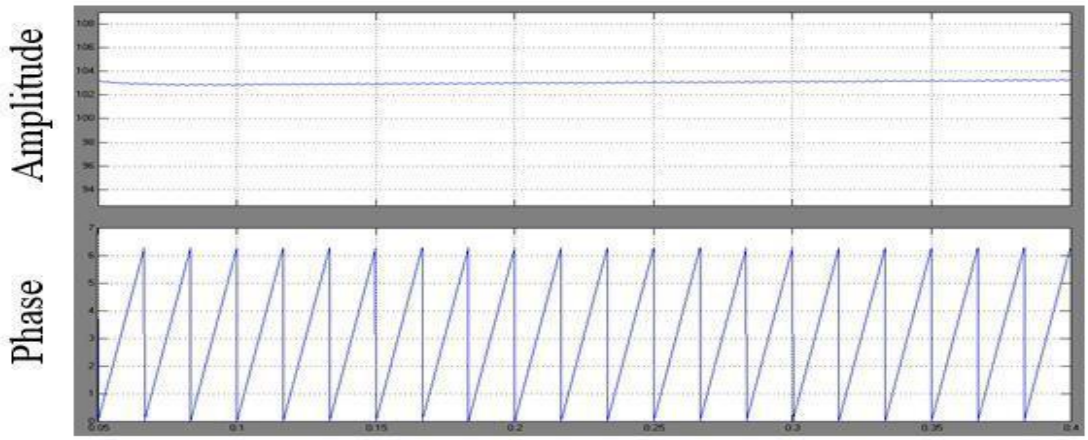

Fig.11(f) Amplitude and phase for 3EPLL

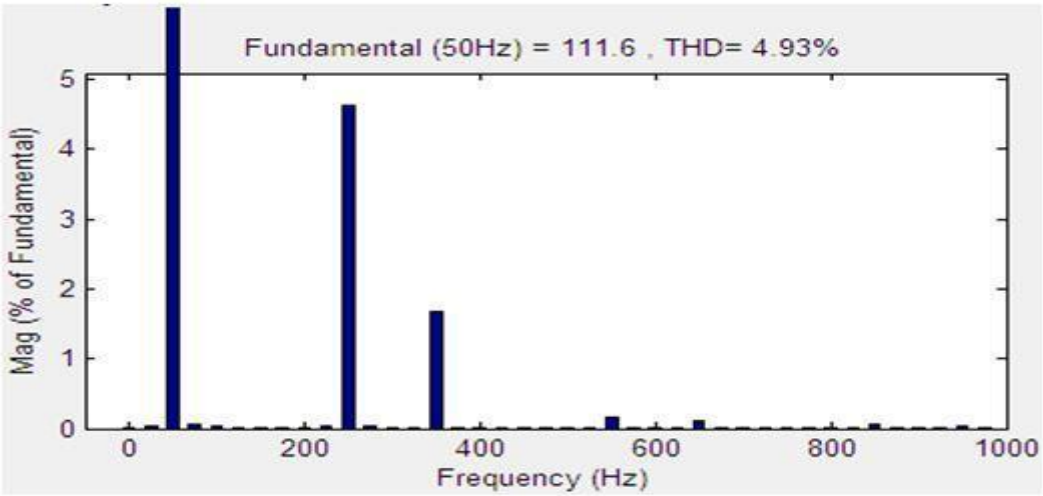

Fig.11(g) THD for 3PEPLL

VI. CONCLUSION

The behavior of three advanced grid synchronization system(GSS). Each structures are presented, and their Performance are explained. Moreover, their performances are shown in the simulation results, allowing a satisfactory response under balanced and distorted Grid Conditions (GC). The DDSRF PLL and the DSOGI PLL system working in the αβ reference frame, while the 3phEPLL uses the "abc" reference frame, thus working with three variables. As has been shown, this feature simplifies the DSOGI PLL and the DDSRF PLL structures, they reducing the computational burden, as compared to the 3phEPLL, without affecting its performance.

The synchronization capability is fast and accurate under faulty scenarios in all cases. However, the simpler structure of the DDSRF and the DSOGI affords an easier tuning of their control parameters and, therefore, a more accurate control of their transient response. The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater band pass and low-pass filtering capabilities. Although the DSOGI also gives rise to reasonably good results, due to its inherent band pass filtering structure, its response is more affected by harmonics. The lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters, offers a better tradeoff between the presented systems, making them particularly suitable for wind power applications.

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