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Modeling Techniques for MMC Employed on VSC-HVDC Schemes

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Abstract

Modular multilevel converters (MMC) are presently the converter topology of choice for voltage-source converter high-voltage direct-current transmission schemes due to their very high efficiency. These converters are complex, yet fast and detailed electromagnetic transients simulation models are necessary for the research and development of these transmission schemes. Excellent work has been done in this area, though little objective comparison of the models proposed has yet been undertaken. This paper compares for the first time, the three leading techniques for producing detailed MMC VSC-HVDC models in terms of their accuracy and simulation speed for several typical simulation cases.

Keywords: Accelerated model, electromagnetic transient (EMT) simulation, HVDC transmission, modular multilevel converter (MMC), voltage-source converter (VSC).

I. INTRODUCTION

The interest for voltage-source converter (VSC) high voltage direct-present (HVDC) transmission plans has become fundamentally lately. This development is essentially because of the upgrades in the voltage and force appraisals of protected door bipolar

transistors (IGBTs) and various new VSC-HVDC applications, for example, the association of vast seaward wind ranches.

Since its origin in 1997 and until 2010, all VSC HVDC plans utilized a few level VSCs. In 2010, the Trans Bay Cable Project turned into the primary VSC-HVDC plan to utilize particular multilevel converter (MMC) innovation. The MMC has various advantages in contrast with a few level VSCs; boss among these is lessened converter misfortunes. Today, the three biggest HVDC makers offer a VSC-HVDC arrangement which depends on multilevel converter innovation.

The target of this paper is to play out a truly necessary free correlation of the TDM, DEM, and AM models which will empower the perused to settle on a more educated choice while selecting which kind of nitty-gritty MMC model to utilize and to have a more noteworthy level of trust in the MMC models' execution. In this paper, the TDM, DEM, and AM models are implicit the same programming on the same PC and looked at as far as their precision and reenactment speed.

II. MMC VSC-HVDC

The essential structure of a MMC is appeared in Fig. 1. Every leg of the converter comprises of two converter arms which contain various sub modules, SMs, and a reactor Larm, associated in arrangement. The SM contains a two-level half-connect converter with two IGBT's and a parallel capacitor. The SM is likewise outfitted with a detour switch to expel the SM from the circuit if an IGBT fizzles and a thyristor to shield the lower diode from over current on account of a dc-side issue. The detour switch and thyristor are, be that as it may, ordinarily discarded from consistent state and transient studies.

The SM terminal voltage is adequately equivalent to the SM capacitor voltage when the upper IGBT is exchanged on and the lower IGBT is exchanged off; the capacitor will charge or release contingent on the arm current course. The upper IGBT exchanged off, and the lower IGBT exchanged on, the SM capacitor is avoided and, subsequently, is adequately 0 V.

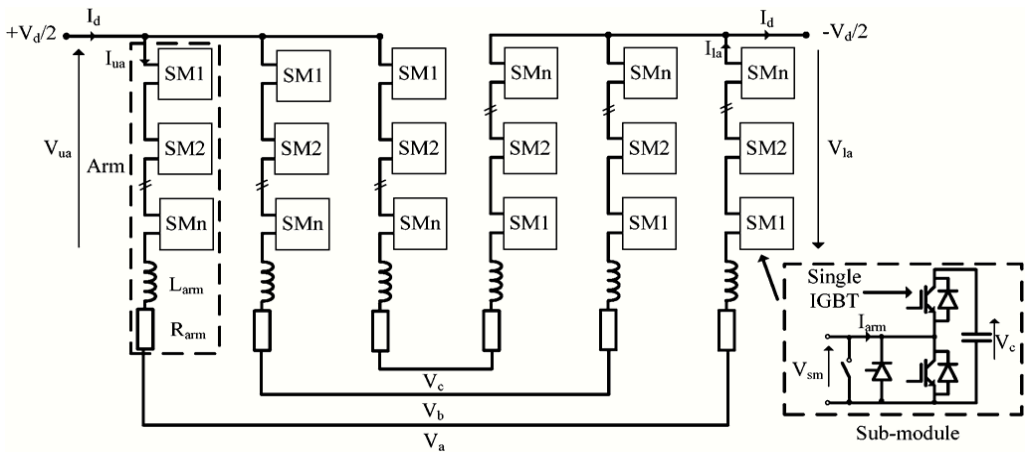

Fig.1: Three-phase MMC

III. DETAILED MMC MODELING TECHNIQUES

This section describes three detailed modeling techniques which represent the converter's IGBTs and diodes using a simple two-state resistance.

A. Traditional Detailed Model

In a traditional detailed MMC model, each SM's IGBTs, diodes, and capacitors are built in the simulation graphical user interface, and electrical connections are made between the SMs in each arm as shown in Fig. 1. This is the standard way of building a detailed MMC model so this type of model is referred to as the traditional detailed model (TDM). This method of modeling is intuitive and gives the user access to the individual components in each SM; however, for MMCs with a large number of SMs, this method is very computationally inefficient.

B. Detailed Equivalent Model

The DEM uses the method of nested fast and simultaneous solution (NFSS). The NFSS approach partitions the network into small subnetworks, and solves the admittance matrix for each network separately. Although this increases thenumber of steps to the solution, the size of admittance matricesis smaller, which can lead to reduced simulation time. A summaryof the DEM is presented in the Appendix; however, further information can be found in. The DEM employed in thiscomparison was obtained directly from PSCAD.

C. Accelerated Model

The accelerated model (AM) was proposed by Xu*etal.*In many respects, the AM is a hybrid between the TDM and the DEM. The user is able to access the SM components, as they can with the TDM, but the converter arm is modeled as a controllable voltage source, which is similar to the DEM. In the AM, the series-connected SMs are removed from each converter arm, separated and driven by a current source with a value equal to the arm current. A controllable voltage source is installed in place of the SMs as shown in Fig. 2.This model was found to offer greater computational efficiency than a TDM.It gives the user access to the individual converter components.

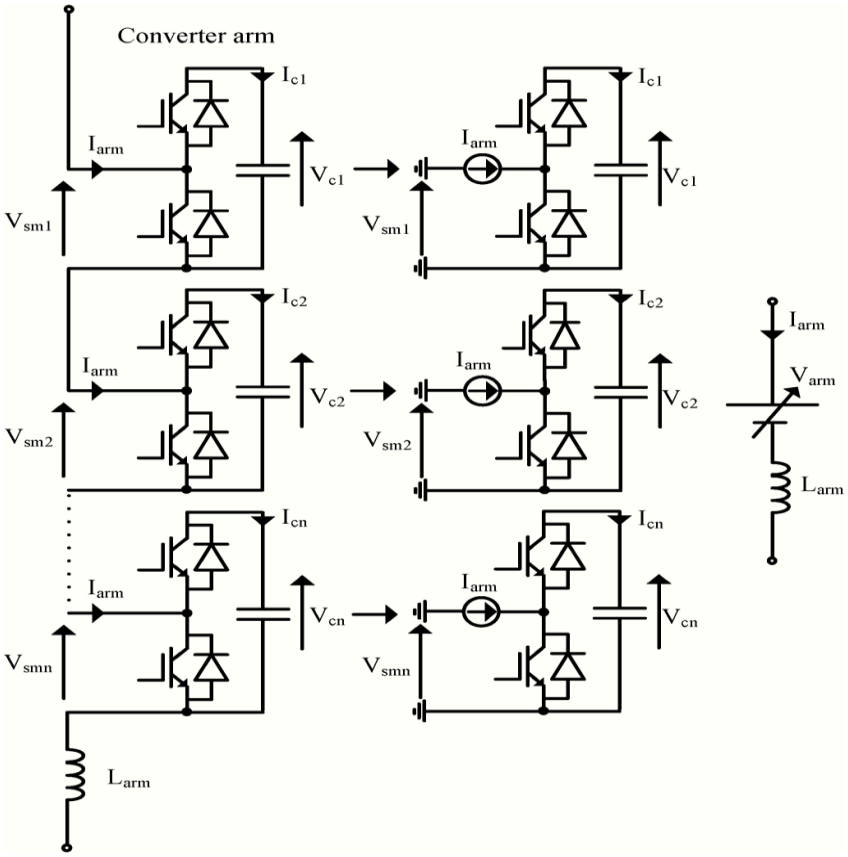

Fig.2: Implementation steps for the accelerated model.

wherethe value of the controllable voltage source is given by

$$V_{arm} = \sum_{i=1}^{n} V_{smi} \quad (1)$$

The AM reduces the size of the main network admittance matrix by solving the admittance matrix for each SM separately. The AM has two key advantages in comparison to the DEM. The first is that the AM allows the user access to SM components. The second is that because the AM is implemented using standard PSCAD components.

IV. SIMULATION MODELS

A detailed MMC model for a typical VSC-HVDC scheme, employing the traditional detailed model (TDM) converter arm representation, has been developed. This model is used as the TDM simulation model. The simulation models for the DEM and for the accelerated model (AM) are identical to the TDM, except that the TDM converter arms are replaced with the converter arms required for the DEM and AM, respectively. This approach ensures that fair comparisons between the different modeling techniques can be made.

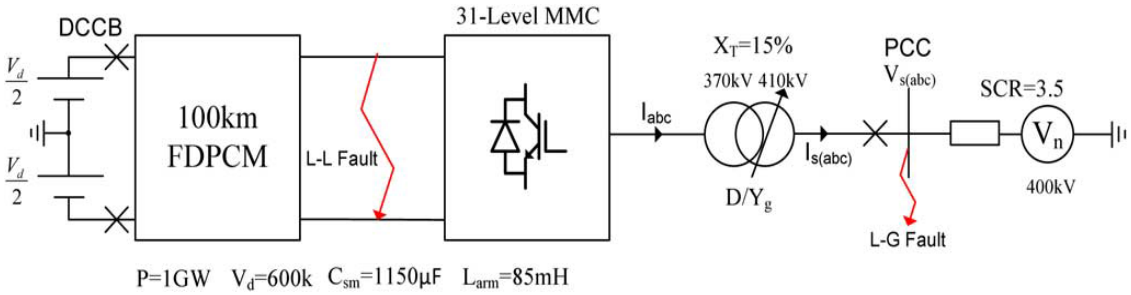

Fig.3: Basic simulation model structure.

A. Model Structure:

This model is similar but represents a subsection of the network rather than just the converter used. The basic structure of the simulation model and the key parameters are shown in Fig. 3.

Developing a TDM for an MMC with hundreds of SMs, such as a commercial installation, would result in lengthy simulation times. A 31-level MMC was selected for this model since it produces acceptable harmonic performance with a nearest level controller without unnecessarily increasing the simulation time and yet providing a sufficient converter complexity to provide a fair test. The selection of the SM capacitance value is a tradeoff between the capacitance ripple voltage and the size of the capacitor. The SM capacitance was calculated to give a ripple voltage of 10%.

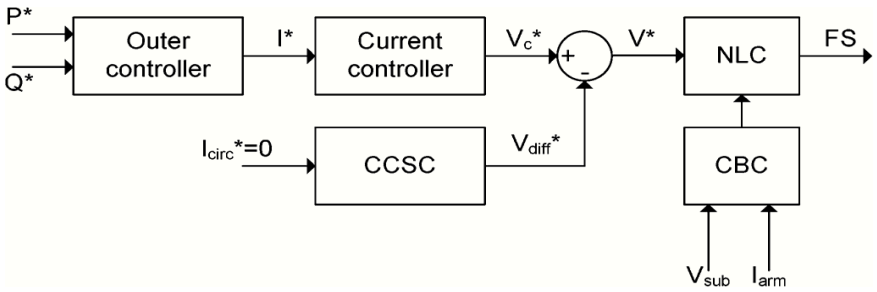

Fig.4: Simplified MMC control system

The arm reactors have two main functions. The first function is to suppress the circulating currents between the legs of the converter, which exist because the dc voltages generated by each converter leg are not exactly equal. The second function of the arm reactor is to limit the fault current rate of rise to within acceptable levels. The dc system is modeled as a dc voltage source connected in series with a frequency-dependent phase cable model (FDPCM) which represents two 300-kV 100-km XLPE cables. The ac network is modeled as a voltage source connected in series with a resistor and an inductor, to give a relatively strong short-circuit ratio (SCR) of 3.5. The converter transformer employs a delta/star winding with a tap changer.

B. MMC VSC-HVDC Control Systems

A simplified diagram for the three-phase 31-level MMC control system is shown in Fig. 4.

1) Current Controller: The impedance between the internal voltage control variables $V_{c(abc)}$and the ac system voltage

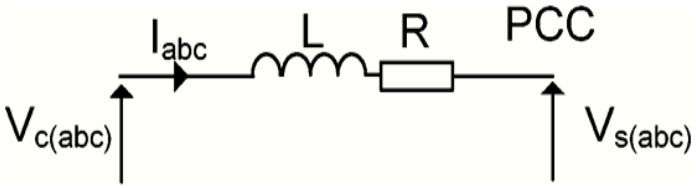

Fig.5: MMC phase a connection to an AC system.

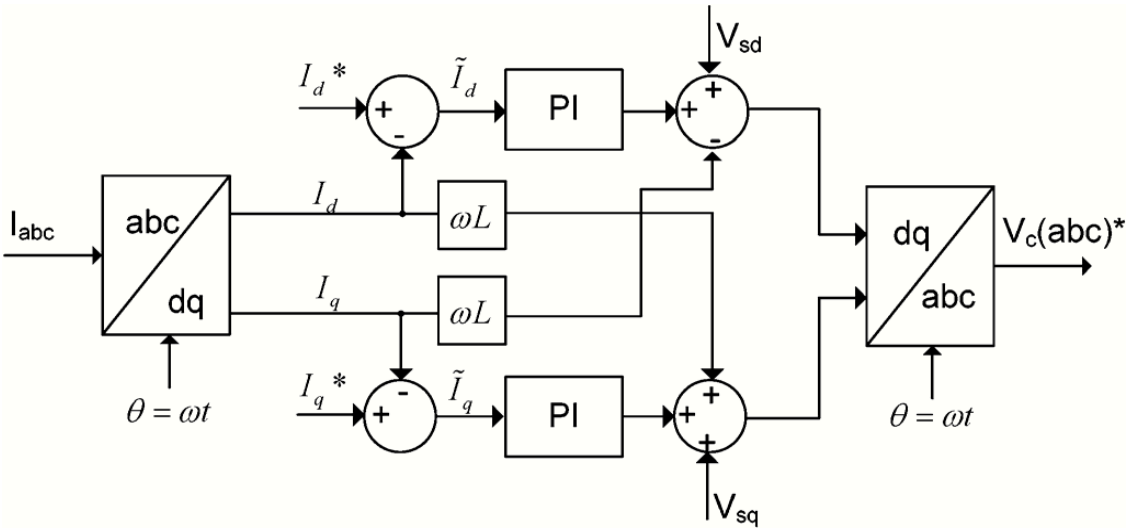

Fig.6: Implementation of the dq current controller.

$V_{s(abc)}$is shown in Fig. 5. Equation (10) describes the relationship between the internal voltage control variable and the ac system voltage for the three phases

$$V_{cs(abc)} = L\frac{dI_{abc}}{dt} + RI_{abc} \tag{2}$$

Where

$$V_{cs(abc)} = V_{c(abc)} - V_{s(abc)}$$

$$L = \frac{L_{arm}}{2} + L_T \qquad R = \frac{R_{arm}}{2} + R_T \tag{3}$$

Equation (2) in the dq synchronous reference frame gives(4) where $P = d/dt$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = R\begin{bmatrix} I_d \\ I_q \end{bmatrix} + L_P\begin{bmatrix} I_d \\ I_q \end{bmatrix} + \omega L\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{4}$$

The current controller employed in this model is a fast feedback dqdecoupled controller.

2) Outer Controllers: In the magnitude invariantdq synchronous reference frame with the -axis aligned withV_a , the real and reactive power flow at the point of common coupling can be described by (5) and (6) respectively. Feed forward

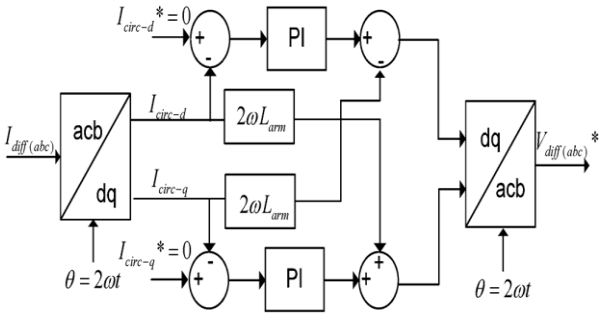

Fig.7: Implementation of CCSC.

controllers are used to set the I_d and I_q values to control the real and reactive power, respectively

$$P = \frac{3}{2} V_{sd} I_d \tag{5}$$

$$Q = -\frac{3}{2} V_{sd} I_q \tag{6}$$

3) Circulating Current Suppressing Controller: The circulating current is a negative-sequence (a-c-b) current at double the fundamental frequency. This current is found to increase the RMS value of the arm current leading to increased converter losses.

$$V_d = V_{ua} + I_{ua}(R + L_P) + I_{la}(R + L_P) + V_{la} \tag{7}$$

$$V_{diff-a} = I_{diff-a}(R_{arm} + L_{arm}p) \tag{8}$$

Where

$$V_{diff-a} = \frac{V_d}{2} - \frac{V_{ua}+V_{la}}{2} \tag{9}$$

$$I_{diff-a} = \frac{I_d}{3} + I_{circ-a} \tag{10}$$

In matrix form, (8) for the three phases can be written as (11). Applying theabc/dq transform to (11) gives (12). The zero-sequence quantities do not affect the d-axis and q–axis values and, hence, the use of I_{circ} in

$$\begin{bmatrix} V_{diff-a} \\ V_{diff-c} \\ V_{diff-b} \end{bmatrix} . R \begin{bmatrix} I_{diff-a} \\ I_{diff-c} \\ I_{diff-b} \end{bmatrix} + L_P \begin{bmatrix} I_{diff-a} \\ I_{diff-c} \\ I_{diff-b} \end{bmatrix} \tag{11}$$

$$\begin{bmatrix} V_{diff-d} \\ V_{diff-q} \end{bmatrix} = R_{arm} \begin{bmatrix} I_{circ-d} \\ I_{circ-q} \end{bmatrix} + L_{arm} p \begin{bmatrix} I_{circ-d} \\ I_{circ-q} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega L_{arm} \\ 2\omega L_{arm} & 0 \end{bmatrix} \begin{bmatrix} I_{circ-d} \\ I_{circ-q} \end{bmatrix} \tag{12}$$

A dq decoupled circulating current controller is employed with the$I_{circ-dq}$ reference values set to zero as shown in Fig. 7.

4) Capacitor Balancing Controller: The capacitor balancing controller (CBC) ensures that the energy variation in each converter arm is shared equally between the sub modules within that arm.

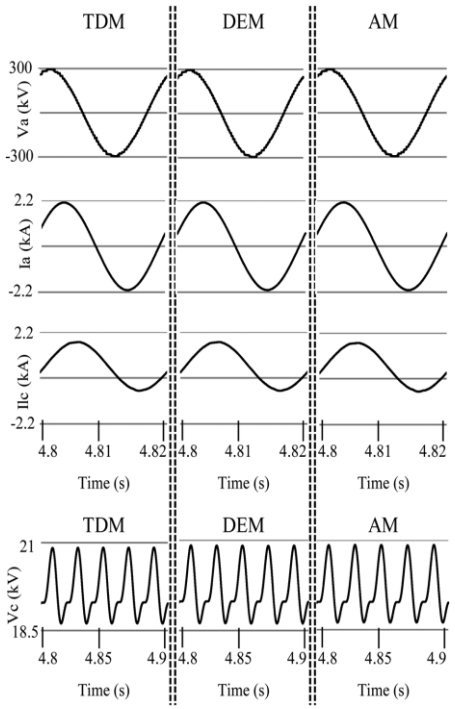

Fig.8: Steady-state simulation results for the three models. From top to bottom: (a) Phase A output voltage. (b) Phase A output current. (c) Phase C lower arm current. (d) Phase A upper arm mean capacitor voltage.

5) Nearest Level Controller: A number of modulation methods have been proposed for MMCs. The nearest level controller (NLC) method produces waveforms with an acceptable amount of harmonic content when a suitable number of MMC levels are

employed. It is the least computational complex method of the aforementioned techniques and, thus, is used for the model in this paper.

V. RESULTS

In this section, the three models are compared in terms of their accuracy.
The models' accuracy is assessed for steady-state and transient events through conducting a range of typical studies. Their accuracy is evaluated graphically and numerically by calculating the mean absolute error (MAE) of the waveforms produced by the DEM and AM with respect to the TDM. The MAE is normalized to the mean value of the TDM waveform.

1) Steady-State: The steady-state waveforms produced by the models for the converter operating as an inverter at 1000 MW are shown in Fig. 8. The waveforms are virtually identical and this is confirmed by the very small (1%) normalized MAE values given in Table I.. The results generally show that the accuracy of themodels decreases as the operating point decreases. This is especially the case for the phase current and arm current. The average THD of the phase A output voltages for the three models, when operating at 1000 MW in steady state, was found to be between 1.35% and 1.36%.

Table I: Normalized mean absolute error for the dem and am waveforms when operating in steady state at 1000 mw

1000MW Steady-state		
Signal	**DEM error (%)**	**AM error (%)**
Va	0.27	0.81
Ia	0.12	0.48
Iua	0.32	0.61
Vc	0.11	0.21

2) DC-Side Line-to-Line Fault: A dc line-to-line fault is applied at 4.5 s to the MMC terminals as shown in Fig. 3. The dc circuit breakers (DCCBs) are opened 2 ms after the fault is applied so that the dc voltage sources do not continue to contribute to the fault current. The MMC converter is blocked at 4.502 s, and the ac-side circuit breakers (CBs) are opened at 4.56 s. In this paper, the converter is considered to be blocked when both IGBTs are switched off. The waveforms produced by the models are shown in Fig. 9 and their normalized MAE values are given in Table IV.

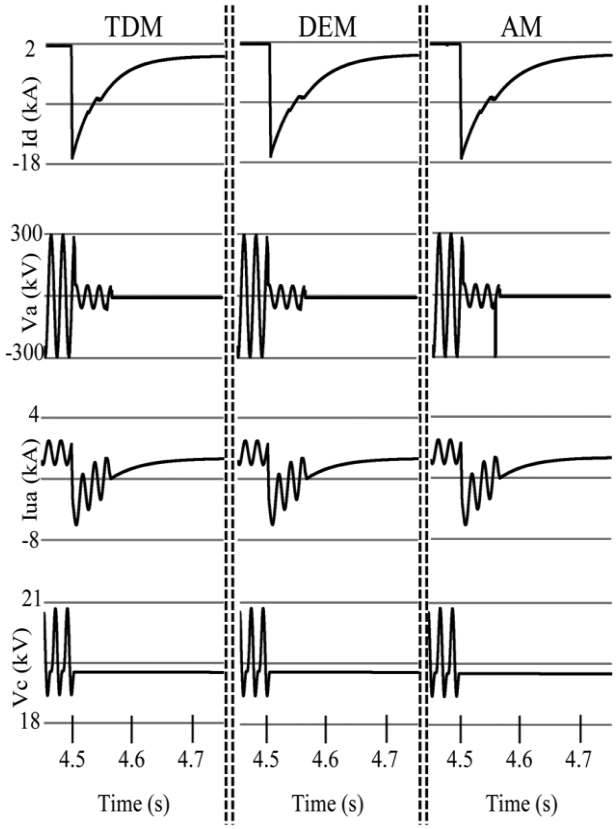

Fig.9: DC line current for a dc line-to-line fault applied at 4.5 s. From top to bottom: (a) dc current, (b) phase A output voltage, (c) phase A upper arm current, and (d) phase A upper arm mean capacitor voltage.

Table II: Normalized mean absolute error for the dem and am waveforms for a dc line-to-line fault

DC Fault		
Signal	**DEM error (%)**	**AM error (%)**
Id	0.41	2.29
Va	0.22	1.12
Iua	0.51	1.83
Vc	0.07	0.07

3) AC Line-to-Ground Fault: A line-to-ground fault is appliedto phase A at the point of common coupling (PCC) for 60ms at 4.5 s as shown in Fig. 3. The waveforms produced by themodels are shown in Fig. 10, and their normalized MAE valuesare given in Table V.

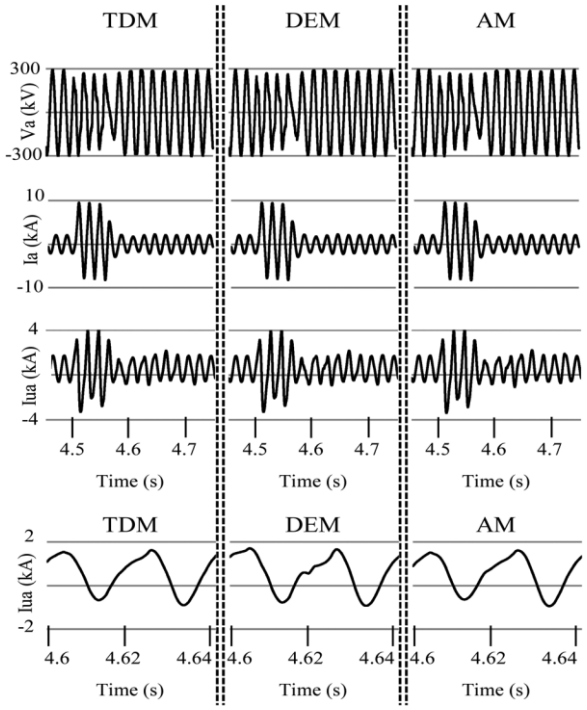

Fig.10: Line-to-ground fault for the phase applied at 4.5 s. (a) Phase A output voltage. (b) Phase A output current. (c) Phase A upper arm current. (d) Phase A arm current, zoomed.

Table III: Normalized mean absolute error for the dem and am waveforms for a line-to-ground ac fault

AC Fault		
Signal	**DEM error (%)**	**AM error (%)**
Va	0.96	1.76
Ia	0.51	1.37
Iau	3.01	4.34
Iau zoom	11.72	5.14

The circulating current is a key component of the arm current as described. Comparing the accuracy of the arm current therefore effectively compares the models' ability to simulate the circulating currents. The CCSC suppresses the circulating currents to very low values in steady-state operation, which is shown in Fig. 10(c) by the low levels of distortion in the arm current waveforms before the ac fault and several cycles after it are cleared (>4.7 s).

4) AM Simulation Limitation: The AM implemented in this paper was found to be unable to fully manage the simulation case when the converter is blocked as shown in Fig. 9. To further demonstrate this issue, the converter is blocked at 3 s when operating as an inverter at 1000 MW, and the Phase A output voltage for the three models is shown in Fig. 11. Clearly, the converter voltage for phase A for the AM is different shown in Fig. 12.

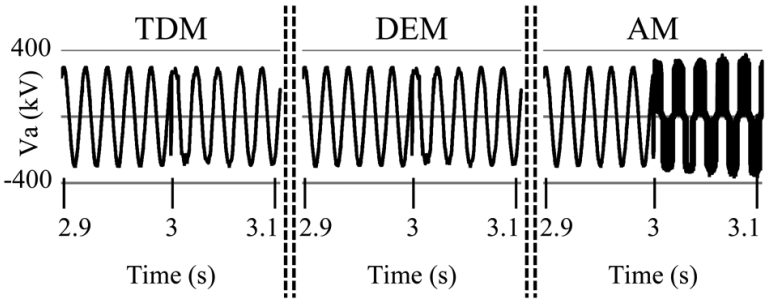

Fig.11: Phase A output voltage.

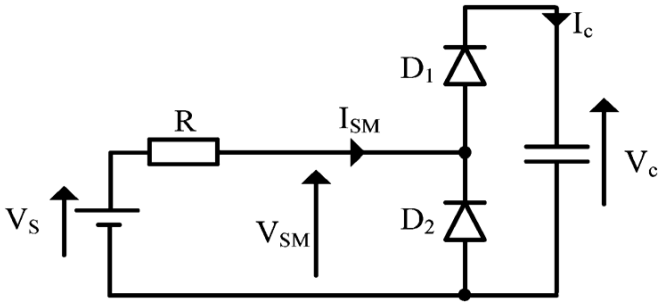

Fig.12: Example SM test circuit.

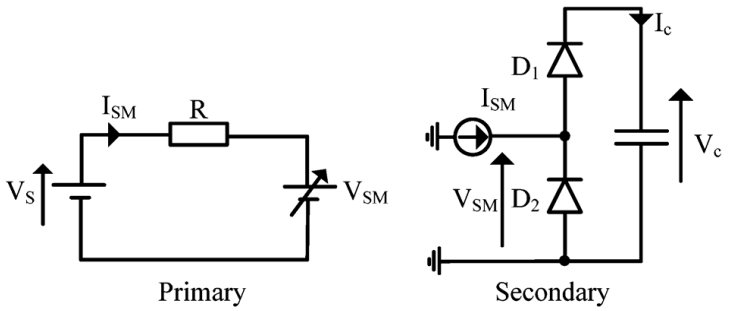

Fig.13: Implementation of the SM test circuit based on AM principles.

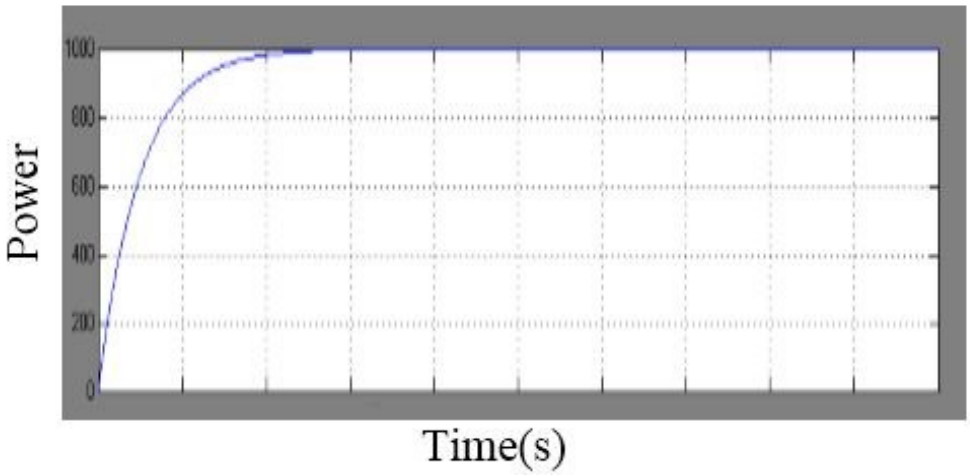

Fig.14: Active Power(P)

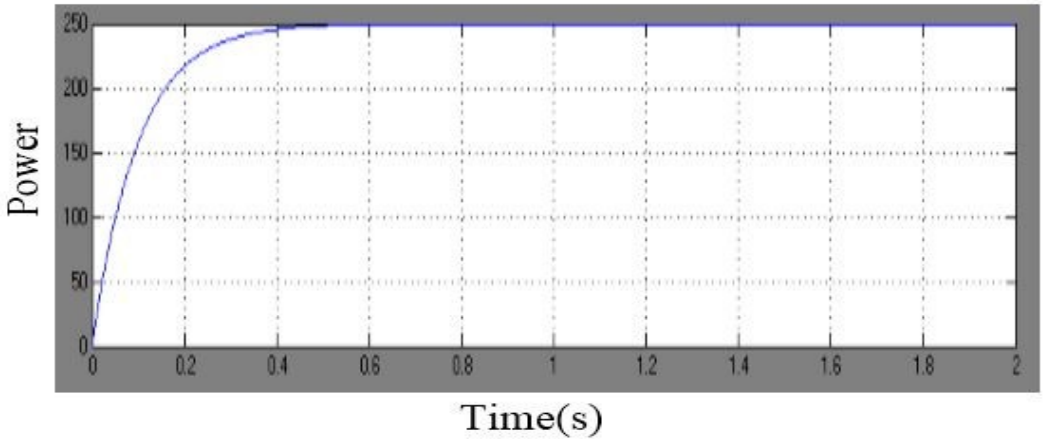

Fig.15: Reactive Power(Q)

A model of this circuit based on the principles of the AM is shown in Fig. 13. The SM current is measured in the primary circuit and is used as the current source reference in the secondary circuit, and the SM voltage is measured in the secondary circuit and is used as the voltage-source reference in the primary circuit. Each network is therefore solved at the present time step based on information from the other network at the previous time step.

Upon model initialization,$V_{sm} = 0V$ and, therefore, the SMcurrent flows in the positive direction causing the upper diode D1 to conduct and the SM capacitor to charge. Once the SM capacitor is fully charged, if the voltage-source value is reduced, the upper SM diodeD_1 should become reversed biased. Assuming that the SM diodes are ideal, the SM capacitor voltage should remain constant $V_s = V_{sm}$and$I_{sm} = 0$.However, this is not the case with the model implemented based on the AM

principles. The arm current in the primary circuit becomes negative because the value ofV_{sm} is equal to V_C which is higher thanV_s At the next time step, the negative arm current value causes the lower diode in the secondary circuit to conduct and, hence,$V_{sm} = 0$. At the next time step, the arm current becomes equal to V_s/R_s , causing the SM capacitor to charge.

CONCLUSION

This paper has presented the first independent comparison of two previously developed MMC modeling techniques (AM and DEM). It is has also presented the first independent verification of the AM, and the first independent verification of the DEM in PSCAD. An MMC-HVDC test system was developed and the AM model and DEM modeling techniques were compared against the TDM modeling technique in terms of accuracy and simulation speed.

The accuracy of the AM and DEM models was evaluated graphically and numerically for steady-state and transient studies. The unique findings contained within this paper have shown that the AM and DEM modeling techniques offer a good level of accuracy but that the DEM is generally more accurate than the AM.

The AM and DEM models have been shown to simulate significantly faster than the TDM, and the DEM is more computationally efficient than the AM.

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