

Carbon Nanotube Field Effect Transistor based Digital Logic Circuits

V. Sridevi¹ and T. Jayanthi²

¹*Research Scholar, Sathyabama University, Tamil Nadu, India.
E-mail: asridevi_2005@yahoo.com*

²*Principal, Panimalar Institute of Technology, Tamil Nadu, India.
E-mail: jayanthymd@rediffmail.com*

Abstract

Carbon nanotubes (CNTs), with exceptional electronic and optical properties, have become great interest for future electronic applications. Some of these properties such as symmetric band structure, direct bandgap, and near ballistic transport make them attractive for circuit implementations. The objective of this paper is modeling, performance evaluation and prediction of carbon nanotube field effect transistors (CNTFETs) for nanoscale devices and circuits. Comparison of circuit performance of carbon nanotube field effect transistor and conventional Si CMOS has been made for various benchmark circuits such as NOT, NAND and NOR gates.

Index Terms: Carbon Nanotube (CNT), CNT Field Effect Transistor (CNTFET), Schottky Barrier, Fermi Dirac probability, Compact modeling, logic gates.

Introduction

For many years MOSFET has been used as a basic element of circuit designing[1]. As the miniaturization of silicon based circuits reaches its physical limitations, molecular devices are becoming hopeful alternatives to the existing silicon technology[2][3]. Carbon Nano Tube (CNT) technology is at the front of these technologies due to the unique mechanical and electronic properties. Semi- conducting carbon nanotube can be used as the channel in Carbon Nanotube Field Effect Transistor (CNTFET). CNTFET Schottky barriers (SB) are formed between the metal contacts at source/drain (S/D) and semiconducting carbon nanotube. Depending on the work function difference between the metal contact and the CNT, carriers at the metal-CNT interface encounter different barrier heights. Therefore, carriers with energies

above the Schottky barrier height reach the channel by thermionic emission. On the other hand, carriers with energies below the Schottky barrier height have to do tunnelling to reach the channel featuring a transmission function. By changing the gate voltage, the transmission coefficient is modulated and as a result the total current changes.

In this work, we have focused on the development of a compact model for the Schottky barrier CNTFET and the versatility of the developed model has been demonstrated using basic logic gates. Introduction of the Carbon nanotubes, their background, the underlying physics and electronic structure of the CNT has been discussed in detail followed by the modeling aspects of Coaxially Gated Schottky Barrier CNTFET and the derivation of equations for charge and current as a function of the applied voltage. The I-V characteristics of the SB CNTFET and simulation results of various benchmark circuits such as NOT, NAND and NOR gates[4] has been discussed. Finally the research paper has been concluded with the work undertaken in this research work and the scope for improvement of the circuit level transistor models.

Carbon Nanotube Electronics

Carbon nanotubes were discovered by S. Iijima[5] in 1991 while performing some experiments on molecular structure composed of carbonium. CNTs are hollow cylinders composed of one or more concentric layers of carbon atoms in a honey comb lattice arrangement [6],[7]. It can be classified into SWCNT (Single Walled Carbon Nano Tube) and MWCNT (Multi Walled Carbon Nano Tube) shown in Figure 1. CNTs can be either metallic or semiconducting; this raises the scope for new integrated circuit technologies made from CNT transistors and interconnects [8]. However, in this research we confine our study to CNT Field Effect Transistor.

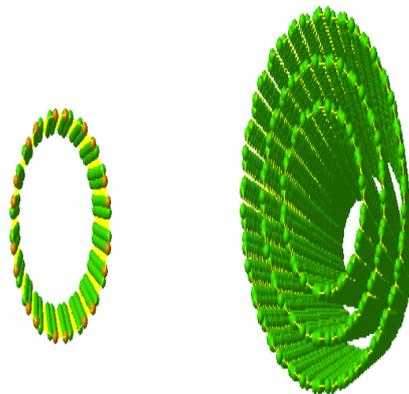


Figure 1: SWCNT and MWCNT.

The SWCNTs are 1-D objects and as such their two-terminal conductance is given by Landauer's equation:

$$G = \frac{2e^2}{h} \sum_i^N T_i \quad (1)$$

where $2e^2/h$ is the quantum of conductance and $T I$ is the transmission of a contributing conduction channel (sub-band). The 1-D nanotube Density of States (DOS) computed for the lowest sub band of a Single Walled Nanotube can be expressed as:

$$D(E) = \frac{4}{\pi \eta v_f} \frac{|E| \theta(|E| - \Delta)}{\sqrt{E^2 - \Delta^2}} \quad (2)$$

where the Fermi velocity $v_f = 8.5 \times 10^5$ m/s and the energy gap is given by,

$$2\Delta = \frac{2\eta v_F}{3R} = \frac{4\eta v_F}{3d_{CNT}} \quad (3)$$

where R = radius of the nanotube and $\theta(x)$ is the Unit step function. Therefore, the Density of States has a symmetric distribution on either side of the Fermi level and the Conduction and Valence bands are symmetric which is advantageous for complementary operations.

CNTFET & its Modelling Aspects

A coaxially gated SB CNTFET is shown in Figure 2. In Schottky Barrier CNTFETs, the gate electrode spans over the entire length of an intrinsic nanotube, and transistor action is achieved by the modulation, by the gate, of the Schottky barrier profiles at the interfaces of the tube at the source and the drain contacts [9]- [13]. The nanotube of radius R_t forming the channel of CNTFET with a cylindrical gate of radius R_g surrounding it.

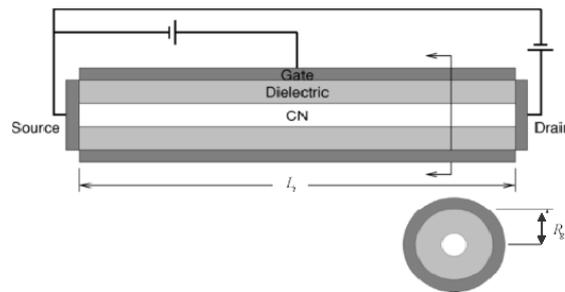


Figure 2: Coaxially gated CNTFET.

There exists a layer of cylindrical dielectric separating the tube and gate electrode. The gate dielectrics typically used for CNTFETs are SiO₂, Zirconia or Alumina. Bulk metal contacts at either side of tube form the source and drain of CNTFET.

The general expression for calculating the charge density of coaxially gated CNTFET is

$$n = \int_{-\infty}^{\infty} f(E) \times D(E) dE \quad (4)$$

where $f(E)$ is the Fermi Dirac probability for the occupation of an energy state E and $D(E)$, the 1-D nanotube Density of States. Fermi-Dirac probability is given by

$$f(E) = \frac{1}{\exp\left(\frac{E - E_f}{K_B T}\right) + 1} \quad (5)$$

where K_B is the Boltzmann constant. At $T = 300$ Kelvin, $K_B T \approx 25.6$ meV. If n is the mid-length charge density on a nanotube channel, then the dependence of the local potential on this charge is given in terms of the gate capacitance as:

$$U = \frac{q^2 n}{C_{ins}} \quad (6)$$

where C_{ins} is the gate capacitance per unit area given by $C_{ins} = \frac{\epsilon_{ins}}{t_{ins}}$. The mid-length charge density can be computed by taking into account the effect of the local potential as

$$n = \int_{E_c}^{\infty} f(E) \times D(E + V_{gs} - U) dE \quad (7)$$

Transistor Current Expressions

The expressions for transistor current flowing through the CNTFET channel can be derived from standard two terminal Landauer conductance formula [14]

$$I = \frac{q}{h} \int_{-\infty}^{\infty} T(E) \cdot [f(E - \mu_s) - f(E - \mu_d)] dE \quad (8)$$

where, $T(E)$ is the quantum mechanical transmission coefficient through the ballistic device and $f(E)$ is the Fermi-Dirac probability. μ_s, μ_d refers to the electrochemical potential at the drain and source end of the device under consideration given by

$$\mu_s = E_f + \frac{qV_{ds}}{2} \quad \text{and} \quad \mu_d = E_f - \frac{qV_{ds}}{2}$$

For our model of the SB-CNFET, the Landauer equation can be modified to obtain the electron current as:

$$I_n = \frac{2q}{\Pi \eta} \int_{E_c}^{\infty} T(E) \cdot [[f(E) - f(E - E_{fn})] - [f(E - E_{fn}) - f(E + qV_{ds})]] dE \quad (9)$$

A similar current equation for the hole current can be derived by expressing electron current equation above in terms of the hole quasi Fermi levels as:

$$I_p = \frac{2q}{\Pi\eta} \int_{-\infty}^{E_v} T(E) \cdot [f(E) - f(E - E_{fp})] - [f(E - qV_{ds}) - f(E + E_{fp})] dE \quad (10)$$

The energy-dependent transmission probability $T(E)$ of the SB is given by

$$\ln T = -\frac{4}{3bV_\pi} \int_{z_i}^{z_f} (\Delta^2 - [E + qV(z)]^2)^{\frac{1}{2}} dz \quad (11)$$

The total current flowing through the device in terms of applied potentials on gate and drain is given by $I = I_n + I_p + I_t$. The expression for the thermionic current as a function of the applied drain voltage for a CNTFET [15] has been derived as

$$I_t = \frac{8e^2}{h} \cdot \exp\left(-\frac{E_g}{2k_B T}\right) \cdot V_{ds} \quad (12)$$

Circuit Model

Figure 3 shows the circuit arrangement for a ballistic one dimensional n-type model[4],[5].

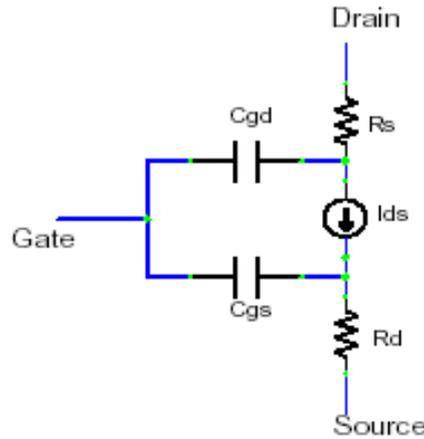


Figure 3: Circuit model of CNTFET.

The basic total drain current expression for our model is given by

$$I_D = \frac{4qk_B T}{h} [\ln(1 + \exp(-\xi_s)) - \ln(1 + \exp(-\xi_d))] \quad (13)$$

where $\xi_i = \left(\frac{\Psi_s - \Delta - \mu_i}{k_B T}\right)$ for $i = s, d$ and Δ is the half band gap energy and μ_i is '0' and –

qV_{ds} respectively for source and drain. Ψ_s is given by $V_{gs}-U$, where U is the local potential. Therefore the current expression can be implemented as

$$\Psi_s = V_{gs} - U \quad (14)$$

$$\xi_s = \frac{(\Psi_s - \Delta)}{k_B T} \quad (15)$$

$$\xi_D = \frac{(\Psi_s - \Delta - V_{ds})}{k_B T} \quad (16)$$

$$I_D = \frac{4qk_B T}{h} [\ln(1 + \exp(-\xi_s)) - \ln(1 + \exp(-\xi_D))] \quad (17)$$

$$I_t = \frac{8e^2}{h} \cdot \exp\left(-\frac{E_g}{2k_B T}\right) \cdot V_{ds} \quad (18)$$

$$I = \begin{cases} I_D + I_t & \text{for } V_{gs} > V_{th} \\ 0 & \text{for } V_{gs} < V_{th} \end{cases} \quad (19)$$

In the above circuit model, all the parasitic resistances and capacitances have been neglected. The interconnect capacitors and the gate-source and gate-drain overlap capacitors are the significant parasitic capacitors in the design. Likewise, the electrode resistances (R_s and R_d) play an important role in the delay characteristics of a CNTFET based circuit.

I-V Characteristics of SB CNTFET

The parameters used for the model are given below.

- Length of the tube: $L_t = 100\text{nm}$
- Chiral vector = $[19,0]$
- Gate Dielectric Thickness: $R_g = 6.0\text{nm}$
- SWNT Work function = Source/drain/gate metal work function = 4.5eV
- Operating temperature = 300K

Unipolar Characteristics of SB CNTFET

As the voltage across the gate and the source of SB-CNTFET is increased from 0 volts, the Fermi level of the nanotube moves closer to the conduction band. This band lowering effect causes barriers to develop at nanotube-metal junctions. The electrons which have enough potential will cross the barrier and flow into the tube, causing leakage current. In our model, the main source of leakage is the thermionic current. When a positive voltage is applied on the drain, the barrier spike begins to progressively diminish at that end of the channel. The barrier thickness, as seen by the charge carriers, begins to reduce too. Consequently, the electrons induced on the channel can now enter the drain metal by tunneling through the barrier while those carriers with sufficient thermal energy can jump over the barrier. The limiting value

of current through the nanotube is described by the thermionic current component.

We can see from the figure, that when no gate voltage is applied, for the case of $V_{gs} = 0$ in Figure 4(a), the current increases linearly with V_{ds} . This is attributed to the linear dependence of the thermionic current on the drain voltage. The application of a positive gate voltage induces heavy charge on the channel. It can be seen from the same figure that the current due to charge, tunneling through the barrier at the drain end, is significantly greater than the thermionic current component. The transfer characteristics in Figure 4(b) reflect a similar scenario. For an applied drain voltage, the current increases almost quadratically as soon as a gate voltage is applied. The two drain and transfer characteristics show that the current flowing through the device is very sensitive to the drain voltage and is largely controlled by manipulating the barrier height at the contacts.

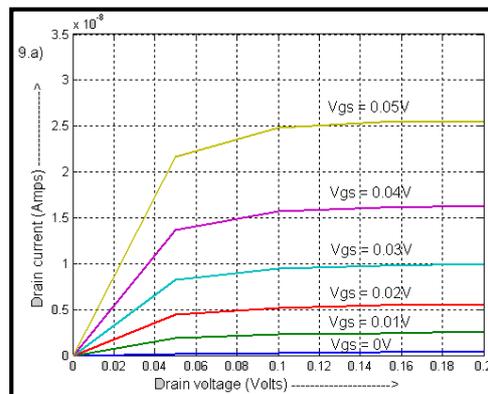


Figure 4(a): SB-CNTFET sub threshold Drain characteristics.

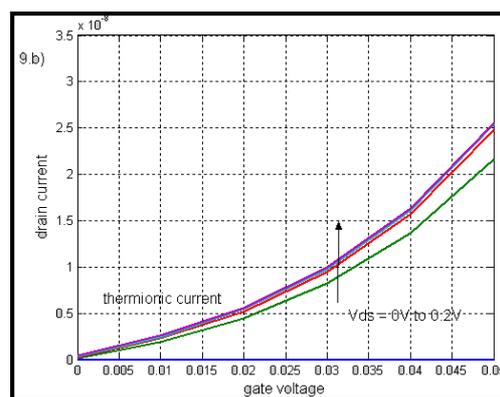


Figure 4(b): SB-CNTFET sub threshold Transfer characteristics.

We can see from Figure 5(a) that for a given V_{gs} , the current saturates at the region, i.e., when the applied $V_{ds} \approx$ barrier height. At this point the barrier is entirely suppressed and there is maximum current flow through the channel. Figure 5(b) shows an almost linear increase in the current as a function of the gate voltage. The

onset of current saturation as a function of drain voltage is expressed very clearly here. The plot consists of 5 curves for V_{ds} ranging from 0 – 1 V. However, while there is a marked increase in the current for an increase of V_{ds} from 0.1V to 0.3V, beyond this limit, all the other curves representing the higher values of V_{ds} are almost merged. The electron current beyond this point is independent of V_{ds} .

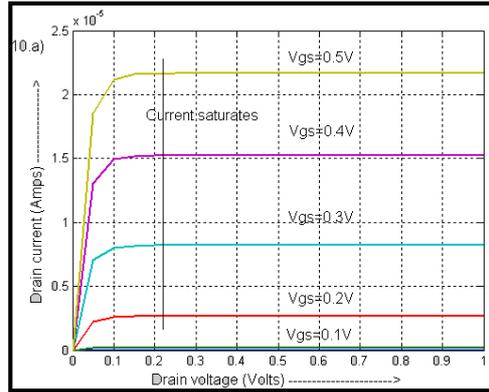


Figure 5(a): SB-CNTFET drain characteristics.

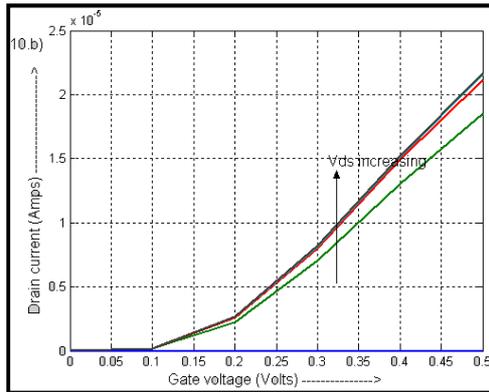


Figure 5(b): SB-CNTFET transfer characteristics.

Bipolar Current Characteristics of SB CNTFET

Figure 6 shows the Bipolar I-V characteristics for a SB-CNTFET which includes contribution due to the thermionic current. As the drain voltage is increased beyond the half bandgap value of SWCNT, the barrier for electrons at the drain is entirely suppressed and now a tunneling barrier begins to form for the holes. This leads to a net bipolar current that has contribution from the electrons injected into the channel from the source as well as holes injected into the channel from the drain. As V_{ds} keeps increasing, the hole current begins to increase until the point where V_{ds} is equal to the valence band edge of the SWCNT. At this point, the contribution due to the hole current equals that of the electron current and for a higher V_{ds} , the hole current exceeds the electron current in magnitude.

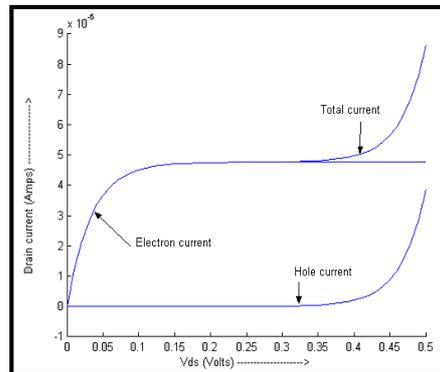


Figure 6: Bipolar I-V Characteristics of SB CNTFET.

Simulation Results & Discussions

In order to demonstrate the versatility of the CNTFET compact model, we employed it to design basic logic gates. Unipolar CNTFET behavior is very similar to conventional MOSFET. Unipolar CNTFETs can thus be used to design circuits using the same architectures than the ones used in standard CMOS technology, in particular complementary logic circuits such as NOT, NAND and NOR gates.

Not Gate

Figure 7 shows an exemplary logic gate (inverter) comprising of P-type and N-type CNTFETs. They are coupled together in series between a high supply voltage (V_{DD}) and a low supply reference V_{SS} , as shown. The first CNTFET which is biased to conduct holes, functions as a driver transistor with its gate providing an inverter input V_{IN} . The second transistor which is biased to conduct electrons, functions to facilitate an active load with its gate coupled to a supply V_{GG} for appropriately biasing it, so that the output provides suitable low and high values when V_{IN} is high and low respectively as shown in Figure 8.

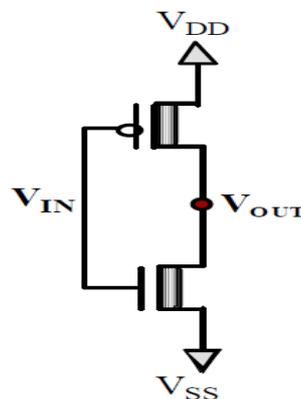


Figure 7: Structure of NOT gate.

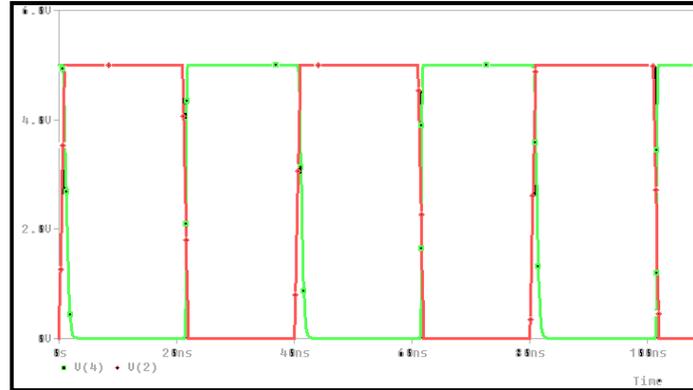


Figure 8: Behavior of CNTFET based NOT gate.

Nand Gate

Figure 9 shows an exemplary NAND gate comprising of CNTFETs as discussed herein in accordance with some embodiments. It comprises of driver CNTFETs coupled together in parallel between a high supply reference (V_{DD}) and a series active load transistors, which is coupled to a low supply reference V_{SS} , as shown. The gates of the driver transistors provide first and second NAND gate inputs respectively and a gate output is provided at the drain of third transistor as shown. If either input or any one of the input is Low (e.g., 0V) then the output is High (approaching V_{DD}), if both inputs are high, then the output will be Low as shown in Figure 10.

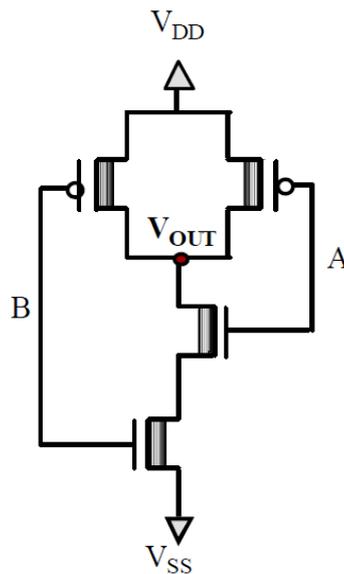


Figure 9: Structure of NAND gate

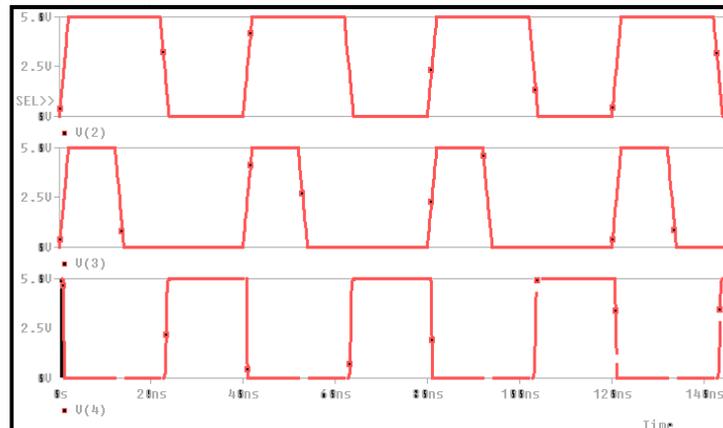


Figure 10: Behavior of CNTFET based NAND gate

Nor Gate

Figure 11 shows an exemplary NOR gate comprising of CNTFETs as discussed herein in accordance with some embodiments. It comprises of driver CNTFETs coupled together in series between a high supply reference (V_{DD}) and a parallel connected active load transistors, which is coupled to a low supply reference V_{SS} , as shown. The gates of the driver transistors provide first and second NOR gate inputs respectively and a gate output is provided at the drain of parallel combination as shown. If either input is Low (e.g., 0V) then the output is High (approaching V_{DD}), Conversely, if both inputs are high (approaching V_{DD}), then the output will be Low as shown in Figure12.

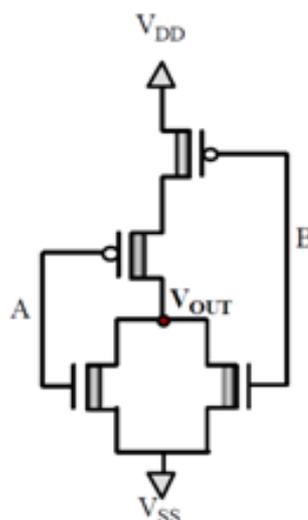


Figure 11: Structure of NOR gate.



Figure 12: Behavior of CNTFET based NOR gate.

Conclusion

The compact model has been developed for the Schottky-Barrier Carbon Nanotube Field Effect Transistor. The performance of the empirical model developed was evaluated using various characteristics. This model adequately explains the working of the SB CNTFET and demonstrates the bipolar nature of current flow in the transistor, it also accounts for the thermionic (leakage) current through the device and can generate the transistor I-V characteristics and their dependence on the gate dielectric thickness and nature of the insulator used. Simulation results of various benchmark circuits such as NOT, NAND and NOR gates has been discussed. A comparison has been made between the conventional MOSFET and CNTFET which shows that the power dissipation factor for generalized logic gates based on SB CNTFET library dissipate 19% less power on an average than a library of former CMOS gates.

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