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Need of A Nano-Transistor

[1]Abhishek Kumar and [2]Yogesh Wankhede

[1]ECE Department Lovely Professional University, Jalandhar, India
E-mail: abhishek.15393@lpu.co.in
[2]Electrical Engineering Department VJTI, Mumbai, India
E-mail: yogesh17.wankhede@gmail.com

Abstract

In this paper the limitation of conventional transistor has been demonstrated. Scaling of transistor gate lengths will ultimately be limited by off-state leakage current. Future transistor scaling will require the incorporation of new device structures, Carbon nanotube Field effect transistor (CNTFET) is one of the most promising device. In this paper technique to adjust the threshold voltage (Vt) of CNTFET and off state leakage current (I_{OFF}) has been discussed. The symmetric CNTFET has been the focus of much attention due to its inherent robustness to short-channel effects and improved current drive capability. Advantages of using alternative channel materials to facilitate scaling are investigated.

Keywords: MOSFET Scaling; CNTFET; Off state leakage.

Introduction

MOSFET is the one of the most preferred transistor due to its unique property of scaling. Scaling allows reducing the device size by all around without affecting the performance. Smaller size and portable device is the demand of industry and any other application, but there is limit of scaling beyond that the device does incorporate unexpected result.

In the mid- 1970 the gate length Lg was 4μm and the gate oxide thickness tox was 50 nm. Since then, each new generation of technology has shrunk Lg by about 30% and tox by about 25%. The Important principle in MOSFET scaling is that Lg and tox must decrease together. Scaling one without the other does not yield adequate performance improvement. Further scaling of device incorporate certain problem such

as short channel effect, drain induced barrier lowering (DIBL), reduction in threshold voltage, sub threshold leakage, band to band tunnelling (BTBT). A *nano* transistor wins over these problem and lead scaling beyond conventional transistor.

Limitation of Conventional Transistor

The conventional MOSFET transistor does incorporate following limitation.

- Short Channel Effect
- Lowering of Threshold voltage.
- Drain induced barrier lowering(DIBL)
- Sub threshold leakage current
- Band to Band Tunnelling(BTBT)
- Ratio of ON/OFF Current

Short channel effect in scaled MOSFET devices is the decreasing channel length, which lowers the threshold voltage Vth. In long-channel devices, the source and drain are separated far enough that their depletion regions have no effect on the potential or field pattern in most part of the device and hence the threshold voltage is virtually independent of the channel length and drain bias. In a short-channel device the source and drain depletion width in is comparable to the effective channel length. This causes the depletion regions from the source and the drain to interact with each other.

The short-channel effects are attributed to two physical phenomena:

1. The limitation imposed on electron drift characteristics in the channel,
2. The modification of the threshold voltage due to the shortening channel length

For a long-channel device, the barrier height is mainly controlled by the gate voltage and is not sensitive to Vds, but in small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage Vgs and the drain-to-source voltage Vds. Under off conditions this potential barrier between the source and the channel prevents electrons from flowing to the drain. When a high drain voltage is applied to a short-channel device, barrier height is lowered resulting in further decrease of the threshold voltage. The source then injects carriers into the channel surface without the gate playing a role. This is known as drain induced barrier lowering (DIBL). [2]

Ideally, DIBL does not change the sub threshold slope S, but does lower Vth. The DIBL effect increases as Vds increases. Higher surface and channel doping and shallow source/drain junction depths reduce the DIBL effect. As DIBL increases the Vth of the device gets significantly lowered resulting in higher subthreshold leakage current. The reduction of the potential barrier eventually allows electron flow between the source and the drain even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions (Vgs<Vt) is called the sub-threshold current. The current increases exponentially as the threshold voltage are lowered. Which result in increased ON/OFF current ratio.

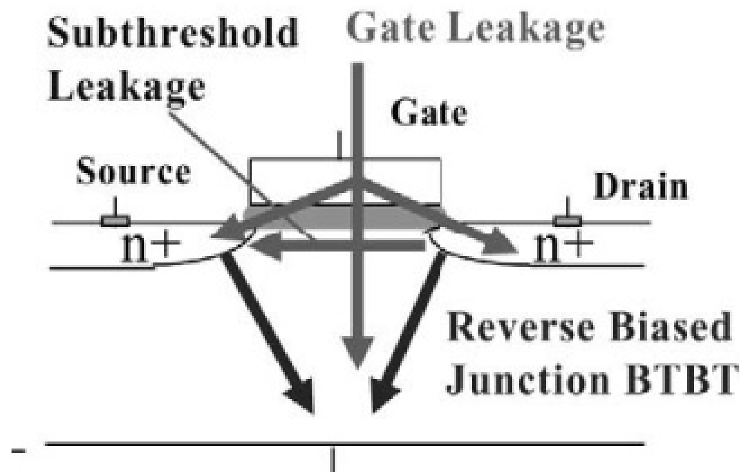

Figure 1: Limitation in MOSFET.

To mitigate the problem of lowered Vth in MOSFET the channel doping is increased in a region below the drain and the source and near the source-bulk and drain-bulk junctions.

These higher doping regions serve to increase the threshold voltage of the device and lower the subthreshold current. However for scaled devices (leff < 50nm) the increased halo doping creates a high electric field across the reverse biased drain-bulk junction. This causes a junction band-to-band tunnelling (BTBT) current to flow from the drain to the source of an N-MOS device. Thus the halo doping decreases the sub threshold current at the cost of higher BTBT leakage in scaled devices.

Now a day's semiconductor devices are scaling down beyond their physical limits. In the process the circuit and the system engineer is facing challenges of device stability. The Silicon MOSFET is no longer a perfect choice. Further, process variation has led to variation of the critical transistor parameters like length, width and threshold voltage (Vth) thereby reducing the production yield. Future transistor scaling will require the incorporation of new device structures. The novel devices include Modifications of bulk silicon into FINFETs, triage structures, double gate MOSFET, Carbon Nanotube transistor and Nanowire transistor. These modified MOSFET have better short channel immunity, better sub threshold slopes and better threshold voltage control. These devices with characteristics different from Silicon could potentially have better scalability and increase the on current to off current ratio.

Available Solution

Carbon Nano Tube

The single wall carbon nanotube (SW CNT) is a promising candidate as a building block for future nanoelectronic Devices. These devices typically use a gate electrode to control the carrier density of a semiconducting SW CNT. The simplest

configuration of a CNT FET is the bottom-gate FET, as shown in fig.2, in which, a SW CNT is dispersed or directly grown on a SiO2 /Si substrate, source drain contacts formed at the ends of the CNT and its transport properties controlled by applying a substrate voltage. [1]

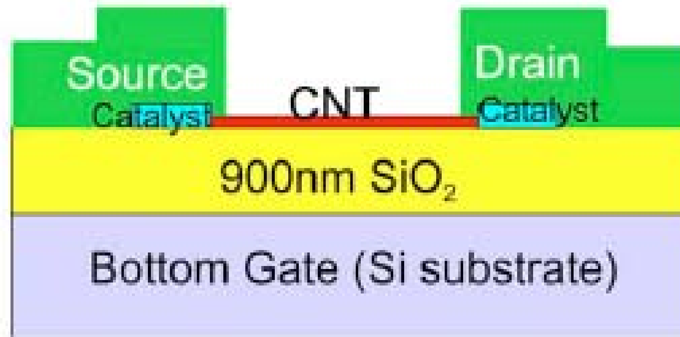

Figure 2: Bottom gate CNTFET.

Another variation is Top-gate CNT FETs in which the gate electrode and gate insulator are located on top of the SW CNT. To improve the device performance further a thinner gate insulator with a higher dielectric constant can be used. Recently, high k materials, such as, TiO2, ZrO2 and HfO2.

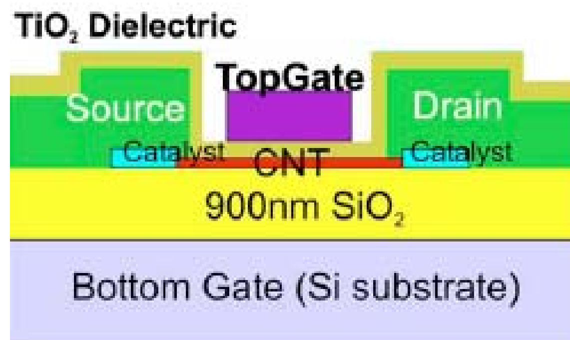

Figure 3: Top gate CNTFET.

The gate transfer characteristics of Bottom gated CNTFET is presented in Fig.4 At Vds=200 mV, the threshold voltage Vth is 0 V, on-current Ion=$1*10^{-7}$ A, and off-current Ioff=$1*10^{-12}$ A, giving this device an on/off ratio=10^5. The subthreshold slope is 1000 mV/dec and transconductance 0.04 μS|Vds=200 mV. As shown in fig.4 the subthreshold leakage current under condition (Vgs<Vt) is negligible. Variation in threshold voltage along with applied voltage one of most important property of Carbon nano tube. The gate transfer characteristics of Fig. 4 clearly shows a large Vthreshold hysteresis of 7 V depending on the direction the gate voltage

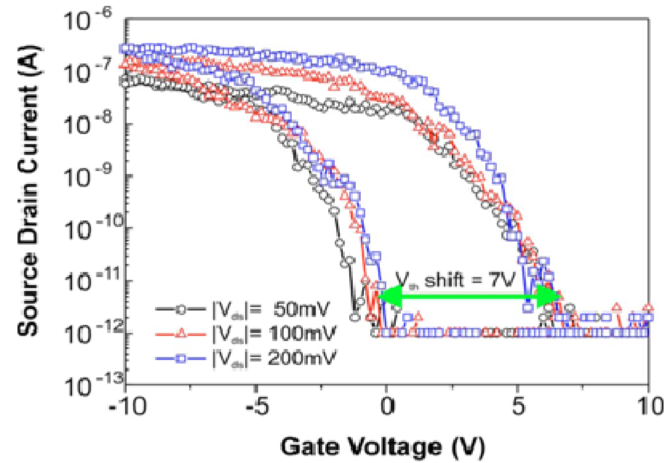

Figure 4: gate transfer characteristics of Bottom gate CNTFET.

A 5 nm TiO2 was deposited on top of the structure. The gate transfer characteristics of covered CNTFET were determined again as shown in Fig 5. At Vds=200 mV, the threshold voltage Vth is 0 V, on-current Ion=5*10^{-7} A, and off-current Ioff=4*10−11 A. The on/off ratio is 10^4 and the subthreshold slope improved to 320 mV/ deg. The transconductance also increased to 0.38 μS|Vds=200 mV By simply covering the CNT but still maintaining the bottom-gate operation, we observed that the hysteresis in Vthreshold was reduced to 2 V.

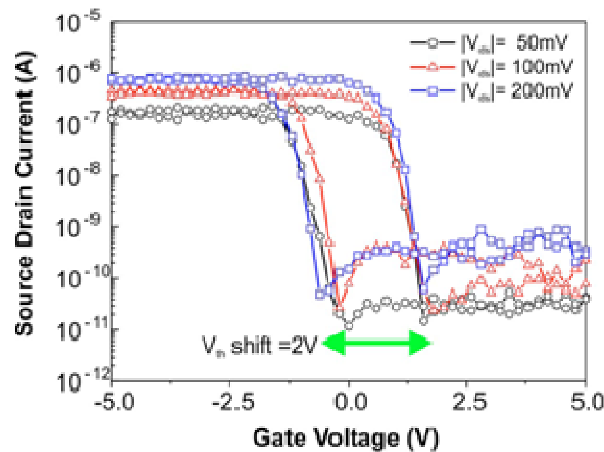

Fig.5 Gate transfer characteristics of Covered CNTFET

The top-gated CNT FET with a TiO2 high-k gate dielectric exhibits the highest transconductance (1.3 μS or 1000 μS/μm) a subthreshold swing 67–70 mV/dec. By simply covering the CNT but still maintaining the bottom-gate operation, we observed that the hysteresis in Vthreshold was reduced by 5 V.

Fig.6 and 7 Shows the comparative study of Drain voltage vs drain current characteristics of CNTFET and MOSFET, having nanotube diameter 1nm and gate dielectric constant 3.9.

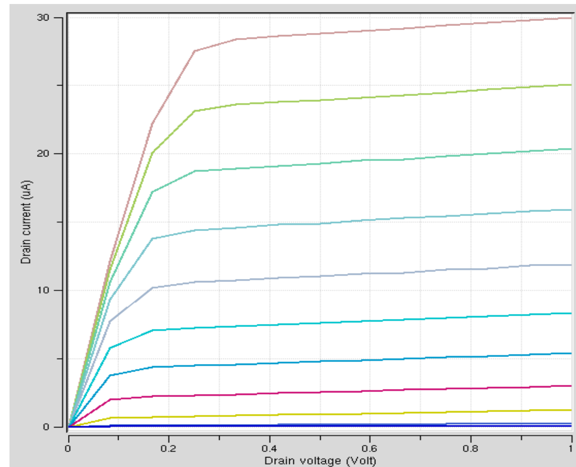

Figure 6: Id Vs Vd characteristics of CNTFET.

Compare to MOSFET; CNTFET shows less current in saturation region. For the same drain voltage CNTFET shows more control over drain current, while for a MOSFET the drain current depend on the gate length. For the same gate voltage 0.2 voltage MOSFET drain current is around 1800 µA and CNTFET drain current is 18 µA. Improvement ratio in off state current(Ioff) is 100 times. Since CNTFET having better control over drain current having less off state leakage current and improved short channel effect. Less off state current further result in better subthreshold leakage.

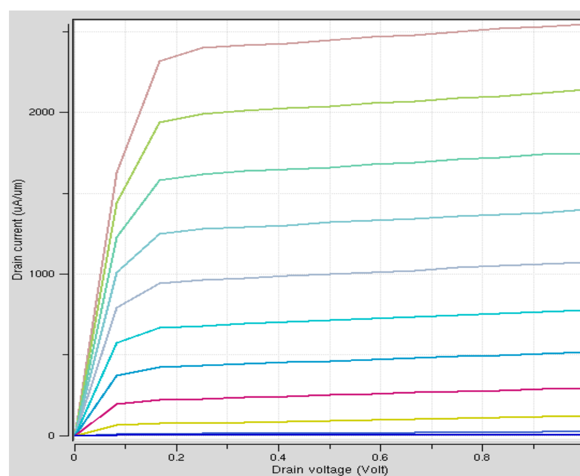

Figure 7: Id Vs Vd characteristics of MOSFET.

Conclusions

Limitations and challenges in gate length scaling threshold voltage control, off state leakage current of conventional MOSFET have been visualized. It has been observed the use of CNT allow us the further scaling. The use of low-k materials reduce subthreshold leakage and permit to control the threshold voltage of transistor. Threshold voltage of a carbon nanotube field effect transistor can be adjusted by up to ~2 V. These techniques enable device tuning for performance optimization.

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