Secure Communication using Chaotic Synchronization of PLL

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Abstract

A technique of secure communication via chaotic synchronization is proposed. A suitable frequency modulated (FM) signal is used to drive two different phase locked loops (PLLs) in chaotic region to obtain two different chaotic signals. Out of these two signals one will be transmitted to the receiver PLL depending on the digital data. Receiver PLL synchronized with the transmitted chaotic signal and an additional decision circuit regenerate the digital data depending upon the magnitude of the control voltage of the receiver PLL. The experimental results confirm the validity of the proposed technique.

Index terms: FM signal, PLL, Chaos, secure communication.

Introduction

Secure communications via chaotic synchronization have been reported earlier [1-9]. The idea of secure communication was first introduced by a group of scientist Pecora and Carroll [1-3]. A nonlinear sub-system can produce all state variables of the original chaotic system by sending the state variable from driver system to synchronizing system. By inserting the information signals with a chaotic signal of the original system at transmitter side and then recover the informational signal by using the synchronized chaos of the sub-system at receiver side. Generation and synchronization of chaotic signals using electronic circuits, namely Chua’s circuit, Jerk circuit, PLL, etc. are well documents in the literature [4-7]. In this article a secure communication technique of digital data using chaotic signals have been described. Here we have used second order PLLs for the generation and synchronization of chaotic signals since generation of chaotic signal using second order PLL in the influence of FM signal and its synchronizations are very common technique today.
System Description

The block diagram of the proposed secure communication systems using three second order PLLs are shown in figure 1. Two PLLs (PLL1 and PLL2) are located in the transmitter side to produce two different chaotic signals. The PLL3 is located in the receiver side to synchronize the received signals. The center frequencies of the PLL1 and PLL2 are $f_1$ and $f_2$ ($f_2 > f_1$) which are responsible for generating two different chaotic signals $S_1$ and $S_2$ in the transmitter side. It is well known that a PLL subjected to out of band FM signal can produce chaotic signals for specified design parameter [4]. The input of PLL1 and PLL2 is a common FM signal of carrier frequency $f_c = (f_1+f_2)/2$. In the receiver side another PLL of large lock range is used to synchronize the chaotic signals $S_1$ and $S_2$ generated by PLL1 and PLL2. Chaotic signals $S_1$ and $S_2$ are present in the lower and upper band of the frequency spectrum respectively. Therefore, if a wide range PLL is used to synchronize these two signals then the control dc of the PLL will be remarkably different for the chaotic signals $S_1$ and $S_2$ since they are present in two different frequency bands. A 2-to-1 multiplexer (MUX) selects one of the chaotic signals ($S_1$ or $S_2$) to be transmitted depending on digital data, i.e. 0 and 1 bit stream (pseudo random (PN) sequence) and transmits it to the receiver side. PLL3 in the receiver synchronizes to this signal. Therefore the control dc voltage of PLL3 changes between two values (say $v_1$ and $v_2$) depending on the received chaotic signals $S_1$ and $S_2$. This dc voltage is connected to a comparator after passing through a low pass filter. The output of the comparator is the regenerated digital data 0 and 1 bit stream depending on the dc voltage level of the output of the low pass filter (LPF). The performance of the proposed system is also studied in presence of noise signal and the results are satisfactory according to theoretical prediction.

![Figure 1: Functional block diagram of the secure communication system.](image)

System Parameters and Simulation Results

The proposed system as shown in figure 1 has been simulated using commsim...
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The inputs of PLL1 and PLL2 are common FM signal whose carrier frequency is 200Hz. The frequency spectrum of the FM signal is shown in figure 2. The free running frequency of PLL1 and PLL2 are 180Hz and 220Hz respectively. In both the cases VCO gain is 20Hz/volt. The receiver PLL has free running frequency of 200Hz and the VCO gain of this PLL is 30Hz/volt. The low pass filter used in all the PLLs are of the type of lead-lag filter. The frequency spectrum of chaotic output signals ($S_1$ and $S_2$) and the dc control voltage of the VCOs of PLL1 and PLL2 are shown in figure 3 and figure 4 respectively. The spectrum of the receiver PLL is shown in figure 5 for two different conditions: (i) the transmitted signal is directly connected to the input of the receiver PLL, (ii) the transmitted signal is added to the unwanted noise signal and then it is connected to the receiver PLL. The performance of this system is satisfactory when the magnitude of the noise signal is less than or equal to -7dBm/Hz. The threshold voltage value of the comparator is fixed in such a way so that the dc control voltage of PLL3 is distinguishable for two different chaotic signals $S_1$ and $S_2$. The transmitted data (PN Sequence) and the regenerated data from the control voltage of the receiver PLL is shown in figure 6 when the transmitted signal containing noise signal of magnitude -7dBm/Hz. This result confirms the validity of the proposed system for serial data communication.

![Figure 2: Frequency spectrum of the FM signal.](image2)

![Figure 4: Frequency spectrum of the FM signal.](image4)
Figure 3: (a) VCO control voltage of PLL1 (b) frequency spectrum of the chaotic output signal of PLL1.

Figure 4: (a) VCO control voltage of PLL2 (b) frequency spectrum of the chaotic output signal of PLL2.
Figure 5: Frequency spectrum of the output signal of the receiver PLL: (a) transmitted signal without noise (b) transmitted signal plus noise signal of amplitude -7dBm

Figure 6: Transmitted data (PN Sequence) and the regenerated data from the control voltage of the receiver PLL.

Conclusion
The proposed system successfully performs the function of secure communication of digital data. Two different PLLs successfully generate two different chaotic signals $S_i$
and $S_2$ when a common FM signal drive the PLL under out of lock condition. The performance of the receiver PLL gives satisfactory results even when the transmitted signal is corrupted by unwanted noise signal. The drawback of this algorithm is a small time difference between the transmitted data (PN Sequence) and the regenerated data. This time difference is equal to the locking time of receiver PLL and it is a common problem in all synchronies communication systems.

References