

Noise Reduction using Adaptive Filter Design with Power Optimization for DSP Applications

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Abstract

Noise in any signal is a very important factor to be dealt with. The noise includes the actual signal, making it difficult for the user at the receiver end to understand and interpret the information present in the signal in a correct manner. Therefore, it becomes very important to understand the characteristics of the noise present and reduce it in a way that the message is preserved. Adaptive filters are designed to pass signals of interest and suppress undesired signal components. Usually they are more complex and difficult to analyze than non adaptive systems but they offer the possibility of substantially increased system performance when input signal characteristics are unknown or time varying. Hence we implement an adaptive linear filter using LMS algorithm. There are several algorithms for adaptive filter design but LMS is the simplest technique. Here we use an 8 tap FIR filter whose coefficients are modified through a number of iterations specified by the user. The code is written in Verilog and tested and simulated in Cadence.

Index Terms: Dynamic Frequency Scaling, LMS Algorithm, Threshold Signal, Adaptive Filter

Introduction

In signal processing, the function of a filter is to remove unwanted parts of the signal, such as random noise, or to extract useful parts of the signal, such as the components

lying within a certain frequency range. The following block diagram illustrates the basic idea.

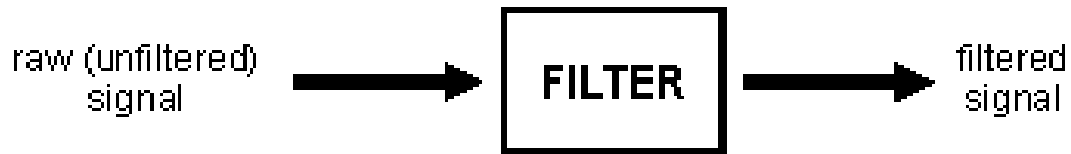


Fig 1 Basic Filter block

There are two main kinds of filter, analog and digital. An analog filter uses analog electronic circuits made up from components such as resistors, capacitors and op amps to produce the required filtering effect. A digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer such as a PC, or a specialized DSP (Digital Signal Processor) chip.

A Disturbance especially a random and persistent disturbance that reduces the clarity of signal is referred to as noise. They exist in various degrees in almost all environments. There may be several varieties of noise which could degrade the quality of communication such as acoustic background noise, thermal noise, electromagnetic noise, co-channel interference, radio-channel distortion. Noise can cause transmission errors. The various sources of noise affecting the audio signals are electromagnetic, acoustic, channel distortions, digitization and quantization noise.

There are various algorithms available for noise reduction. Adaptive filters are self-designing using a recursive algorithm. Adaptive filtering techniques have important applications such as echo cancelling, equalization, noise cancellation and others. The rapid growth of computer Technology has opened up new avenues in the development of new adaptive filter algorithms for more challenging situations like strong fading, large signal and noise distortions.

LMS Algorithm

Most popular adaptation algorithm is LMS. It was introduced by Widrow & Hoff in 1959. It is simple, no matrices calculation involved in the adaptation. LMS belongs to the family of stochastic gradient algorithms. It is derived from steepest descent method. It doesn't require gradient to be known, it is estimated at every iteration

System Block Using the LMS

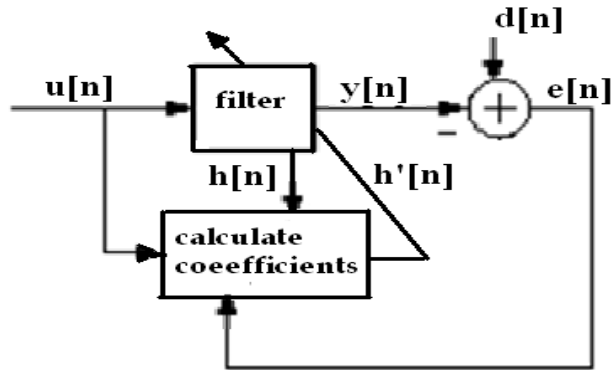


Fig 2 Basic LMS block

- $u[n]$ = Input signal from the channel
- $y[n]$ = Filter output
- $d[n]$ = Desired Response
- $h[n]$ = present coefficient
- $h'[n]$ = updated coefficient
- $e[n]$ = Error feedback

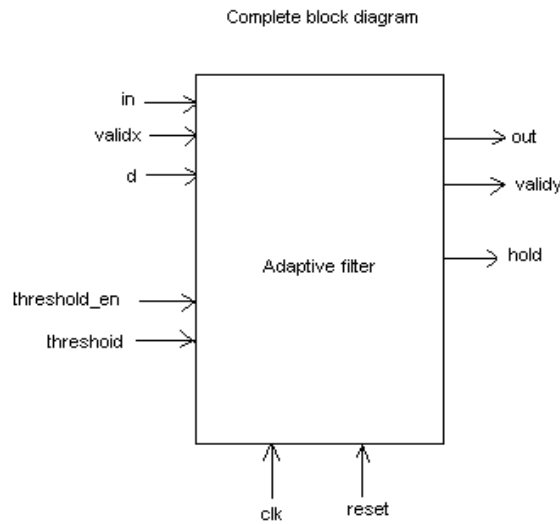


Fig 3 Block Diagram

Description

Top Level Description

The clock signal (clk) given is at 200 kHz frequency. At each pulse an input signal (in) of 8 bits is fed into the block with 4 integer bits and 4 fractional bits. The input is

accepted by the filter only when validx is asserted. If the filter is still processing the input signal, a hold signal is generated to stop the signal generator from producing more inputs. The output (out) obtained is also 8 bits, with 4 bits integer and 4 bits fractional. The signal validy is given when output y is obtained.

The threshold signal is given by the user to determine the number of iterations to be performed in the filter to obtain y. Greater the number of iterations, greater is the reduction in noise but this will increase processing time. Thus this signal allows the user a scope for programmability. This threshold value can be loaded through the signal threshold_en.

When the reset is given, all the inputs and control signals are set to 0. The top entity is divided into four other modules.

Internal Block Diagram

The top entity is divided into the following sub-blocks:

- filter block
- coefficient calculator
- error-check block
- controller

The following block diagram shows the interconnection of the several blocks. The filter output is fed to the error module where the error is calculated. This value of error is sent in to the coefficient calculator. This module now calculates the new set of coefficients based upon the old set of coefficients and the control signals generated by the controller. The controller also generates the signals h_en and d_en which triggers the filter to work.

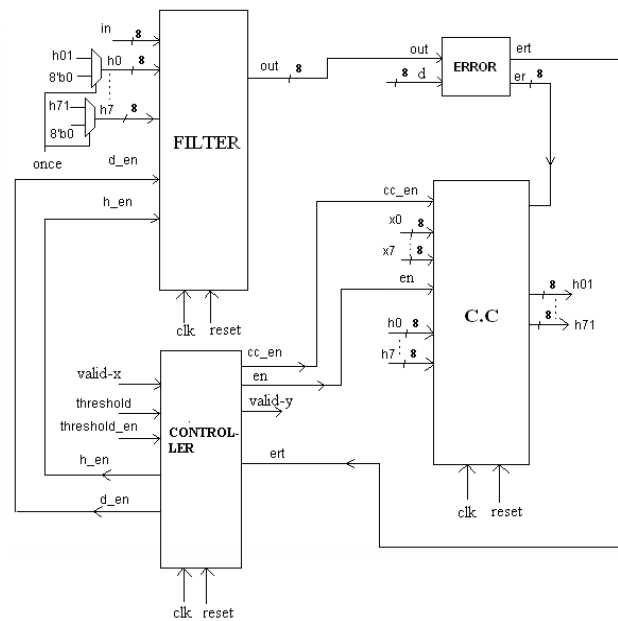
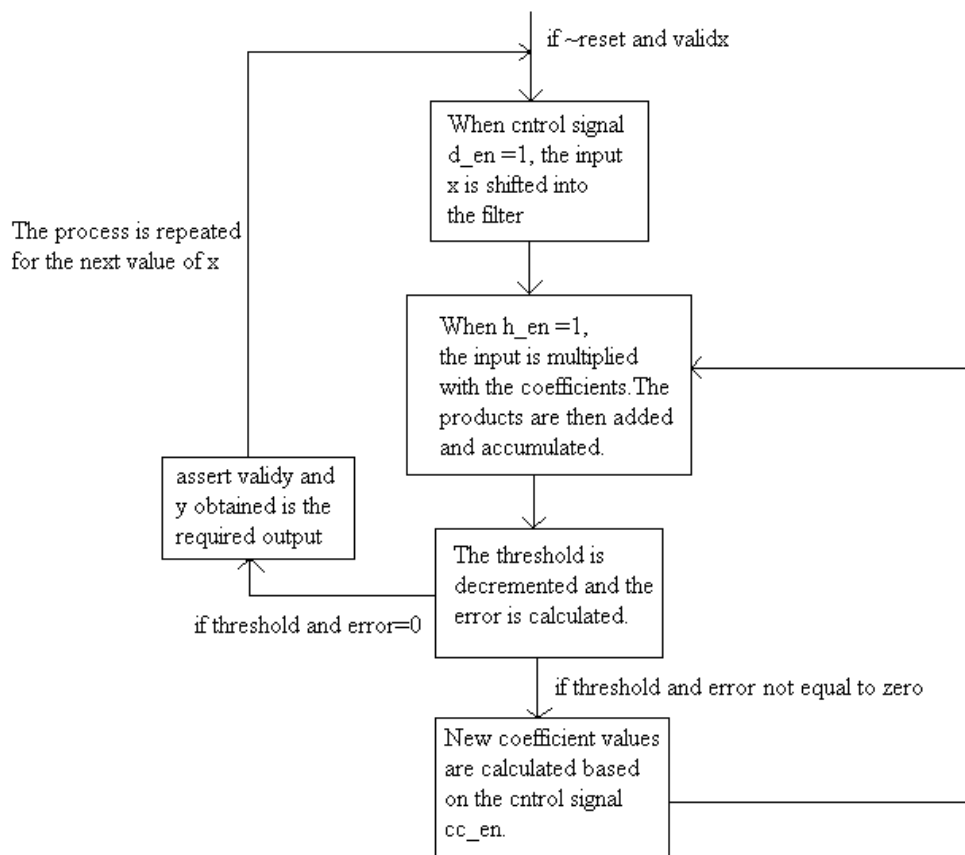


Fig 4 Internal block diagram

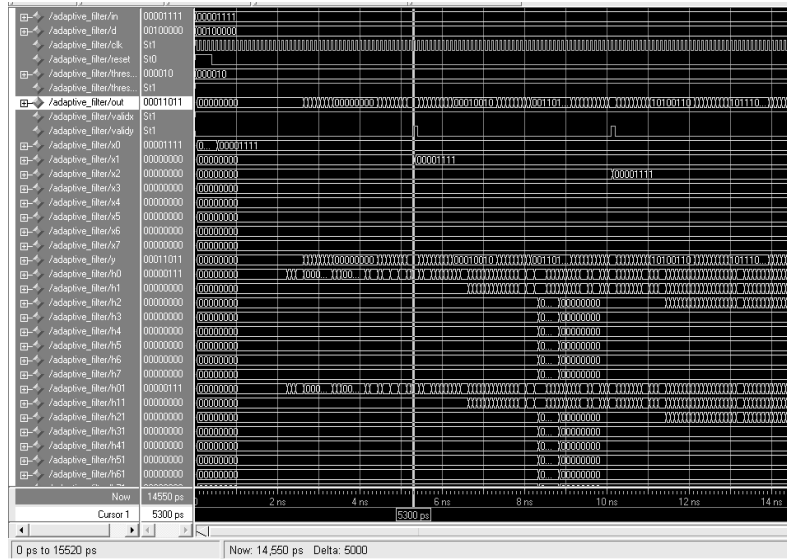
The controller is the heart of the adaptive filter module since it decides which block must function depending on the calculation to be performed. It generates the control signals 'h_en' and 'd_en' for functioning of the filter and 'cc_en' and 'en' signal for functioning of the coefficient calculator. It also generate 'valid_y' signal when the output is calculated. All these signals are generated based on the input signals 'valid_x', 'threshold', 'threshold_en' and 'ert' signals.

Software Description

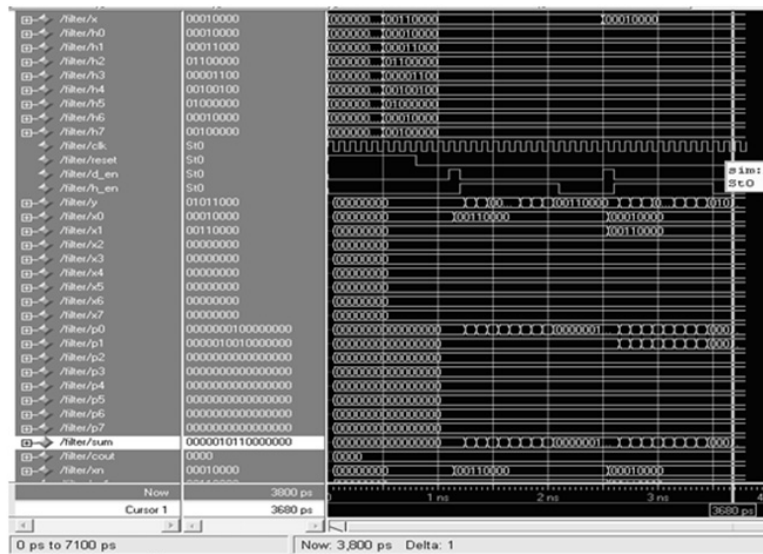
The following is the overall flow diagram of the adaptive filter module.



Results The Adaptive Filter



Filter Block



The design has been synthesized using Cadence Tool and the controller does the optimization based on the error level. The system is run at different frequencies and there by controlling the power consumption.

Report Area

Instance adaptive_filter
Cells 3234

| | |
|-----------|------------|
| Cell Area | 24679 |
| Net Area | 0 |
| Wireload | <none> (D) |

Report Power

| | |
|-------------------|-----------------|
| Instance | adaptive_filter |
| Cells | 3234 |
| Leakage Power(nW) | 22150.842 |
| Dynamic Power(nW) | 274304.828 |
| Total Power(nW) | 296455.670 |

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Conclusion

The design has been successfully tested as per the given specifications. Considerable amount of noise reduction has been achieved. The codes have been simulated in Xilinx and the desired simulation results are presented above.

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