

Internal Model Control Strategy based Cascaded 5 Level Inverter Type Dynamic Voltage Restorer for Power Quality Improvement

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Abstract

Usually PID controller does not possess the disturbance rejection capability. The internal model control (IMC) brings in a very good performance for set point tracking, but gives lethargic response for disturbance rejection problem. The study proposes a systematic procedure for pole-placement & IMC for PID controller tuning. The proposed control strategy is implemented in Cascaded 5 level inverter type dynamic voltage restorer (DVR). The case studies are presented to test the performance of the proposed control strategy. The test circuit is developed in Matlab/simulink and the results are presented to validate the proposed strategy.

Keywords: IMC, DISTURBANCE, DVR, POLE-PLACEMENT.

Introduction

For decades, power quality has been an exciting research topic for many scientists. Especially in the developing countries like India much research on this area is going on. The term “power quality” may be defined “*The powering and grounding of electrical equipment so as to maintain the safe operation of that equipment.*” Power quality assets are voltage sags, swells, interruption, transients, flickers and harmonics. Some methods have been proposed in recent times to classify the power quality problems [1]-[3]. These assets are very vital especially in distribution system. Among this power quality assets, voltage sag is the most frequently occurring problem. Voltage sags are usually caused due to faults in distribution system, motor starting and sudden increase of the loads etc. Voltage sags is defined as reduction of rms voltage to less than 1per unit for duration of 0.5 cycles to 3mins.

Due to increase of power electronic devices, the loads in the distribution system have become more sensitive. These sensitive devices have to be protected from various power quality problems especially voltage sags.

Dynamic voltage restorer (DVR) is a series connected device to mitigate the voltage fluctuations at the load end. There are many control strategy for the operation of DVR [4]-[5]. Most often used controller is PI controller, however tuning of the PI controller parameters is more difficult in industrial applications.

In recent past, engineers have developed improved tuning rules for PID controllers [6]-[10]. IMC PID tuning rule is one among them. IMC is more advantageous in compromising between closed loop performance & robustness. The main advantages of using IMC control for PID tuning compared to classic feedback controller are internal stability and performance characteristic that correlates directly to controller parameter [11]. If there is no model mismatch the perfect controller can be reached. When process dynamics are slower than the desired closed loop dynamics, IMC tuning rule provides adequate suppression of output disturbances and less suppression of load disturbances. However by including additional integrator in the output, additional load disturbance suppression can be obtained.

IMC controller complexity depends on two factors namely complexity of the model and performance requirements. This paper mainly focuses on design of IMC tuning rule for DVR application.

The paper structure as follows: Section II gives the brief description about the process. Section III and IV describes the internal model control strategy for PID tuning.

Process Description

As the DVR employs the isolated dc source, inverter and series injection transformer, it requires a filter at the output of the inverter to reduce the harmonics before the transformer. The fig 1 shows the process to be regulated. The circuit comprises of multilevel inverter with an output LC filter. As per fig 1, output voltage of filter is given by

$$V_s = \frac{1}{LCS^2 + RCS + 1} V_{inv} + \frac{LS + R}{LCS^2 + RCS + 1} I_L \quad (1)$$

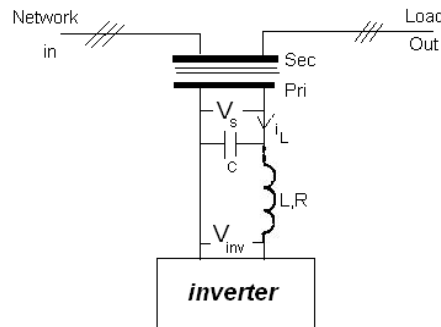


Figure 1: Process to be regulated.

V_s , V_{inv} , i_L is the filter output voltage, inverter output voltage and transformer primary current.

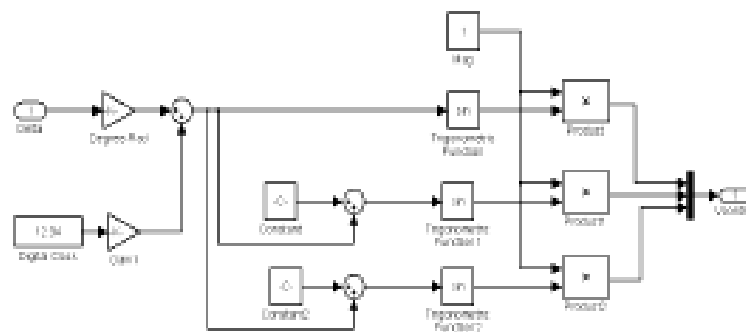
$$V_C = \sin(\omega t + \delta + 2\pi/3) \quad (3)$$


Figure 2: phase modulation of the control angle δ .

Classic Pi Controller

The circuit comprises of multilevel inverter with an output LC filter. As per fig 1, output voltage of filter is given by eqn (1). The function of the filter is to block the ripple frequency by its low pass function without modifying the reference signal. The eqn. (4) indicates that the output voltage of the filter is affected by the transformer

current as a disturbance. This disturbance has an adverse effect on the controller and indirectly on the dc energy source which has to supply the power required. Fig 4 represents the closed loop system of a plant with PI controller placed in feed forward path. The reference signals to be generated by DVR will be regulated by a PI or RST controller [13]. Parameters of regulation system ensures the short response time and acceptable reject perturbation caused by the load current i_L crossing the active conditioner and perturbing the injected voltage V_{inv} on the output filter capacitor terminals C. The plant (LC filter) transfer function is given by

$$G(S) = \frac{1}{LCS^2 + RCS + 1} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (5)$$

LC values are chosen to have cut-off frequency of 650 Hz. Assuming K_p and K_i be the proportional and integral gain values, the controller transfer function can be written as

$$C(S) = K_p + \frac{K_i}{s} \quad (6)$$

The closed loop transfer function of the system is given by

$$G_o(s) = \frac{G(s)}{1 + G(s)} \quad (7)$$

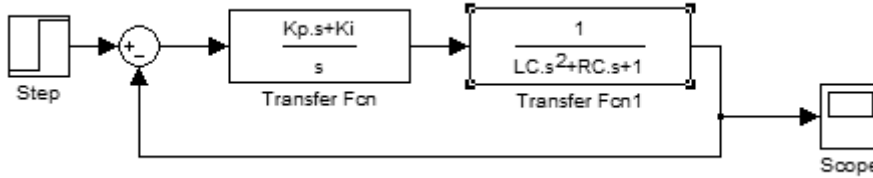


Figure 3: PI controller.

The characteristic equation of the closed loop system is given by

$$G(S) = s^3 + 2\zeta\omega_n s + (\omega_n^2 + K_p\omega_n^2)s + \omega_n^2 K_i \quad (8)$$

Where ε and ω_n are obtained from the plant transfer function by the formulae

$$\varepsilon = R/2 \omega_n L \quad (9)$$

$$\omega_n = \frac{1}{\sqrt{LC}} \quad (10)$$

Since $Gcl(s)$ is of third order form, it can be written as $P_1(s)P_2(s)$, where $P_1(s)$ corresponds to dominant pole and $P_2(s)$ corresponds to auxiliary poles chosen depending on poles of the plant. i.e., if plant poles are complex, then auxiliary poles

will be also complex. If complex pole is chosen as auxiliary, then it must have its conjugate. $P_1(s)$ & $P_2(s)$ are arbitrarily chosen as real and complex conjugate poles.

$G_{clp}(s)$ now can be written as

$$G_{clp}(s) = (s+a)(s^2 + 2\zeta_d \omega_d s + \omega_d^2) = P_1(s)P_2(s) \quad (11)$$

The values of a , ζ_d and ω_d are chosen arbitrarily in order to modify the rise time, zero steady state error and less settling time

$$a = 133, \zeta_d = 0.02 \text{ and } \omega_d = 4851.96 \text{ rad/sec.}$$

Substituting these values in eqn. 11

$$G_{clp}(s) = s^3 + 33.130s^2 + 25689.8s + 314761218 \quad (12)$$

Equating eqns. (10) and (12), values of K_p and K_i are obtained.

The step response of the system with PI controller with and without step disturbance is shown in fig 5 and Fig 6.

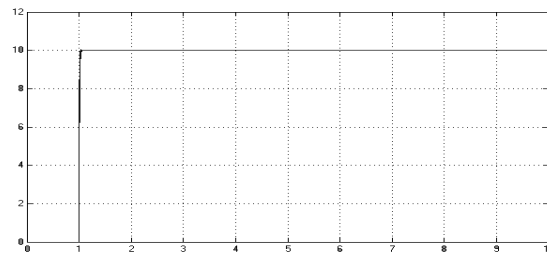


Figure 4: Step response of closed loop system with PI controller without disturbance.

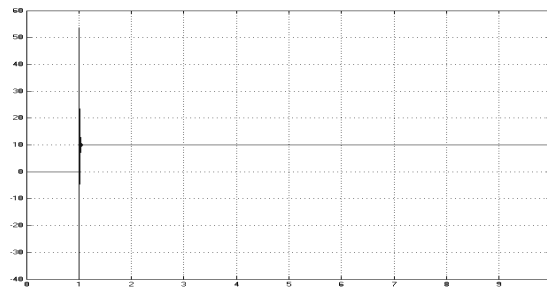


Figure 5: Step response of closed loop system with PI controller and disturbance of $u(t)=5$.

PI controller does not have disturbance rejection capability. So it cannot track the input signal accurately in the presence of disturbance (spike at $t=1\text{sec}$) as shown in fig 6. This disturbance will increase the stress on the PWM controller and indirectly increase dc energy required. The controller input is an error signal obtained as a difference of the reference voltage and r.m.s value of the terminal voltage (with

disturbance) measured. Such error is processed by a PI controller and output is provided to the carrier PWM signal generator. It is important to note that in this case, indirectly controlled converter, there is active and reactive power exchange with the network simultaneously: an error signal is obtained by comparing the reference voltage with the r.m.s voltage measured at the load point.

Internal Model Controller (IMC)

IMC (internal model controller) is one of the robust controllers, which can be designed with both one degree and two degree of freedom. Here, IMC is designed with one degree of freedom. Moreover robustness can be measured based on stability and disturbance rejection. In this project, IMC is designed for reference tracking with disturbance rejection.

o Design Procedure:

- Select the plant $G(s)$
- Select the plant model $G_m(s)$.
- Partition the plant model into minimum phase and non-minimum phase (all pass) components i.e non-invertible and invertible components. Non-invertible component $G_m^-(s)$ contains the terms, if inverted leads to instability and realisability problems. For example zeros in right hand plane and delays. Remaining terms of the plant model will be invertible component $G_m^+(s)$.
- $G_m(s) = G_m^+(s) G_m^-(s)$
- Set $q(s) = G_m^+(s)^{-1}$. If $q(s)$ is improper then $q(s)$ should be multiplied by low pass filter.
- Set $G_{imc}(s) = G_c(s) * G_f(s)$ where $G_f(s) = 1/(\tau s + 1)^n$ where n value is chosen so as to make the $G_{imc}(s)$ proper.
- $G_{pid}(s) = \frac{G_m^+(s)^{-1} G_f(s)}{1 - G_m^-(s)^{-1} G_f(s)}$ (13)
- Select value of τ depending on robust stability. τ value also shapes the sensitivity function.

Consider the Block diagram of an IMC system is shown in below fig 6:

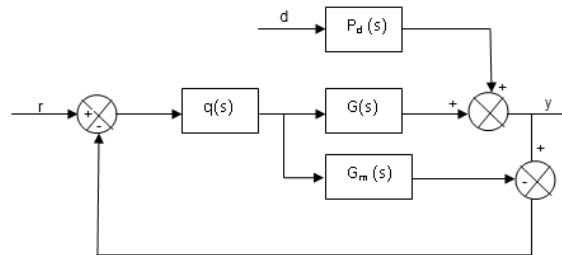


Figure 6: Block diagram of IMC.

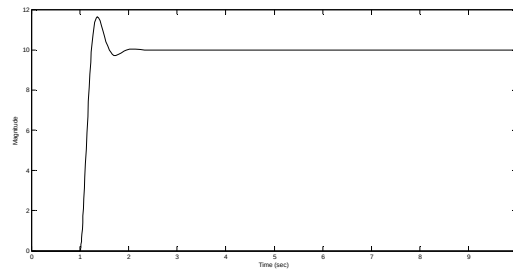


Figure 7: Step response of closed loop system with IMC controller without disturbance.

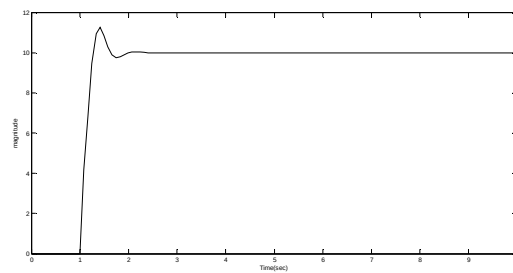


Figure 8: Step response of closed system with IMC controller with step disturbance of $u(t)=2$.

Test System

The test parameters are

$$L=3\text{mH}, C=20\mu\text{F}, R=1\text{ohm}$$

With pole placement technique,

$$K_p = 0.4142 \text{ and } K_i = 188.858$$

With IMC technique

$$\tau = 0.1, G_m^+(s) = \frac{1}{LCS^2 + RCS + 1}, G_m^-(s) = 1$$

$G_f(s) = 1/(\tau s + 1)^n$. n is 2 for PI controller and 1 for PID.

Single line diagram of the test system for DVR is shown in fig 9:

The test system is employed to carry out the simulation of DVR in fig 10: such system is composed by a 13KV, 50HZ generation system. Feeding two transmission lines through a 3 winding transformer connected in Y/ Δ / Δ , 13/115/15 KV such transmission lines feed two distribution networks through two transformers connected in Δ /Y 15/11KV. To verify the working of a DVR employed to avoid voltage sags and to mitigate the voltage disturbance at the utility end. The capacity of D.C storage device is 5KV.

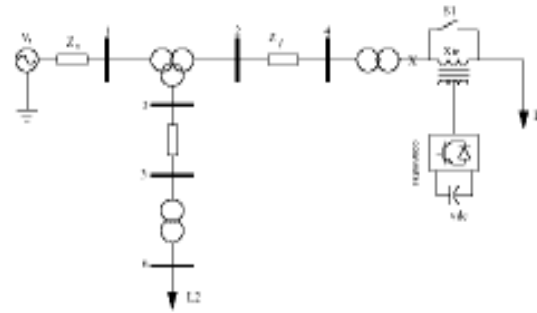


Figure 9: single line diagram of the test system for DVR.

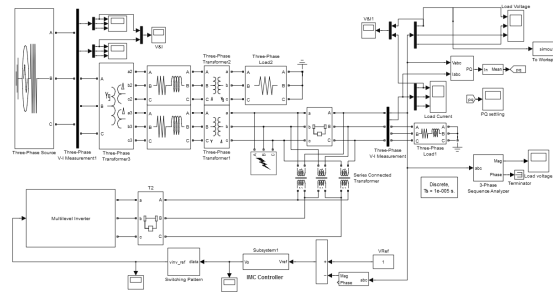


Figure 10: Simulink model of DVR test system.

Case 1: A triple line fault is created with fault resistance of 0.66ohms at point x in the fig 7. This fault results in a voltage sag of 20% in the load voltage. The fault is created for duration of 0.5 to 0.8ms. The load voltage is depicted as shown in the fig 11.

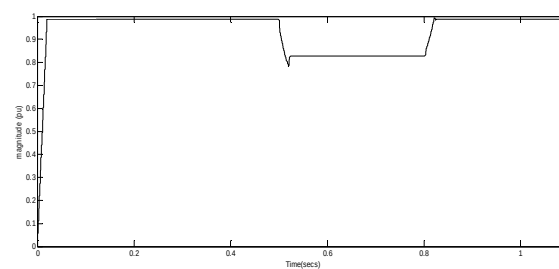


Figure 11: Load voltage without DVR with three phase fault (fault resistance (0.66ohms)).

When DVR is operated during abnormal condition, load voltage is resumed to 98% as shown in fig 12. The load voltage waveform is same for IMC and PI controller. With IMC DC source voltage is reduced to 2KV compared to 2.5KV with PI.

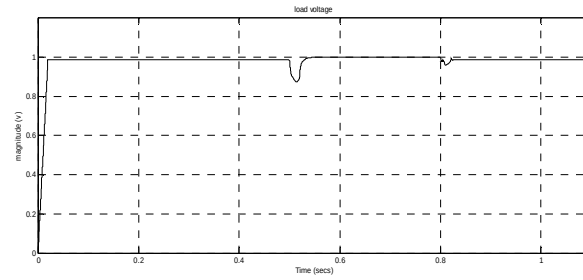


Figure 12: Load voltage with DVR.

To simulate the both control strategies are simulated in MAT lab Simulink the results are presented to verify the performance of the both control strategies for DVR.

Case 2: A triple line to ground fault is created with a fault resistance of 0.001 ohms at point x in the fig 7. This fault results in a voltage interruption in the load voltage. The load voltage is shown in the fig 13.

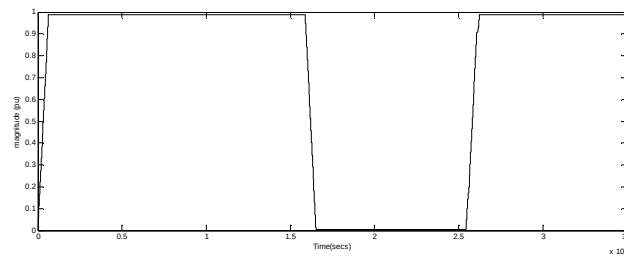


Figure 13: Load voltage without DVR with three phase to ground fault (fault resistance 0.001ohms).

When DVR is operated during abnormal condition, load voltage is resumed to 98% as shown in fig 14. The load voltage waveform is same for IMC and PI controller. With IMC DC source voltage is reduced to 2.3 KV compared to 2.8KV with PI.

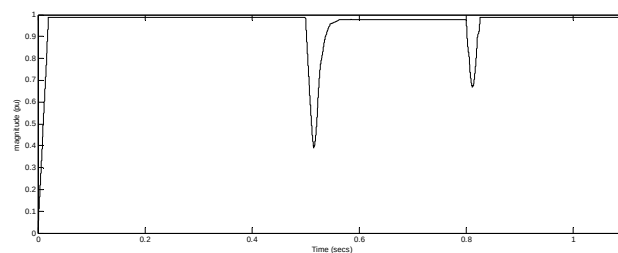


Figure 14: Load voltage with DVR.

Conclusion

- The test system employing the cascaded multilevel inverter type DVR is modeled in matlab simulink.
- Two different control strategies namely, pole placement and internal model control for PI tuning is discussed briefly.
- The use of multilevel inverter as voltage source converter reduces the dc requirement and filter rating further reducing the cost for dc storage & the filter.
- Pole placement design methodology is discussed briefly for PI tuning.
- The figs depict that PI controller cannot track the reference signal in the presence of disturbance.
- Internal model control design is presented for PI tuning.
- With this method, PI gains the disturbance rejection capability as shown in the fig
- The comparison between Pole-placement and IMC are as follows

Type of the control strategy	DC voltage requirement	THD	Robustness (disturbance Rejection)
Pole placement	2.5KV	No effect	No
IMC	2KV	Reduces	Yes

- With IMC strategy, DC storage requirement can be reduced resulting in reduction of the cost.
- IMC strategy has further advantage that due to disturbance rejection capability, the controller produces accurate δ based on which pulse generator produces pulses for the inverter reducing stress on the pulse generator.
- From the table IMC strategy is very effective and robust compared to Pole-placement method

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