

Simulation of Acquisition behavior of Second-order Analog Phase-locked Loop using Phase Error Process

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Abstract

This work presents a method for modeling and simulating a second-order analog phase-locked loops (PLL) in time domain for studying its acquisition behavior. The proposed method uses phase error process for analyzing the PLL characteristics. The method enables to study the lock-in and pull-in phenomena of analog PLL and the effects of changing phase offset and voltage offset values on acquisition behavior. The method combines mathematical level modeling of voltage controlled oscillator and phase detector with circuit level modeling of the loop filter. The complete simulation program for the entire PLL system is written in Turbo C. The MATLAB program is used for graphical analysis of simulated data. The simulation results show that the method can be applied to verify the PLL characteristics during acquisition.

Keywords: Phase Locked Loops, Acquisition behavior, Phase error, Lock-in, Pull-in, Cycle slip.

1. Introduction

The Phase-locked loop (PLL) is an indispensable sub-system in a many general and special purpose communications systems now-a-days. The PLL system is used

extensively in modern electronic systems, such as modems, mobile communications, satellite receivers and television systems. The simulation of PLL is considered essential in view of rapid improvement in the field of Integrated Circuit (IC) technology. Simulation helps in understanding both linear and non-linear behavior of the PLL system. The linear analysis is done with the assumption that phase error is small. The cycle slip is a non-linear phenomenon and it occurs when the phase error exceeds the value of phase error limit. A basic PLL system consists of multiplier, used as phase detector (PD), loop filter (LF) and a voltage controlled oscillator (VCO) shown on Fig. 1. The theories of PLL systems have been analyzed in details in the literature [1]-[8]. It is observed that the PLL system is already well established by its theoretical works and practical applications. However different methods are being used for studying and for further improving various performance parameters of PLL.

The motivation behind this work is to simulate the acquisition behavior of PLL with the objective of determining locking parameters such as lock-in, pull-in, phase and voltage offset using phase error process in time domain. The work is mainly based on circuit level modeling of the LF combined with mathematical model representation of the multiplier and the VCO.

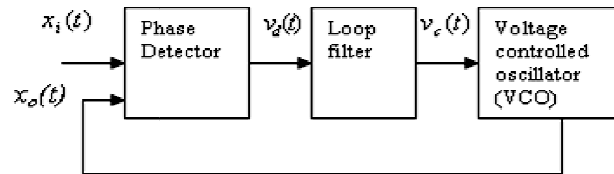


Fig. 1: Block diagram of PLL

2. Brief Overview of PLL Behavior

A PLL is an electronic system which control the phase of its output signal in such a way that phase error between VCO output signal phase and input reference signal phase reduces to a minimum. Multiplier performs a mixing operation between the input reference and VCO signals. This mixing is true analog multiplication and the output of the multiplier is a function of signal amplitudes, frequencies and phase of the inputs. The phase error between VCO signal and the input reference signal is quantified by the multiplier used as PD. The output of the PD is processed by the LF and the output is applied to the input of the VCO. The output of the LF controls the phase and frequency of the VCO.

If the reference input and VCO frequencies are not equal, the output of the LF will be an increasing or decreasing voltage depending on which signal has the higher frequency. This change in frequency is tracked by a change in the LF output, and thus forcing the VCO free running frequency to capture the reference input frequency. The PLL system usually operates either in the acquisition mode or in the tracking mode. In the acquisition mode, the PLL system is either out of lock or just starting up to lock

with the input reference signal. In tracking mode, the PLL is already locked and it tries to maintain the locking condition even in the situation of sudden change of phase and frequency of the input signals.

3. The Basic Components

The multiplier used in PD is a very important part of PLL system since it compares the input reference and the VCO signals simultaneously. If both inputs to the multiplier are sinusoidal then the mixing operation is true analog multiplication and the output is a function of input signal amplitudes, frequencies and phase relationships. The multiplication of two input signals makes analog PLL well suited for much special purpose application. The multiplier type PD can work well up to the microwave frequency region. Such multipliers can provide adequate performance when the input signal is buried in noise. The error computed by the multiplier is the difference between the instantaneous phases of two input signals.

The PLL filter is required to remove any high frequency components which may pass out of the multiplier and may appear along with the input signal to the VCO. Finally this unwanted signal may appear at the output of the VCO as noise signal. The LF plays a crucial role to the operation of the whole PLL system and it is used to determine the overall response of the system. The choice of the values of the circuit elements must be balanced in view of a numbers of conflicting requirements. The transient performance of the PLL system is governed by the chosen values of the components of the LF.

The VCO is an oscillator that works with reference to a quiescent frequency. It produces an output signal that is proportional to the input control voltage. The input control voltage corresponds to some filtered form of the phase error. In response to this, the VCO adjusts its output frequency. The practical VCOs are designed to meet the requirements such as (i) phase stability (ii) large frequency deviation (iii) high modulation sensitivity (iv) linearity of frequency versus control voltage. These requirements are usually in conflict with one another and therefore a compromise is needed.

4. Modeling of the System

A. System level modeling of PD and VCO: The multiplier performs a mixing operation between the input reference and VCO signals. The PD produces an output signal which is proportional to the phase difference between its two input signals i.e.

$$\begin{aligned} v_d &= K_d \sin(\theta_i - \theta_v) \\ &= K_d \sin(\phi) \end{aligned} \quad (1)$$

Where θ_i is the phase of the input reference signal, θ_v is the phase of the VCO output signal, ϕ is the phase error between the two signals and K_d is the multiplier gain in volts/rad.

The instantaneous output frequency f_{inst} of the VCO is a linear function of the LF output voltage V_c with reference to the VCO free running frequency f_0 . The deviation of VCO output frequency from its free running frequency f_0 is expressed as $K_v V_c$, where K_v is the VCO sensitivity and it has the unit of radians per second per volt. The the instantaneous output frequency f_{inst} becomes equivalent to the input frequency f_i . So the mathematical relations for VCO are appropriately written as:

$$\begin{aligned} f_{inst} &= f_o + K_v V_c = f_i \\ \Rightarrow V_c &= \frac{f_i - f_o}{K_v} \\ \Rightarrow V_c &= \frac{\Delta f}{K_v} \end{aligned} \quad (2)$$

In Eq.2, Δf is the frequency difference at the input of the multiplier. This equation is important as it gives an idea of LF output voltage or VCO control voltage V_c required for determining PLL parameters such as Lock-in, Pull-in etc.

B. Component level modeling of LF: LF is a very important component as it determines the stability, settling time, noise performance and lock range of the s PLL system. The LF used in this work is of lag-lead type as shown in the Fig. 2. This is the most common type of LF that is normally used in analog PLL system. This LF is of linear dynamic type and its equivalent circuit may be represented by transient solution method of linear dynamic network [9]. The charge-storage element capacitor must be reduced to simplified equivalent circuit known as linear companion network model used in SPICE [10] simulation software. A capacitor is transformed by using a two step process.

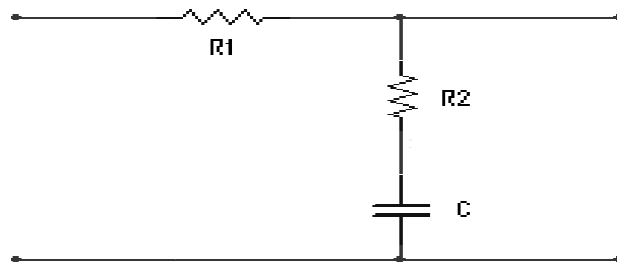


Fig. 2: The Loop filter.

The first step is to apply numeric integration to the current-versus-voltage relationship of a capacitor. The next step is to use the result to develop the linear companion model suitable for applying nodal analysis. The method transforms capacitor by applying a numeric integration to the current-versus-voltage relationship of a capacitor i.e.,

$$i_c = C \frac{dv_c}{dt} \tag{3}$$

This derivative is approximated numerically by using the backward Euler formula. Backward Euler offers a good compromise of accuracy and stability. The approximation of the derivative in Eq.3 is written as

$$\left. \frac{dv}{dt} \right|_{t=t^{n+1}} \approx \frac{v^{n+1} - v^n}{t^{n+1} - t^n} \tag{4}$$

Where the “n” superscript refers to a particular time point and it is assumed that the difference between successive time points is constant i.e.

$$t^{n+1} - t^n = T \tag{5}$$

Where, T is called the time step or step size. Now Eq.3 is approximated by using Eq.4 as

$$i_c^{n+1} = C \frac{(v^{n+1} - v^n)}{T} \tag{6}$$

The current $I_c^{(n+1)}$ is an approximation to the true capacitor current. The linear companion model representation for a capacitor follows from Eq.6 by viewing this equation as a Kirchoff’s Current Law (KCL) at a branch node as shown in the Fig. 3.

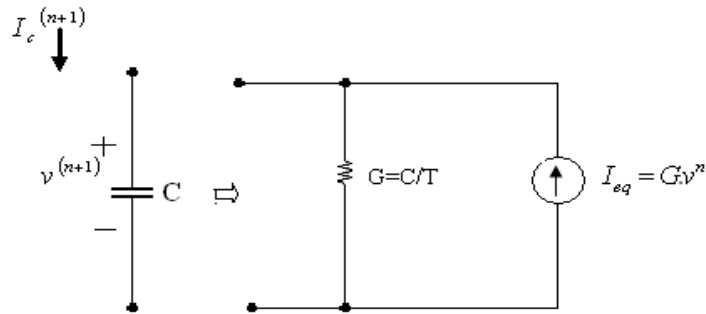


Fig. 3: Companion network model of capacitor.

Conductance G describes the part of C’s current dependent on its new voltage $v^{(n+1)}$. The current source $I_{eq} = G \cdot v^n$ describes the other part based on the past voltage.

Since v^n is the node voltage from previous time step and remains fixed, only $v^{(n+1)}$ changes with each new iterative voltage value and $I_c^{(n+1)}$ changes to become the linear I-V relation for the new capacitor voltage at that transient time point. The nodal equations for LF are represented in a set of matrices as $[G][V]=[I]$. This matrix characterizes the linear representation between the voltage and current for every element in the LF circuit. At each discrete time point, the numeric integration determines the linear I-V relationship for the capacitor. The value of the resistors R1 and R2 of LF are represented by its conductance value in the system matrices.

5. The Acquisition Mode

The lock-in and pull-in parameters are related to acquisition mode of PLL when its output is either out of lock or just starting up to lock with the input reference signal. At higher frequencies the loop gain of a first order PLL is defined as $K=K_v K_d F(\infty)$. Where $F(\infty)$ is known as high frequency asymptotic response [1] of lag-lead filter. For lag-lead filter $F(\infty) = \tau_2/\tau_1$ where $\tau_1 = (R_1+R_2)C$ and $\tau_2 = R_2C$. As a fair approximation, the same gain value is assumed for a second order PLL with a lag-lead filter [1][7].

When the input reference signal frequency is close to the VCO free running frequency i.e. the value of Δf is small then the PLL locks with just a phase transient and there will be no cycle slipping before the locking. This frequency range over which the PLL acquires phase locked without cycle slip is known as Lock-in limit (Δf_L). The lock-in limit for a second order analog PLL with lag-lead filter is approximately estimated as

$$\Delta f_L \approx K_v K_d F(\infty) \quad (7)$$

If the initial frequency difference is very large or the LF output is very small, then the loop cannot pull in. The maximum frequency range for which the loop can still lock is known as Pull-in limit and is denoted by Δf_p . An approximate formula for pull-in limit is defined as

$$\Delta f_p \approx \sqrt{2 K_v K_d K} \quad (8)$$

6. The Simulation

The literature [11]-[13] have discussed some important points about PLL simulation. Some of the important points regarding PLL simulation are the presence of high frequency signal with low frequency time constants, difficulty in observing the dynamics of the entire loop with small simulation step etc. So it is recognized that the PLLs are inherently difficult systems to fully and accurately simulate. Simulation speed and modeling accuracy are other two important aspects that decide the usefulness of a particular simulation tool.

A. Simulation method: The method presented in this paper simulates the PLL system in time domain to study the acquisition behavior by using the phase error process. The method is based on the combination of component level modeling of LF and mathematical modeling of VCO and the multiplier PD [14] for complete simulation of PLL system. As used in SPICE based software, the LF is represented by its equivalent companion network model. The nodal equations for companion network model are represented in a set of matrices which characterize the linear representation between the voltage and current for every element in the circuit. The set of nodal matrices are then solved for node voltages using an iterative method.

The simulation program is written in Turbo C for the complete PLL system. The program extracts phase information from the input signals and then computes the phase error between them during acquisition process. The method restricts phase error variable ϕ between $-\pi/2$ to $+\pi/2$ in case of sinusoidal PD with normal linear region of operation and between $-\pi$ to $+\pi$ in case of sinusoidal PD with extended linear region of operation. The MATLAB programs are used for graphical analysis of data for observing the cycle slip phenomena at the extreme end of phase error values while determining the lock-in limit and pull-in limit.

B. Matrix solution: Iterative method is used to solve the matrices by the method of approximations. The process starts with an initial guess. Then successive solutions are found by using the previous solution as the guess for the next iteration. Thus approximations are used at each step to converge to a solution. Iterative method used here is the Gauss-Seidel method [15] which is helpful to control the round-off error. An error tolerance value is set beforehand for checking the convergence conditions and it is checked with absolute relative approximate error after each iteration. If successive solutions lie within a pre-specified tolerance interval then the solutions are assumed to have converged.

7. The Algorithm

The flowchart shown in the Fig. 4 combines the SPICE based algorithm for component level simulation of LF with mathematical modeling of VCO and the PD. The block 1 represents the source of sinusoidal input reference signal. The block 2 represents the mathematical model of multiplier used as PD and the block 14 represents the mathematical model of the VCO. The block 2 multiplies the sinusoidal signals generated by the block 1 and the block 14. The SPICE based circuit level simulation algorithm starts from block 3 after analyzing the output from block 2. The block 3 is the initial guessing of an operating point for starting the simulation of LF. The inner loop (4 - 6) is used for finding the solution for LF components. The linear circuit element resistor and the non linear circuit element capacitor of the LF are replaced by its equivalent linear model known as companion network model in block 4. In this inner loop, the blocks 5 and 6 are used for nodal analysis and for solving the nodal equations for circuit voltage. Gauss-Seidel iterative method is used for the solution of

nodal matrix $[G] \times [V] = [I]$. It may take number of iterations before the calculations converge to a solution. The outer loop (7- 9) along with the inner loop is used for calculating time step T and time points for performing a transient analysis. Then a new operating point is chosen based on the new voltages and then the same process is started all over again. The solution is said to be converged when the circuit voltage falls below some predefined value from one iteration to the next.

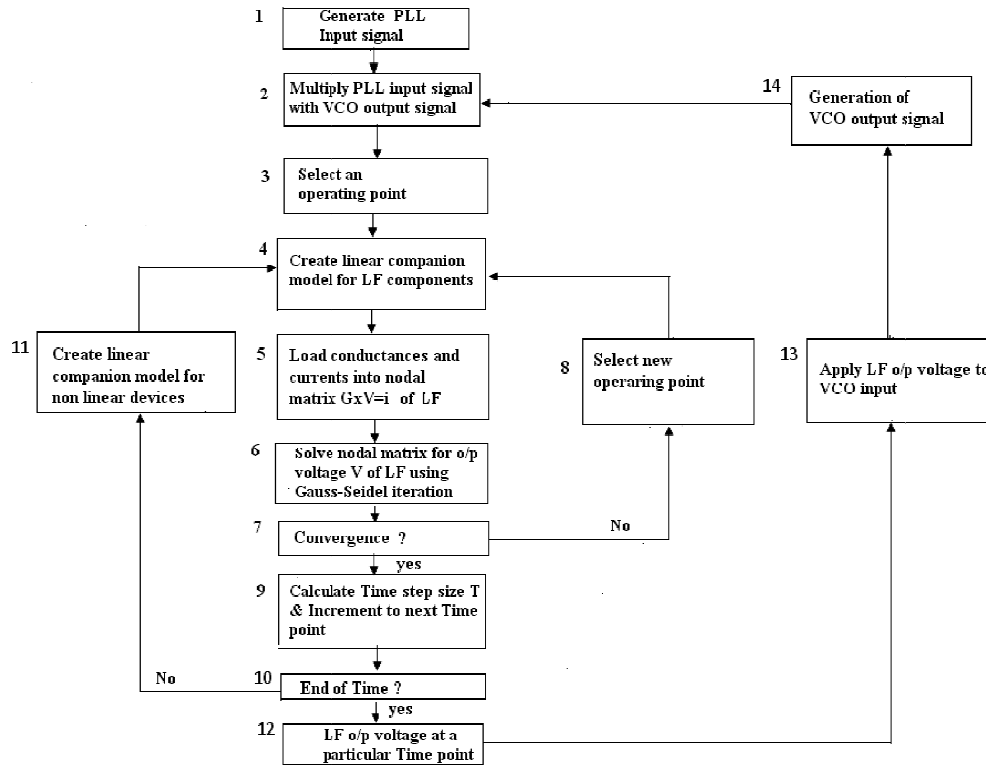


Fig. 4: Flowchart of PLL simulation.

The Table 1 shows the PLL parameters along with symbols and values for a typical example for simulation.

Table 1: PLL parameters for simulation

Sl. No	PLL Parameters for Simulation	Symb ol	Value
1	Simulation time step	T	10^{-8} second
2.	Resistance	R1	88 K Ω
3.	Resistance	R2	6 K Ω

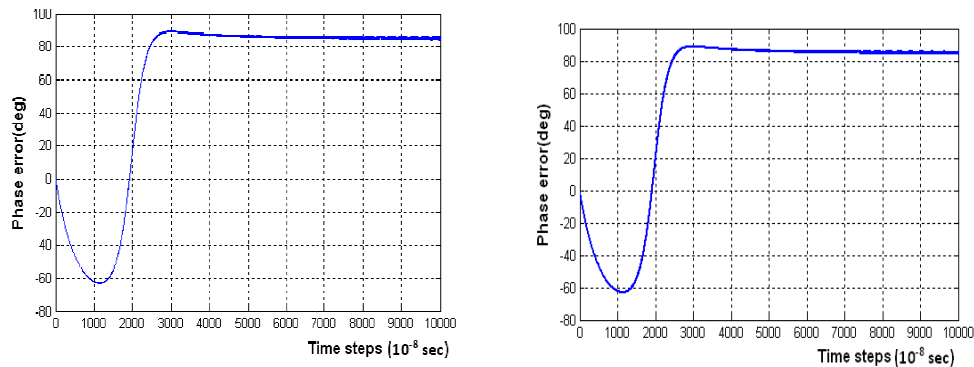
4.	Capacitor	C	1.6 nF
5.	VCO free running frequency	f_0	10 MHz
6.	VCO gain	K_v	1 MHz/volt
7.	Amplitude of input reference signal	A_i	1 Volt
8.	Amplitude of VCO output signal	A_v	1 Volt
9.	Multiplier gain	K_d	0.5Volt/radian
10.	High frequency asymptotic response of filter	$F(\infty)$	0.0632
11.	Theoretical value of lock-in limit	Δf_L	32 KHz
12.	Theoretical value of pull-in limit	Δf_P	178 KHz
13.	Damping factor	ζ	0.7
14.	Loop natural frequency	f_n	22450 Hz

8. Results and Discussion

The simulation results are discussed in four parts as follows:

8.1 Acquisition behavior during lock-in

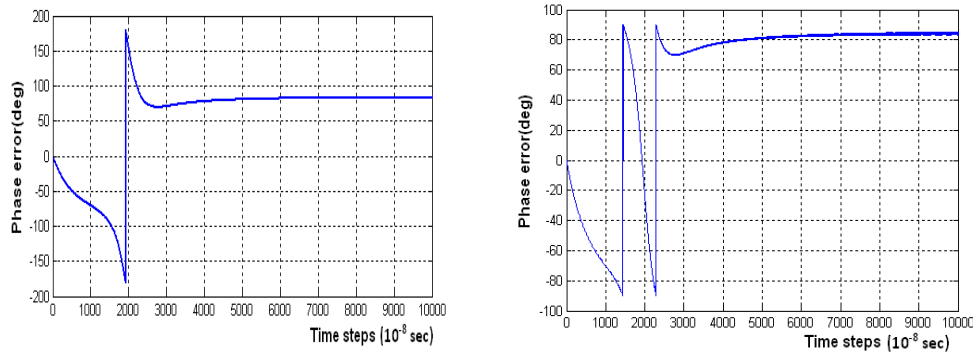
The Fig. 5 gives the simulation response to observe the acquisition behavior at $\Delta f=40$ KHz. The program has been run with the input reference frequency f_i , set at 10.040 MHz and the VCO free-running frequency f_0 , fixed at the value of 10 MHz. The Fig. 5 (a) and (b) show the similar phase error behavior without cycle slip for the two PDs with phase error $-\pi$ to $+\pi$ and $-\pi/2$ to $+\pi/2$. In this situation, the PLL is said to be locked at lock-in value of $\Delta f=40$ KHz after phase error transient for duration of around 30 μ sec. This extended phase error response in Fig. 5 (a) and (b) occurs as the damping factor value is less than 1.



(a) PD with phase error range $-\pi$ to $+\pi$ (b) PD with phase error range $-\pi/2$ to $+\pi/2$

Fig. 5: Acquisition behavior at $\Delta f=40$ KHz ($\zeta=0.7$ and $f_n=22450$ Hz)

The Fig. 6 gives the simulation response to observe the acquisition behavior at $\Delta f=41$ KHz. It is observed in Fig. 6 (a) that there is cycle slip at 19.24 μ sec and the steady state starts at around 50 μ sec. However in Fig. 6 (b), the same has occurred at 14.39 μ sec and the locked state starts at around 70 μ sec. The phase error behavior is not similar in Fig. 6 (a) and (b) due to the occurrence of cycle slip at $\Delta f=41$ KHz. The value of $\Delta f=40$ KHz is said to be the lock-in limit for PLL simulated with parameters as per Table 1.

(a) PD with phase error $-\pi$ to $+\pi$ (b) PD with phase error $-\pi/2$ to $+\pi/2$ **Fig. 6:** Acquisition behavior at $\Delta f=41$ KHz ($\zeta=0.7$ and $f_n=22450$ Hz)

8.2 Acquisition behavior during Pull-in

The Fig. 7 gives the simulation response to observe the acquisition behavior at $\Delta f=180$ KHz. Here the input reference frequency f_i has been set at 10.180 MHz and the VCO free-running frequency f_0 fixed at the value of 10.00 MHz. It is observed that with the increasing value of $\Delta\omega$, the pull-in is still taking place. As the initial frequency difference increases, the gain of the multiplier is reduced and so the LF output is not sufficient to push the VCO free-running frequency towards input signal. So the number of cycle slips increases sharply with the increasing value of Δf . The simulation result in the Fig. 7 (a) shows that with phase error range of $-\pi$ to $+\pi$, the number of cycle slip is 7 and the locked state starts at around 150 μ sec and for the PLL with phase error range of $-\pi/2$ to $+\pi/2$, the number of cycle slip is 14 and the locked state starts at around 200 μ sec. It is observed that the PLL achieves the locked state with a number of cycle slips at the cost of additional acquisition time and the PLL with extended linear region of operation is quick to achieve the locked state with less number of cycle slips. The value around $\Delta f=180$ KHz may be considered as pull-in limit (depending upon the tolerance range) for the PLL simulated in this work using the parameters as per Table 1.

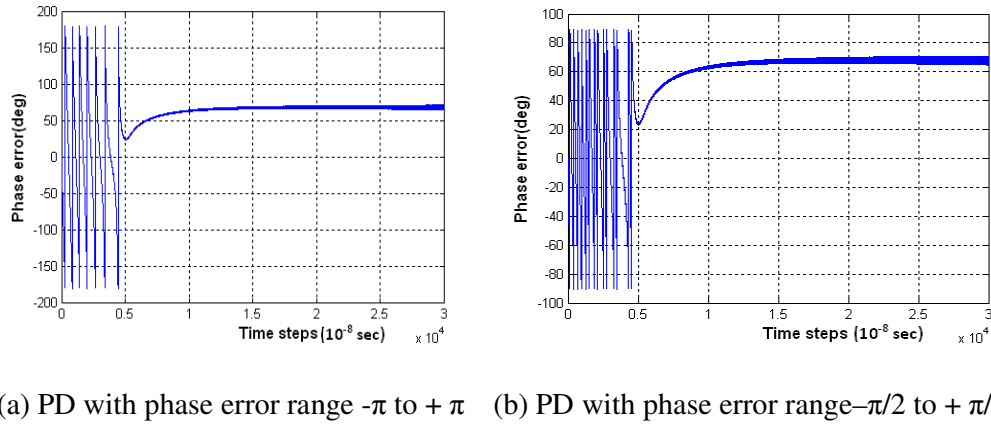


Fig. 7: Acquisition behavior during pull-in at $\Delta f=180$ KHz ($\zeta=0.7$ and $f_n=22450$ Hz)

8.3 Acquisition behavior with initial VCO phase offset

The Fig. 8 shows the comparison of the phase error transients before lock-in for different values of initial phase offset of the VCO signal with reference to the input reference signal.

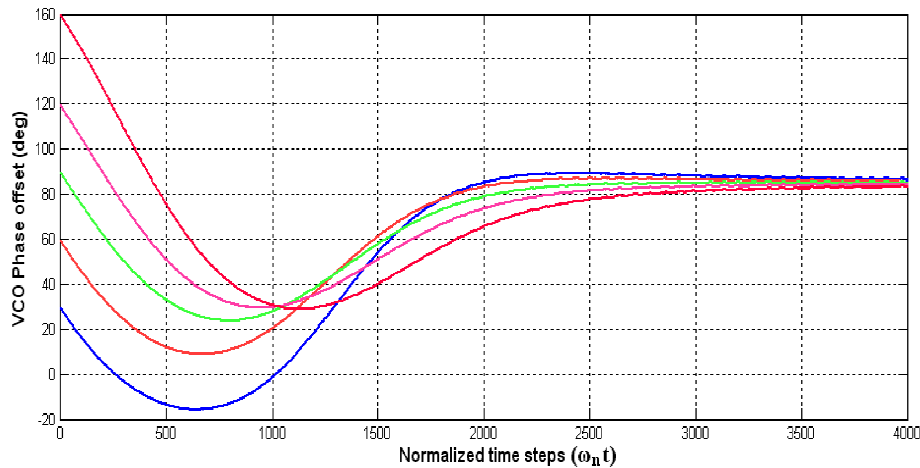


Fig. 8: Acquisition with initial VCO phase offset at $\Delta f = 40$ KHz ($\zeta=0.7$, $f_n=22450$ Hz)

The phase offset values range from 30^0 to 160^0 for $\Delta f =40$ KHz. It is observed that as the initial phase offset of the VCO increases, the settling time required for lock-in is increased. The phase error transient at the offset value of 15^0 is the fastest to attain lock-in state whereas at offset value of 160^0 , the phase error transient is slow to attain lock-in.

8.4 Acquisition behavior with PD dc offset

The Fig. 9 shows the undesirable affects on acquisition due to the presence of dc offset voltage at the output of the PD. It is observed that as the value of the dc offset voltage is increased, the region of operation of phase error is drifting away from the expected region of operation. So the dc offset values up to $10\mu\text{volt}$ may be set as limit for this simulated PLL as the

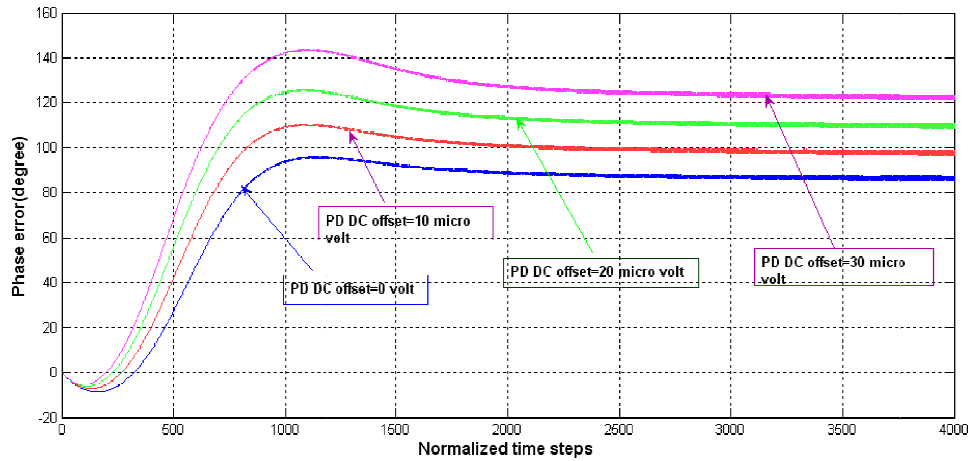


Fig. 9: Acquisition behavior with PD dc offset ($\zeta=0.7$, $f_n = 22450$ Hz)

DC offset voltage beyond this causes a variation by more than 10 degree (assuming a 10% tolerance value with reference to the expected 90 degree).

9. Conclusion

This paper presents a simulation tool for analyzing second-order analog PLL. The aim of this simulator is to quickly and accurately determine the PLL locking parameters during acquisition. The simulator is useful for studying the PLL characteristics for different parameters of the VCO, the multiplier and the LF. The simulation tool is one complete program for the whole PLL system with uniform simulation time step size. The tool, written in Turbo C, has the advantage of flexibility and improved accuracy and speed. The method has the added advantage of post processing the simulated data using MATLAB. The time domain aspect of the simulator helps in observing the actual shape of signals at desired time intervals. This time domain aspect is important when the simulation is run for long time.

The PLL locking parameters such as lock-in and pull-in have been observed using phase error process. The phase error transient phenomena have been compared both for the normal linear ($+\pi/2$) and the extended linear ($+\pi$) region of operation of PD characteristic. It is observed that the reduced linear zone of the PD characteristic leads

to more number of unwanted cycle slips and more locking time during acquisition process. The effects of initial VCO phase offset with reference to input reference signal and the PD dc voltage offset on acquisition are observed. The simulator program uses uniform time step size of 10^{-8} second to accurately represent the high frequency input signals to the PLL system. The simulation program has been run for maximum of 30000 time steps or 300 μ sec to allow the dynamics of the PLL to be examined. The accuracy of the simulator is confirmed with the observation that the theoretical values known from literature of PLL has been found to be almost similar with the simulated values.

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