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Hybrid Modulation Technique for Cascaded Multilevel Inverter for High Power and High Quality Applications in Renewable Energy Systems

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Abstract

The objective of the work is to improve multilevel power electronic converter topologies for high quality and high power applications with specific emphasis on renewable energy systems. The rapid evolution of renewable energy within the last several years has resulted in the design of efficient power converters suitable for medium and high-power applications such as wind turbine and photovoltaic (PV) systems. Today, the industrial trend is moving away from heavy and bulky passive components to power converter systems that use more and more semiconductor elements controlled by powerful processor systems. However, it is hard to connect the traditional converters to the high and medium voltage grids, as a single power switch cannot stand at high voltage. For these reasons, a new family of multilevel inverters has appeared as a solution for working with higher voltage levels. This paper presents four different sequential switching hybrid-modulation strategies and compared for cascaded multilevel inverters. Hybrid-modulation strategies represent combinations of fundamental-frequency modulation and multilevel sinusoidal-modulation (MSPWM) strategies, and are designed for performance of the well-known alternative phase opposition disposition, phase-shifted carrier, carrier-based space-vector modulation, and single-carrier sinusoidal-modulations. The main characteristic of these modulations are the reduction of switching losses with good harmonic performance, balanced power loss dissipation among the devices with in a cell, and among the series-connected cells.

Index terms: Cascaded Multilevel Inverter, Fuzzy Logic Controller, Pulse Width Modulation.

Introduction

Multilevel inverters (MLIs) are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation. Various multilevel inverter (MLI) structures are reported but the cascaded MLI (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI). CMLI synthesizes a medium voltage output based on a series connection of power cells that use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy.

Many new modulations have been developed to cater the growing number of MLI topologies. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency and phase fundamental component that is usually a sinusoid in steady state. Since the modulation scheme is intended to be used in high power converters, the main figures of merit pursued are high power quality and minimum switching frequency. These two requirements compete with each other and are considered one of the major challenges in MLI technology.

Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition (APOD) PWM), or with horizontal displacements (phase-shifted carrier (PSC) PWM) Space-vector modulation (SVM) is also extended for the MLI operation, offers good harmonic performance.

Features of Multilevel Inverters

A multilevel inverter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The main features of a multilevel inverter are,

- Staircase waveform quality
- Common-mode (CM) voltage
- Input current
- Switching frequency

Multilevel Inverter Topologies

Multilevel inverter topologies can be classified into three types as,

- Diode – clamped multilevel inverter
- Capacitor – clamped multilevel inverter.
- Cascaded multilevel inverter.

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less distortion, less high switching frequency, higher efficiency, lower voltage devices and better electro-magnetic compatibility. The commutation of the switches permits the addition of semiconductors must withstand only reduced voltages.

Modulation Techniques and Its Types

The inverter output can be changed and controlled according to the desired level by the triggering pulse given to the gate terminal in the inverter. This controlling method is obtained by a method called as modulation technique. There are several types of PWM modulation techniques for controlling the inverter output by changing the pulses given to the gate from the PWM modulation technique. The pulse is used as a triggering pulse for the gate terminal of the power devices which is used to ON and OFF the power devices.

The various pulse width modulation techniques for controlling the multilevel inverter topologies are step modulation, sinusoidal PWM, space vector modulation, selective harmonic PWM, modified sinusoidal PWM and multiple pulses PWM. Among this space vector PWM is now used in research and development areas but its algorithm is very complex having many number trigonometric functions, so this has less preference to use in the practical implementation.

Methodology

The objective of the proposed system is to reduce the switching loss of multilevel sinusoidal modulation (MSPWM) schemes with low computational overhead. Also, this covers the methodology for equal power dissipation among the power devices, and the power modules. The five-level case is presented here, and this method can be equally applied to any number of voltage levels, any number of phases, and switching transitions.

Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and MSPWM for each inverter cell operation, so that the output inherits the features of switching-loss reduction from FPWM, and good harmonic performance from MSPWM. In this modulation technique, the four switches of each inverter cell are operated at two different frequencies; two being commutated at FPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses, and therefore, differential heating among the power devices. A simple base PWM circulation scheme is also introduced here to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules.

PWM switching strategies not only addresses the primary issues viz, less THD, effective dc bus utilization etc but also take care of secondary issues like EMI reduction, switching loss, better spreading of Harmonics over the spectrum. Real-time method of PWM generation can be broadly classified into Triangle comparison based PWM (TCPWM) and Space Vector based PWM (SVPWM).

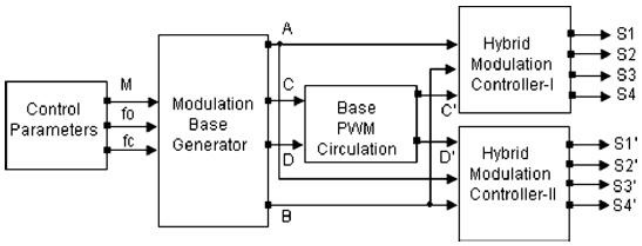


Figure 1: Scheme of proposed sequential switching hybrid modulation.

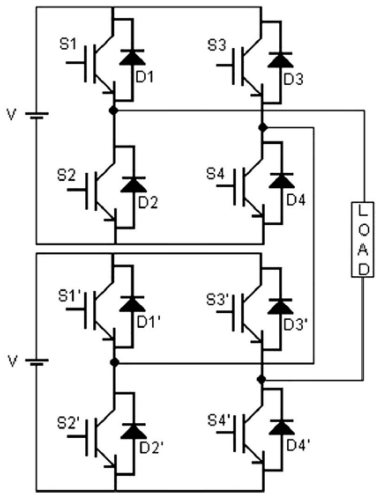


Figure 2: Schematic diagram of the inverter topology for hybrid modulation.

Space Vector Modulation

SVM is intrinsically a non-carrier-based digital technique for generating switching angles. However, due to the constant sampling rate used in SVM, equivalent carrier-based techniques have been developed. Carrier-based SVM is appropriate for inverters with more than five levels, where the computational overhead for conventional SVM is exceeded due to many output states. This strategy is known as carrier based space vector pulse width modulation (CBSVM). These high-frequency methods produce high frequency stepped-voltage waveforms that are easily filtered by the load and, therefore, present very good reference tracking and low-current harmonic distortion. However, this also causes high switching losses, which is undesirable in high-power applications.

The principle behind this hybrid modulation is to mix fundamental frequency PWM and carrier based space vector modulation for each inverter module of a cascaded multilevel inverter. Therefore, the output contains the features of fundamental frequency PWM and CBSVM. In this modulation technique, the four switches of each inverter module are operated at two different frequencies, two being commutated at the fundamental frequency, while the other two switches are pulse width modulated at CBSVM. Unfortunately, this arrangement causes different

switching losses and therefore differential heating among the switches. In order to overcome this problem, a sequential switching scheme is embedded in this hybrid modulation.

Base PWM Circulation

For long operating-time expectancy, it is important to share the power loss among every module, and furthermore, to every power device in the cell. This is one of the key issues the modulation should cover.

A simple base PWM circulation scheme introduced here to get resultant HPWM circulation among the power modules. The scheme of five-level base PWM circulation is shown in Fig. 4 (b) consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is fo/4, makes the time base for PWM circulation from one module to another. After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module, the second becomes the third, etc., while the last module HPWM shifts to the first. This PWM circulation is based on simple multiplexer logic circuits, which makes the applicability of the algorithm very effective in a CPLD.

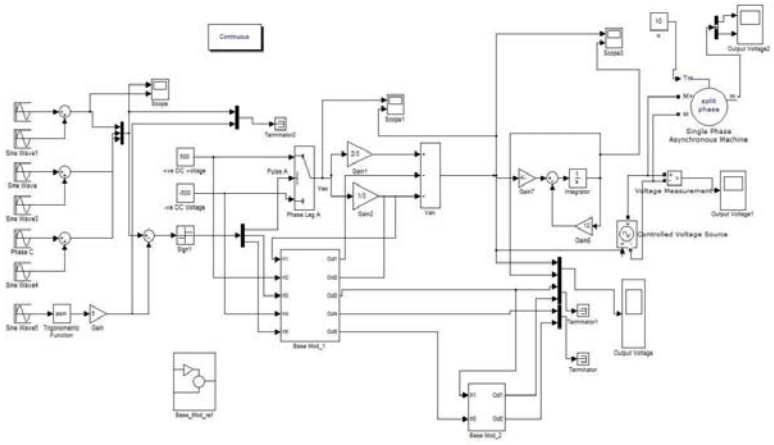
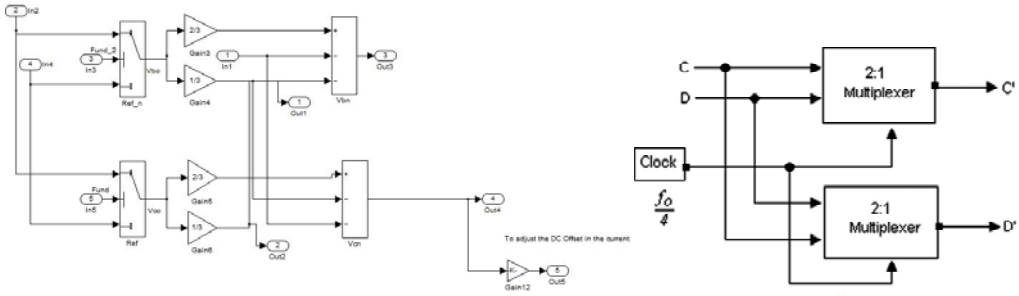


Figure 3: Simulation diagram of the proposed system.



(a) (b)

Figure 4: (a) Sub – circuit of base modulator circuit. (b) Scheme of base PWM circulation for five-level operation.

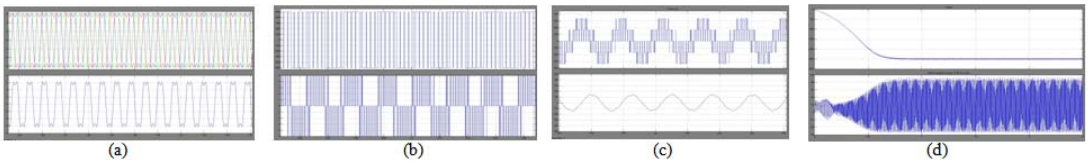


Figure 5: (a) Three phase PWM waveform. (b) Hybrid PWM Wave. (c) Carrier and sine wave (d) Electromagnetic torque and speed curves

PWM Strategies with Differing Phase Relationships

One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. There are three alternative PWM strategies with differing phase relationships:

- Alternate phase disposition (APOD) – every carrier waveform is in out of phase with it neighbour carrier by 180.
- Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero.
- Phase disposition (PD) - All carrier waveforms are in phase.

Alternate Phase Disposition (APOD)

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180 degree. Since APOD and POD schemes in case of three level inverter are the same, a five level inverter is considered to discuss about the APOD scheme.

The rules for APOD method, when the number of level N = 5, are

- The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180.
- The converter switches to + Vdc / 2 when the reference is greater than all the carrier waveforms.
- The converter switches to Vdc / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.
- The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.
- The converter switches to - Vdc / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.

The fig 7(a) displays the switching pattern generated by the comparison of the modulation signals with the four carrier waveforms. Fig 7(b) demonstrates the output voltage waveform of phase “a” for a five-level inverter in APOD scheme.

Phase Opposition Disposition (POD)

For phase opposition disposition (POD) modulation all carrier waveforms above zero

reference are in phase and are 1800 out of phase with those below zero. The rules for the phase opposition disposition method, when the number of level N = 3 are,

- The N –1 = 2 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 1800 out of phase with those below zero.
- The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.
- The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
- The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

The fig 8(a) illustrates the switching functions produced by POD carrier based PWM scheme. In the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the lower triangle from 0 to –1 and these two triangle waveforms are in out of phase. When the modulation signal is greater than both the carrier waveforms, S1ap and S2ap are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S2ap and S1an are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S1an and S2an are turned on and the converter switches to negative node voltage.

The Fig 8(b) shows the carrier's waveforms are displaced out of phase and compared with the sinusoidal modulation signal and the phase "a" output voltage waveform.

Phase Disposition (PD)

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Figure demonstrates the sine-triangle method for a three-level inverter. Therein, the a-phase modulation signal is compared with two (n-1 in general) triangle waveforms. The rules for the phase disposition method, when the number of level N = 3, are

- The N –1 = 2 carrier waveforms are arranged so that every carrier is in phase.
- The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.
- The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
- The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

The fig 9(a) illustrates the switching pattern produced by the carrier-based PWM scheme. In the PWM scheme there are two triangles, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. In the similar way for an N –level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/(N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/(N-1)), second carrier waveform from (1-4/(N-1)), and the bottom most triangle varies from (2-2/(N-1)) to –1.

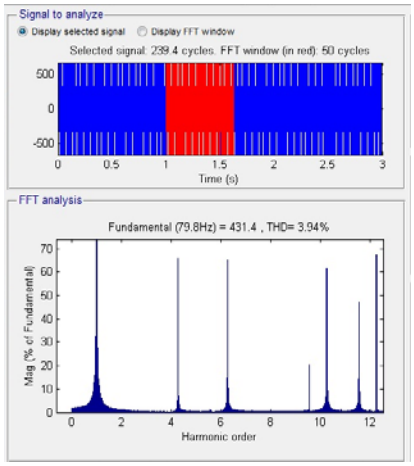


Figure 6: FFT Analysis.

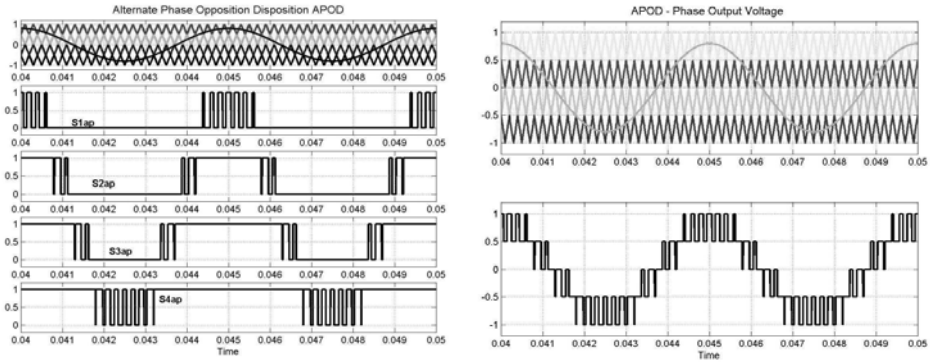


Fig.ure 7: (a) Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter. (b) Output voltage waveform of phase "a" for a five-level inverter in APOD scheme.

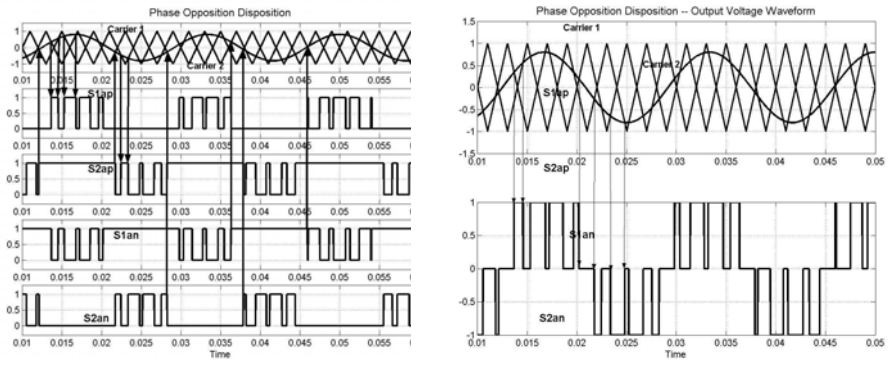


Figure 8: (a) Switching pattern produced using the POD carrier-based PWM scheme. (b) Simulation of carrier-based PWM scheme using POD. I. Modulation signal and out of phase carrier waveforms (II) Phase "a" output voltage.

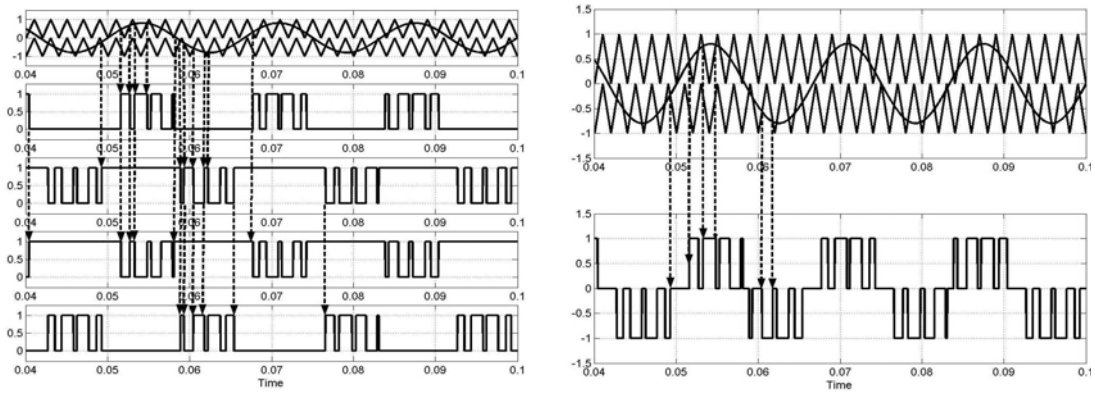


Figure 9: (a) Switching pattern produced using the PD carrier-based PWM scheme. (b) Simulation of carrier-based PWM scheme using the phase disposition (PD).

In Fig 9(b), the switching pattern of each device can be seen. It is clear from the figure that during the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S1ap and S2ap are turned on and also during the positive cycle S2ap is completely turned on. When S1ap and S2ap are turned on the converter switches to the + Vdc / 2 and when S1an and S2ap are on, the converter switches to zero and hence during the positive cycle S2ap is completely turned on and S1ap and S1an will be turning on and off and hence the converter switches from + Vdc / 2 to 0. During the negative half cycle of the modulation signal the converter switches from 0 to -Vdc / 2. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage.

Conclusion

This paper proposed a new family of SSHM techniques for CMLI, operating at a lower switching frequency is proposed. The proposed technique is applied to well-known MSPWM schemes; APOD, PSC, CBSVM, and SCSPWM. Compared to conventional MSPWM schemes, less number of commutations and considerable switching-loss reduction is obtained while achieving the same fundamental voltage tracking. The harmonic performance of the SSHM schemes are analyzed in the entire range of modulation index and it seems to be good. An efficient sequential switching and PWM circulation techniques are embedded with these hybrid modulations for balanced power dissipation among the power devices within a cell and for series connected cells. These modulations can be easily extended to higher voltage level through the generalization process and implementation possible with existing CMLI structures.

In future this proposed system can be extended further for higher voltage level through generalisation process with the existing CMLI structure. This system can be implemented in new techniques such as fuzzy logic control, and genetic algorithm

using other software's such as PSPICE or PSCAD, and their corresponding results can be compared and further this THD value can be reduced which will be a new development of the research work.

References

[1] O. Keiser, P. K. Steimer and J. W. Kolar, "High power resonant switched capacitor step-down converter, " in Proc.IEEEPESC2008, Jun., pp.2772–2777.

[2] M. Shoyama, T. Naka and T. Ninomiya, "Resonant switched capacitor converter with high efficiency, " in Proc.IEEEPESC2004, Jun., vol. 5, pp.899–903.

[3] K. Sanoand H. Fujita, "Voltage-balancing circuit based on a resonant switched-capacitor converter for multilevel inverters, " IEEE Trans. Ind. Appl., vol. 44, no.6, pp.1768–1776, Nov. /Dec. 2008.

[4] G. Narayanan, D. Zhao, H. K. Krishnamoorthy, R. Ayyanar and V. T. Ran ganathan, "Space vector based hybrid PWM techniques for reduced current ripple, " IEEE Trans. Ind. Electron., vol. 55, no. 4, pp. 1614–1628, Apr.2008.

[5] C. Govindaraju and K. Baskaran, "Efficient hybrid carrier based space vector modulation for cascaded multilevel inverter, " J. Power Electron., vol.10, no.3, pp.277–284, May2010.

[6] C. Govindaraju and K. Baskaran, "Performance analysis of cascaded multilevel inverter with hybrid phase-shifted carrier modulation, " Aust. J. Electr. Electron. Eng., vol. 7, no. 2, pp. 121–132, Jun. 2010.

[7] S. M. Dehnavi, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh, Space vectors modulation for nine-switch converters IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1488 1496, June 2010.