

Performance Analysis of a High Gain CMOS Instrumentation Amplifier for Biomedical Signal Processing

S. Kirthy

*Student of M. Tech, School of ICT, Gautam Buddha University,
Greater Noida, U.P*

Abstract

CMOS Instrumentation Amplifiers are excellent active current mode device with wide band capability valuable for low amplitude signal processing in biomedical signal acquisition. Gain, Bandwidth and CMRR (common mode rejection ratio) are the three most important parameters of an amplifier. Optimizing an amplifier for these parameters leads to contradicting demands. Due to the continuous demand for extracting low amplitude signals below 5mv like in ECG and EMG signals one requires most appropriate Instrumentation Amplifier that can amplify the signal to desired level with rejecting any voltage that is common to both the inputs.

Various architectures like Cascode circuits are widely used in circuit design at places where high gain and high output impedances are required. Different architectures like Single stage Operational Trans conductance Amplifier, Two stage OTA and Folded Cascode OTA architectures have been used to obtain high gains. Different architectures of Instrumentation Amplifier like single op-amp, two op-amp and three stage op-amp has also been implemented to obtain the best results in terms of gain and CMRR.

This work describes a novel technique of designing a low noise high gain CMOS instrumentation amplifier for biomedical applications. The circuit is simulated using Cadence Spectre tool and layout is designed in Cadence Layout editor at 0.18 μ m CMOS technology. A three op-amp instrumentation amplifier has been designed by employing two simple op-amps at the two inputs and a folded cascode op-amp at the output. Both input and output stage op-amps are 2-stage. By using folded cascode two stage op-amp at the output, we have achieved significant improvement in gain and CMRR. Transistors sizing plays a vital role in achieving high gain and CMRR. To achieve a desirable gain, common mode rejection ratio, lower power consumption and other performance metrics, selection of most appropriate op-amp circuit topologies & optimum transistor sizing are vital in the design.

