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Optimization of Area and Delay in Low-Power Memory Cell through Adiabatic Technique

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Abstract

The dissipation ofPower in conventional CMOS circuits can be minimized by adiabatic technique. In this paper, the area and delay of conventional CMOS logic and with adiabatic technique for memory block and all the building blocks required in the memory block are computed. Delay of the building blocks is calculated and compared at two different technologies along with the comparison of conventional and adiabatic delay. Area optimization and comparison was computed at different technology. From the simulations results, it could be concluded that the Delay is reduced as compared to conventional CMOS technique. The circuits have been simulated at transistor level using Cadence Virtuoso Tool at 180 nm and 90nm CMOS process technology at VDD=1.8V, 1.1V and T=27^0C.

Keywords: Adiabatic circuits, Low-Power, Conventional CMOS circuits, Power PC D Flip Flop, Memory cell.

1. Introduction

One of the biggest challenges of our times is to limit the power consumed in electronic devices which will lead to longer battery life while maintaining high performance. In today's world power reduction is one of the most important factors for any circuit. This paper provides a fair idea of low power solutions in the Very Large Scale Integration (VLSI) area. The requirement of low static power consumption in conventional CMOS circuits is promptly coming out as one of the major concern in the VLSI design system. The power dissipation is thoroughly reduced by using adiabatic logic structures. Adiabatic logic intends a method to reuse the stored energy of the load capacitors rather than wasting this energy by discharging through the load capacitor to the ground.

In adiabatic logic, V_{DD} is replaced with a periodic ramp signal or an AC power supply. In adiabatic charging the transitions are considered to be satisfactorily slow therefore at constant current all the nodes are charged or discharged. In this way power dissipation can be diminished by decreasing the peak current flowing completely from the transistors. [1, 2, 3]

2. Area and Delay Estimations

Adiabatic Technique also affects other system design parameters like energy, delay and area. Timing, determination gives an idea that how much adiabatic technique affects design or not and it in turn depends on whether the design of the circuit is done by using minimum MOSIS design rule or the layout is designed manually. Automatic layout generation using Cadence is dependent on the details of the width, length and the spacing of the metal and poly layers. In our case, the generation of the layout was done using the automatic technique. So, the adiabatic technique used here did not take into account any delay drawback, and hence with no performance loss power obtained could be saved.

For the system timing evaluation, we have taken maximum operating frequency of 150 MHz. The RC parameters allowed estimation of the interconnect delay itself. The sums of these two contributions were the delays for each address and selection signals, whose maximum value was compared to the delay budget to check for proper behavior at maximum frequency. Area was computed by taking the length and the breadth of the generated layout designs of all the building blocks and for the 4x3 memory cell structure.

3. A Review of Related Work

This section presents various power reduction topologies which come under adiabatic reduction technique outlined so far by numerous researchers and scholar's in the area of semiconductor CMOS design.

Chun-Keung Lo et.al [4] "Design of Low Power Differential Logic Using Adiabatic Switching Technique," implemented ADCPL NAND and Carry Look ahead Adder, XOR, AND-OR circuits at a frequency 10MHz – 50MHz on SPICE tool at 500nm CMOS technology, proposed Adiabatic Differential Cascode Voltage (ADCPL) Technique for energy loss reduction.

Low Power Multiplier Design Using Complementary Pass-Transistor Asynchronous Adiabatic Logic [5] implemented 4 bit, 8 bit, and 16 bit multipliers with Complementary Pass Transistor Asynchronous Adiabatic Logic (CPTAAL) circuits at 100MHz-300MHz on Tanner EDA tool with SPICE Support.

Alex G. Dickinson and John S. Denker [6] proposed CMOS Logic Family known as Adiabatic Dynamic Logic by implementing ADL Inverter and Static and Dynamic CMOS Inverter circuits at an operating frequency of 250MHz. These techniques and circuits can be applied for energy loss reduction.

Jianping Hu et.al [7] "A Single-Phase Adiabatic CAM Using Improved CAL Circuits", implemented CAL buffer, CAL NAND/AND, OR/NOR, 16X16 adiabatic CAM at 100MHz frequency using HSPICE at TSMC 180nm.

Edward K. Loo et.al [8] "Low-Voltage Single-Phase Clocked Quasi-Adiabatic Pass-Gate Logic" proposed Low-voltage Quasi-Adiabatic Pass-Gate Logic (QAPG) family using a single power clock by implemented Full Adder circuit using frequency up to 250MHz at HSPICE tool on 90nm technology.

Hamid Mahmoodi-Meimand et.al [9] "Efficiency of Adiabatic Logic for Low-Power, Low-Noise VLSI" implemented 8-bit carry look-ahead adder at 600nm technology. The switching noise characteristics is also improved with reduced floating node problem.

4. Design Simulations and Results

In this section delay is calculated at different technologies and also comparison of conventional and adiabatic technique in terms of delay is evaluated. Area comparison is also done on different technologies.

DELAY OPTIMIZATION-The delay of the building blocks is calculated and compared at two different technologies. All the calculation of delay is done at 180nm and 90nm technology.

Table 1: Shows the Delay calculation of different circuits at different technologies.

Circuits	Delay (180nm) in Sec.	Delay (90nm) in Sec.
Inverter	152.50E-9	4.31E-10
Clocked Inverter	40.46E-9	4.046E-08
2 Input And Gate	30.08E-9	30.08E-9
3 Input And Gate	30.10E-9	9.719E-09
4 Input Or Gate	69.93E-9	3.034E-08
Power Pc D Flip Flop	9.68E-9	7.064E-08
4x3 Memory Using D Flip Flop	12.34E-9	12.34E-9
4x3 Memory Using Power PC D Flip Flop	22.56E-9	22.56E-9

The graphical representation of the delay of different circuits is shown below

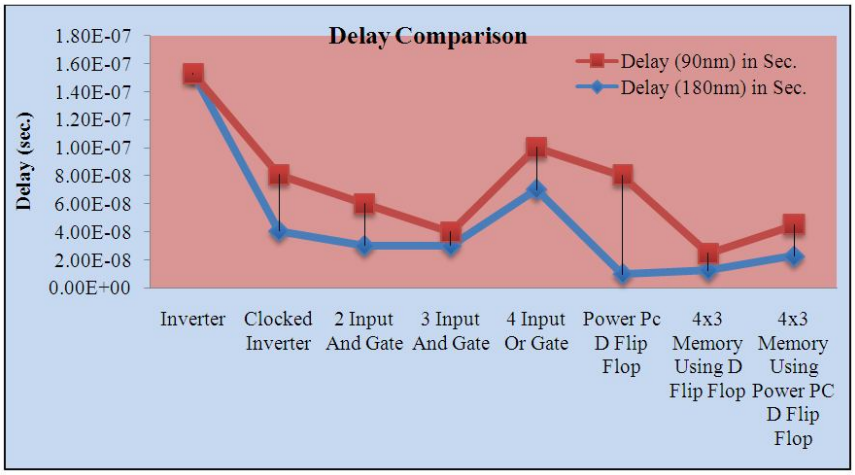

Fig. 1: Shows the Delay calculation of different circuits at different technologies

5. Conventional and Adiabatic Delay

The comparison between the conventional CMOS technique and adiabatic technique in terms of delay of all the building blocks is also calculated at 90nm technology. From the results we can conclude that the adiabatic delay is less as compared to the conventional CMOS power. The tabular and graphical representation of average power is shown below.

Table 1: Shows the conventional and adiabatic delay comparison of all the building blocks

Circuits(90nm)	Delay (Sec.)	Adiabatic Delay (Sec.)
Inverter	4.31E-10	4.128E-09
Clocked Inverter	4.046E-08	4.415E-08
2 Input And Gate	30.08E-9	1.65E-08
3 Input And Gate	9.719E-09	2.65E-08
4 Input Or Gate	3.034E-08	3.927E-08
Power Pc D Flip Flop	7.064E-08	5.859E-09
4x3 Memory Using D Flip Flop	12.34E-9	6.75E-09
4x3 Memory Using Power PC D Flip Flop	22.56E-9	7.98E-09

The graphical representation of the conventional and adiabatic delay comparison of all the building blocks is shown in the figure given below

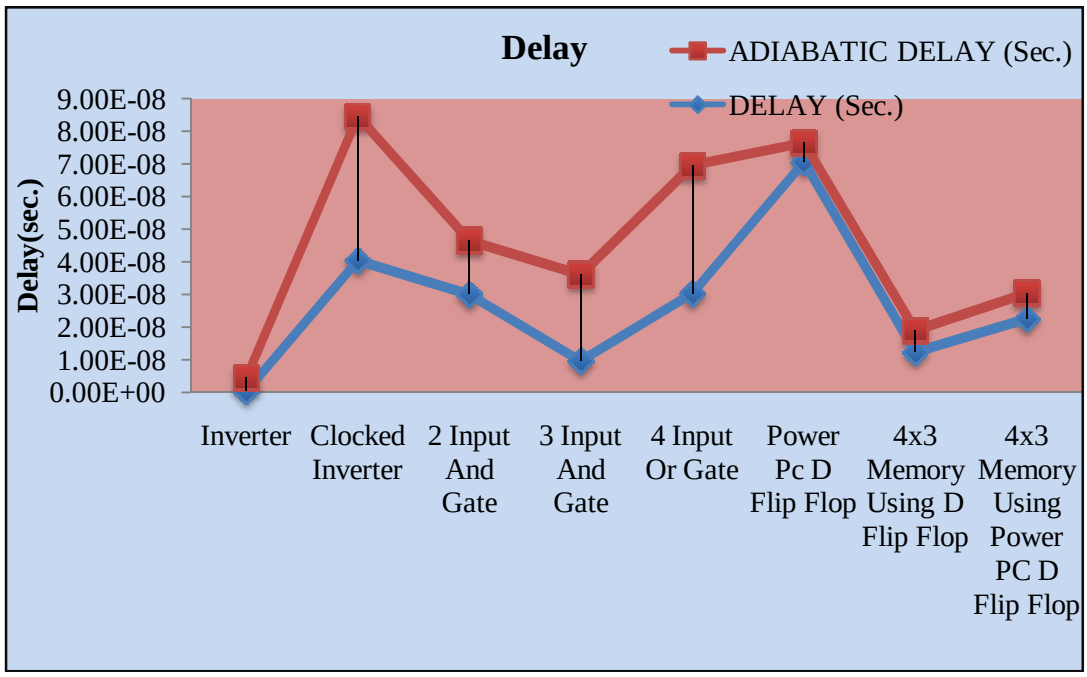

Fig. 2: Shows the conventional and adiabatic delay comparison of all the building blocks.

6. Area Comparison

After designing all the building blocks of the 4X3 memory cell and the 4X3 memory cell itself the post layout simulations are also been done after making the layout design of the circuits at 180nm and 90nm technology and the area consumption is compared for both the technologies Table given below shows the comparison of area at different technologies.

Table 2: Shows the area comparison of different circuits.

Circuits	Area at 180nm (Sq. µm)	Area at 90nm (Sq. µm)
Inverter	73.24	5.36
Clocked Inverter	90.53	20.04
2 Input AND Gate	83.72	28.43
3 Input AND Gate	96.18	38.73
4 Input OR Gate	168.18	72.76
Power PC D Flip Flop	1798.33	185.99
4x3 Memory Block	195044.11	47631.78

7. Conclusion

We have presented an integrated memory area and delay optimization methodology for power reduction by using adiabatic technique. The fundamental feature of the presented approach was the use of memory design phase information related to schematic, in the form of pre-characterized power expenses used to speed up the search for the power reduction. The precise representation of the power overheads translated high-level optimization margins into real power savings; therefore, the adiabatic technique could be used as a high-level power reduction technique for the memory optimization and also for the other CMOS structures.

Results shows that the adiabatic technique was valuable in applications where power reduction would be of prime importance as in high performance battery-operated portable digital systems for example mobile phones, note-book computers and digital aides.

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Biographies

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