

A 2.4-GHz Differential Low-noise Amplifiers using 0.18 μ m CMOS Technology

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Abstract

A 2.4-GHz inductive degenerate differential narrowband low-noise amplifiers (LNAs) using 0.18 μ m CMOS Technology are presented in this paper. The LNA is properly biased operates at 1.8 volts power supply and perfectly matched input impedance of 50 ohms. The LNA has the Noise figure <2.5dB, Gain(S21) >20dB, Input impedance (S11) <-20dB, Output impedance (S22) <-10dB, IIP3>-10dBm.

Keywords: Low noise amplifier (LNA), impedance matching.

1. Introduction

The wireless communication industry is currently experiencing tremendous growth. In responding to the demand for a low-cost but high performance wireless front-end, many intensive researches on CMOS radio-frequency (RF) front-end circuits have been carried out[3]. The ultimate goal is to minimize the trade-off between high performance and low-cost, low power consumption design.

Low noise amplifier (LNA) is typically the first stage of a receiver. Its performance greatly affects the overall receiver performance. The narrow band LNA uses an inductively degenerated input stage and an LC load. The inductive degeneration is used to enhance the transit time effects. The LNA should have good NF to avoid degrading the overall receiver NF [3]. The LNA is designed in such a way that it should match the impedance of the antenna that's why we kept input impedance of LNA 50 ohms. We required balloon to interface source degenerate LNA so to avoid this differential LNA is used. Another advantage of differential LNA is that it eliminate even harmonics from the output so its noise performance is better than single source degenerate LNA.

2. LNA Design

The signal received at the antenna of the receiver is comparatively weak so good gain and noise performances are necessary requirements for LNA. Its main function is to

provide enough gain to overcome the noise of the subsequent stages. LNA design involves the tradeoff between noise figure (NF), gain, linearity and power consumption. The LNA design optimization technique is used to make tradeoff between gain and linearity. The source degenerated LNA is shown in the fig.1. L_d with the node capacitance at the drain of M_2 will resonate at the operating frequency and provide additional band pass filtering and the very small voltage drop across L_d because it is connected in series so it is also a low power design. M_3 is for biasing the LNA circuit as it is in the current mirror connection with M_1 , and their ratio will determine the current flowing through the cascade branch. Proper selection of M_1 's width will determine the voltage across G-S of M_1 . R isolates the signal path from the current mirror. The value of R is not critical as long as it is much greater than the output impedance of the preceding stage [1]. M_1 provides the cascode amplifier with an infinite input resistance. Another important advantage is that the cascode is able to reduce the effect of M_1 's gate-to drain capacitance, i.e. the Miller effect. This is because the input resistance of M_2 is usually much smaller than output resistance of M_1 [4].

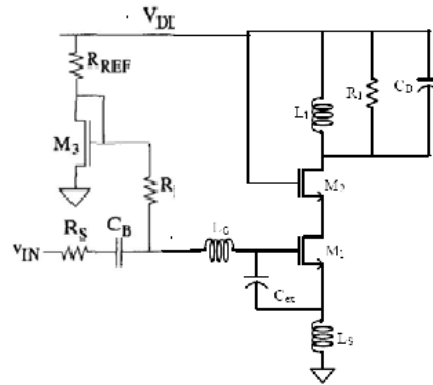


Fig. 1

To obtain the width of M_1 we use power constrain noise optimization technique [1].

$$W_{opt} = \frac{3}{2\omega L C_{ox} R_S Q_{in}} \quad (1)$$

$$W_{opt} \approx \frac{1}{3\omega L C_{ox} R_S} \quad (2)$$

Where W_{opt} is used for the width of M_1 . L is the effective channel length of the M_1 transistor, C_{ox} is the oxide capacitance and Q_{in} is the input circuit quality factor.

C_{ex} is also introduced in the circuit to give more freedom to match input impedance and reduce the value of inductor. To fabricate inductor it occupies more space in the chip.

The width of M_2 is kept equal to M_1 so that they can share drain area. The cascode transistor M_2 also provide isolation between output and input.

The noise figure obtained with W_{opt} is

$$- - - - - \quad (3)$$

The parameter L_g and L_s are used for input impedance matching. The small signal equivalent model for calculation of input impedance is shown in fig.2[4].

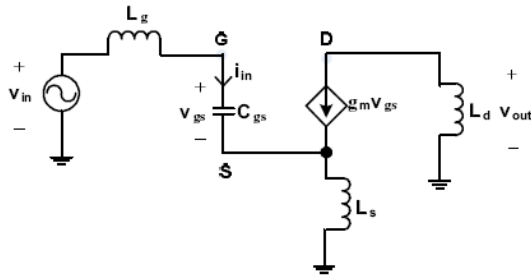


Fig. 2

From the fig.2 we can calculate the input impedance of the circuit and it is given by:

$$- - - - - \quad (4)$$

At resonance

$$- - - - - \quad (5)$$

The width of the mos M_3 is calculated according to the bias current flowing from the LNA.

From single ended source degenerate LNA we can design a differential LNA. The schematic of differential LNA is shown in fig.3.

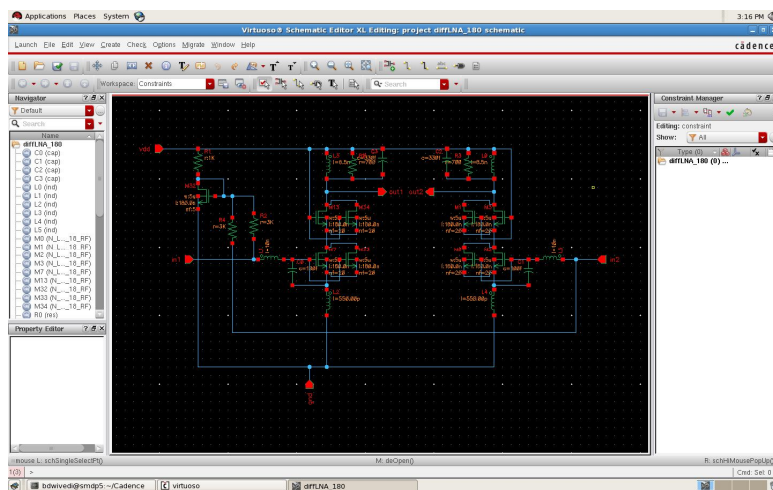


Fig. 3

3. Simulation Results

In the design of differential LNA, the simulation was carried out using Spectre RF from Cadence design suite. The LNA working at 2.44GHz. This design was using UMC 180nm process technology. Fig. 4-7 shows S-parameters result of differential CMOS LNA. The LNA achieved to obtain a voltage gain(S21) of 24.92dB and fig.8 shows the noise figure, NF 0.5 dB. The input return loss, S11 is - 23.64 dB and output return loss is -4.46 dB. The attained value of NF is believed to be good as it exceeds the requirement which is typically below 2 dB without having to trade off the power gain which also satisfies the requirement. The obtained IIP3 is -8.83dBm shown in fig.9.

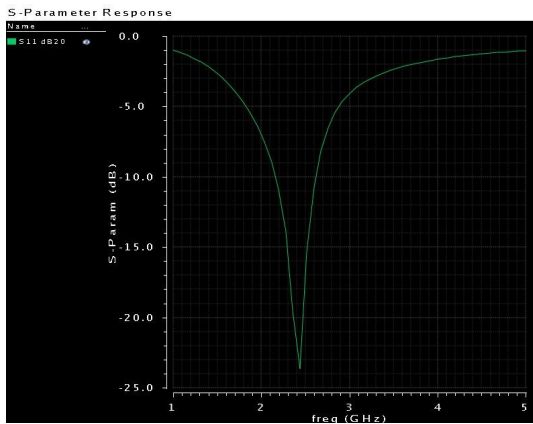


Fig. 4

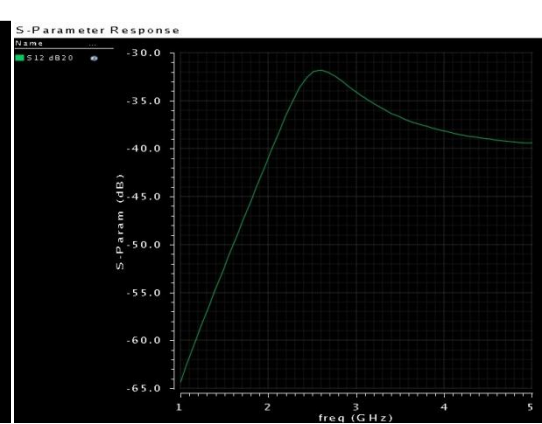


Fig. 5

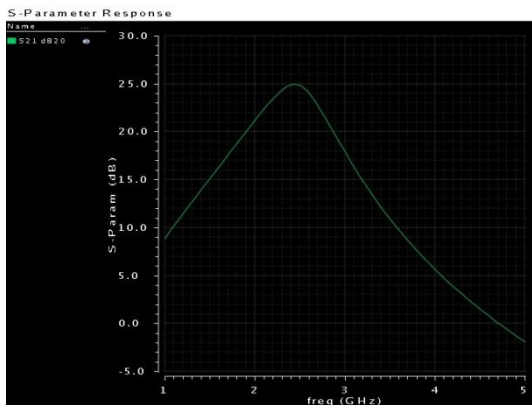


Fig. 6

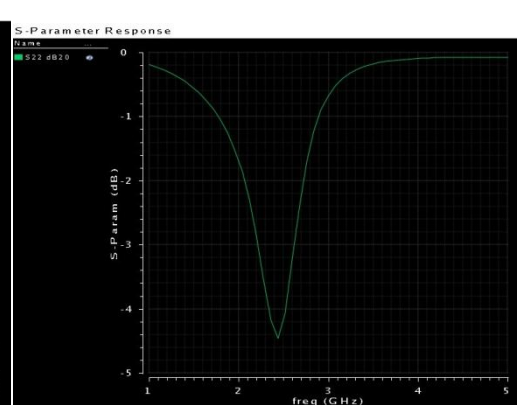


Fig. 7

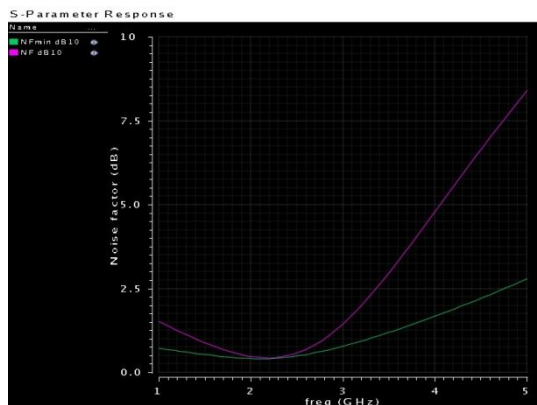


Fig. 8

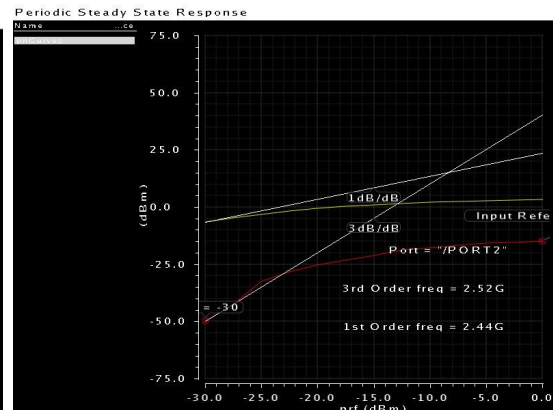


Fig. 9

4. Conclusion

A differential LNA is designed in the Cadence tool using 0.18um technology. The LNA is working at the frequency of 2.44GHz. The Lmin is taken 180nm and maximum width of the transistor is 200um. We obtained the high gain ($\approx 25dB$) Low noise ($\approx 0.5dB$) amplifier having very good noise performance. The LNA operating at 1.8 V power supply.

References

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