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Co-design Approach of RMSA with CMOS LNA for Millimeter Wave Applications

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Abstract

For millimeter wireless communication, integration of small electrically antennas with amplifiers is remains to be challenge. In this paper, design and analysis of Low noise amplifier integrated with rectangular micro-strip antenna is proposed. This novel technique may improve the system integration, reducing chip area, suppressing the noise and saving the effective cost. Three different architectures are designing using CMOS 90nm TSMC design kit and simulated in ADS v.11 platform. In first, 90nm CMOS LNA improves performance parameters at 40 GHz resonant frequency and achieves return loss of -22dB, noise figure of 4.7dB with forward gain of 26dB. In second, a design of rectangular patch antenna with micro-strip feed at 40 GHz which achieves good receiving charactertics with 5dB gain. In third, co-design of patch antenna with CMOS LNA at 40 GHz succeeds higher gain of 27dB with lower noise figure of 3.4dB. A Co-design of LNA and rectangular micro-strip antenna at 40 GHz is to relax the 50Ω impedance matching constraints.

Keywords: Co-design; Rectangular patch antenna; millimeter wave (MMW); CMOS LNA

1. Introduction

Now days, fastest growth of wireless communication industries is establishing a big new market opportunity. Current researchers are founding for new solutions which would be implemented into the existing wireless system networks to provide the broader bandwidth, the high quality and new added services. A millimeter wave (MMW) frequency band is the most promising technology for providing broadband wireless communications [1]. The extensive progress of CMOS technology has

enabled its application in microwave and millimeter wave technologies. Presently, the CMOS technology has became one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [2]. In spite of the advantages of CMOS technology, the design of CMOS transceiver in millimeter wave applications exhibits several challenges and difficulties that the designers must overcome. In addition, Kinetic performances of active devices with patch antenna have been improved, where MMW designs can be considered [3]. In RF receiver, the input signal from antenna first passes through the band pass filter to the LNA that amplifies it's and suppresses noise contributions from preceding stages. Hence, low noise figure and good impedance matching are essential LNA performance parameters while high gain are required by receiver system for achieve the system reliability[4-5]. The basic geometry of complete receiver system are shown in Fig.1

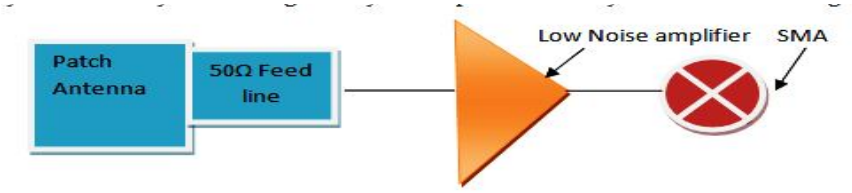

Fig. 1: Basic geometry of Co-design of LNA with patch antenna.

2. CMOS LNA Analysis

As the fulfill requirements of LNA design, we can use the different topology like common source (CS), Common Gate (CG) etc. which are briefly discuss below.

2.1 CG-CS Topology

The common source (CS) and common gate (CG) LNA typologies are one popular architecture choices which are widely used for LNA design. The CS with the source inductor degeneration technique achieves the input impedance matching with the ideal noiseless components and gives to a minimal noise figure and also provides a higher gain whereas common gate has offers wideband operating performance with good linearity and input-output isolation property [6].

2.2 Circuit Design

A 40 GHz two stage of CMOS LNA is designed using 90nm commercial TSMC design kit in Agilent advanced design system. Fig.2 shows the circuit schematic of the CMOS LNA at 40GHz. Before proceed to LNA design, firstly we have analyzed the one stage of CGLNA with low Q factor and achieves the good reverse isolation (S_{11}) is -22dB and 50Ω input impedance with the help of equation given below and its simulation result are shown in Fig.3 but sacrifice its noise figure and gain parameters.

$$Zin = \frac{1}{g_m + jwC_{gs}} \tag{1}$$

$$S_{11} = 20.\log_{10}\left(\left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|\right) \tag{2}$$

For achieving the losses parameters (like noise figure, gain etc), we are using the next stage i.e. CS with source degeneration and achieved best gain of 26dB and minimum noise figure of 3.8dB which are shown in Fig.4 and Fig.5 as per specification of our design. The cascade topology is used to reduce the miller effect, improve the stability and provides the higher power gain. The input-output match is accomplished with an LC impedance transformation network. The 208-fF output capacitor was implemented with one 218-fF capacitors in series to desensitize the process variation [7]. In this simulation, we have chosen design specifications and technologies under low supply voltage of 1V are shown in Table1.

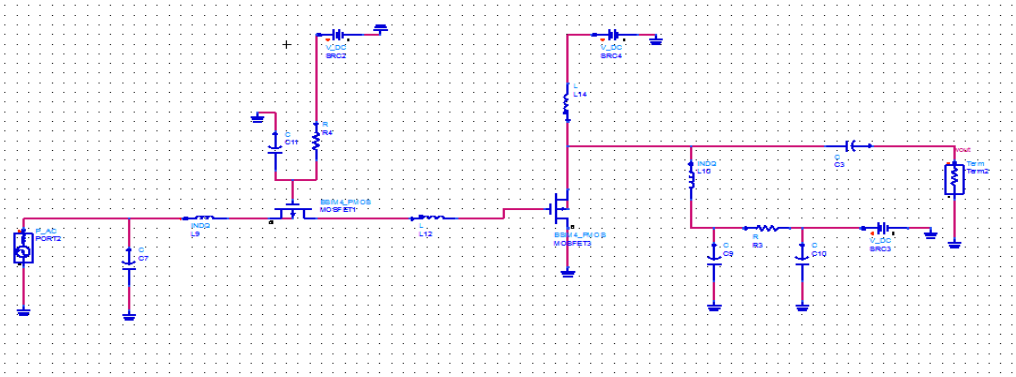

Fig. 2: Schematic of proposed CG-CS LNA at 40 GHz.

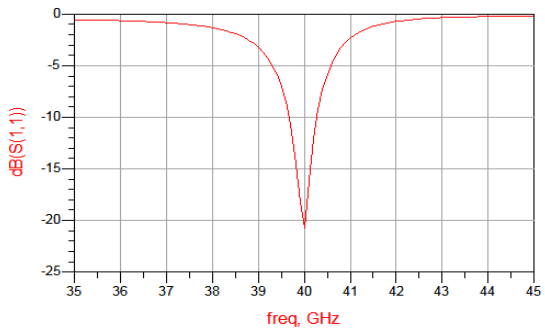

Fig. 3: Return loss Vs Frequency.

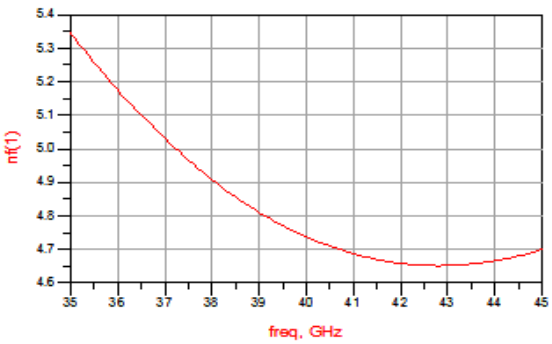

Fig. 4: Noise figure response with Frequency.

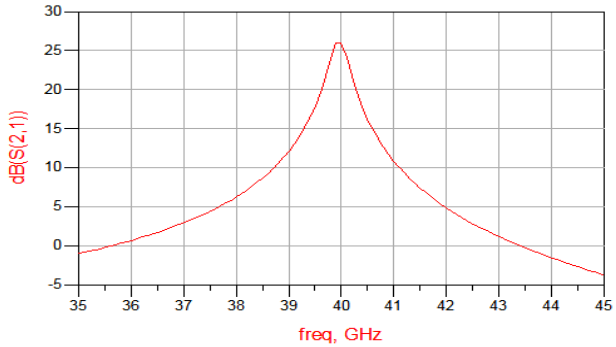

Fig. 5: Forward gain Vs Frequency.

Table 1: Shows specifications and technology of MOS transistors.

	Device Width (µm)	**Length (µm)**	**Biasing (V)**
M1	136	.09	0.6
M2	340	.09	1

3. Design Consideration of the Antenna

In this paper, we have design a rectangular patch antenna at 40GHz with new type of feeding and simulated in ADS tool. All the design work taken a RT durroid substrate with thickness of t = 0.245 mm at the height h = 10mil above a lossless ground conducting layer. The dielectric between metal layers is assumed to have ϵ_r = 2.36 and tanδ = .002. At 40GHz, a 50Ω feedline given these parameters would have a width and length is 2mm and 0.7mm respectively and the final dimensions of the patch are a length L = 2.2mm and a width W = 2.4mm respectively. The 3D view of patch antenna structure is shown in Fig. 6 and Fig.7 respectively.

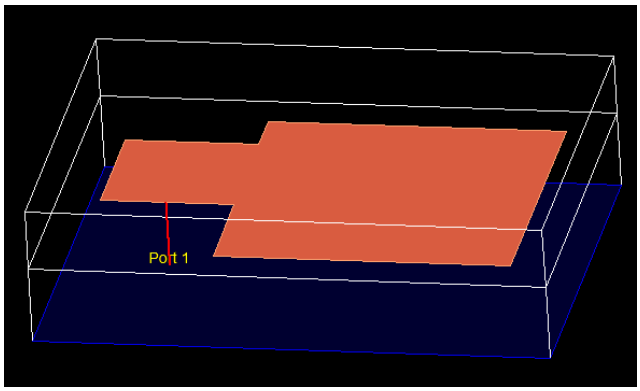

Fig. 6: Geometry of proposed patch antenna at 40 GHz.

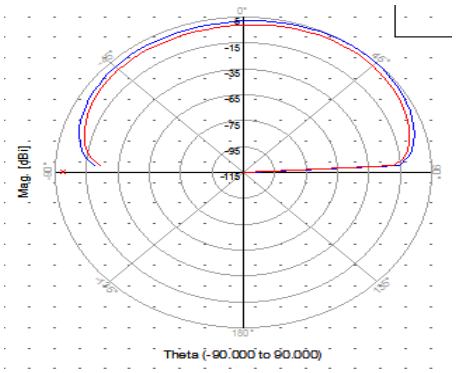

Fig. 7: Gain of patch antenna at 40 GHz.

4. Proposed Structure of the Communication Link

According to previously discussed the analysis of LNA and patch antenna, we are combined the co-design as the single structure on single substrate and check the performance of complete design with the support of simulation tool in ADS2012. It is well known that if we design a receiver system needs a high gain for passes the signal from antenna to the RF connector of end port of LNA. So it reveals from the simulation results of complete design, we have achieved higher gain of 27dB with noise figure of 3.4dB by proper impedance matching of 50Ω. The complete schematic design for receiver system at 40GHz is shown in Fig.8. All simulation results of receiver system are also given below in Fig.9 and Fig.10 respectively.

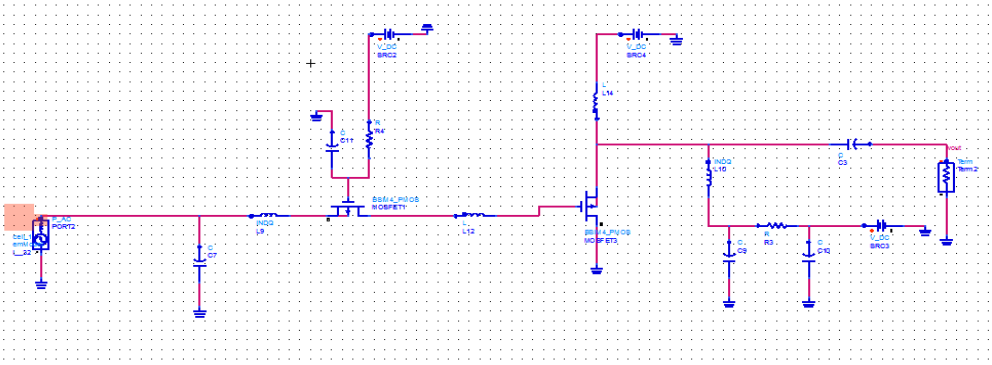

Fig. 8: Schematic of complete design at 40 GHz.

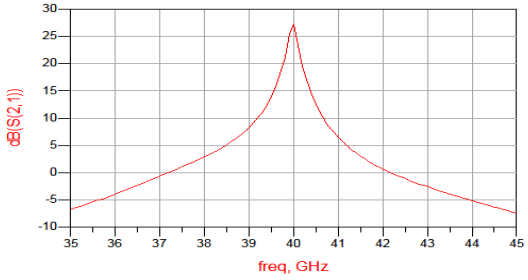

Fig. 9: Return loss Vs Frequency.

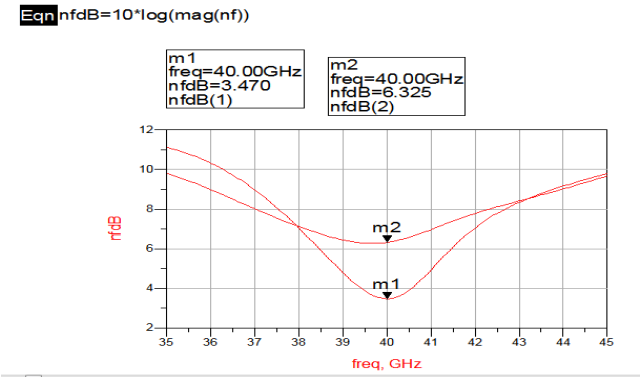

Fig. 10: Noise figure Vs Frequency.

5. Conclusion

The complete receiver system is designed for MMW applications in this paper, based on CMOS technology. Performance standards are met for this new co-design technique. The proposed method of receiver system in MMW applications, increases the level of system integration, reduces chip area and increases the overall system gain.

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