Comparative Study of THD in 5-level Neutral Point Clamped Multilevel Converter Using Multicarrier PWM and SHEPWM Techniques

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Abstract

A multilevel inverter is a power electronic device made to synthesize a desired AC voltage from several levels of DC voltages. Some industrial drives require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. A multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. In this paper career based phase disposition PDPWM, PODPWM, APODPWM and SHEPWM have been analyzed. The PWM control strategy method is used for multilevel inverter to reduce the THD in the output waveform. The simulation is done by Matlab/Simulink environment.

Keywords: multi-level converters, NPC, CHB, FLC, PWM, Power Quality;

1. Introduction

Multilevel converters present great advantages compared with typical and very well-known two-level converters [1][2]. These advantages improvements in the output signals quality and a nominal power increase in the converter. Researchers are trying to improve the THD of multilevel converter, the balancing of the DC capacitors voltage, the ripple of the load currents etc. Multilevel converters have many advantages over the conventional two level converters, for e.g. they produce lower harmonic distortion, have lower *dv/dt* stress, produce lower electromagnetic interference (EMI) and have higher efficiency when compared with the conventional converters.

2. The Multi Level Converter

Multilevel converters are power-conversion systems composed by an array of power semiconductors and capacitive voltage sources that, when properly connected and controlled, can generate a multiple-step voltage waveform with variable and controllable frequency, phase, and amplitude. The stepped waveform is synthesized by selecting different voltage levels.

The numbers of levels of a converter is defined as the number of steps that can be generated by the converter between the output terminal and any reference node within the converter, is usually denoted by N and called neutral. To be called a multilevel converter, each phase of the converter has to generate at least three different voltage levels. This differentiates the classic two-level voltage source converter (2L-VSC) from the multilevel family.

Multilevel converters can generate a variable frequency and amplitude voltage waveform. This is done with pulse-width modulation (PWM) techniques. On the other side, multilevel converters add a new degree of freedom, allowing the use of the voltage levels as an additional control element and giving more alternatives to generate the output waveform. Multilevel inverters have intrinsically improved power quality, characterized by: lower voltage distortion (more sinusoidal waveforms), reduced dv/dt, and lower common-mode voltages, which reduce or even eliminate the need of output filters.

3. Converter Topologies

The most known and established topologies are Cascaded H-Bridge (CHB), Neutral point clamped (NPC) or diode clamped, Flying capacitor (FLC) or Capacitor clamped.

4. Neutral Point Clamped Multilevel Inverter

The neutral clamped inverter, also known as diode clamped inverter. The basic architecture of this inverter discussed in references [7], [9]. The neutral clamped inverter obtained the staircase output voltage. If m is the number of level, then the number of capacitors required on the DC bus are (m-1), the number of power electronic switches per phase are 2(m-1) and the number of diodes per phase are 2(m-2). The DC bus voltage has three levels using two capacitors C1 and C2, for five levels using four capacitors C1, C2, C3 and C4 as shown in Fig.1and.

Table 1: Five Level Switching State.

Terminal Voltage Switching state								
	SA1	SA2	SA3	SA4	SA5	SA6	SA7	SA8
2VDC	ON	ON	ON	ON	OFF	OFF	OFF	OFF
-VDC	OFF	ON	ON	ON	ON	OFF	OFF	OFF
0	OFF	OFF	ON	ON	ON	ON	OFF	OFF
-VDC	OFF	OFF	OFF	ON	ON	ON	ON	OFF
-2VDC	OFF	OFF	OFF	OFF	ON	ON	ON	ON

The voltage across each capacitor is Vdc/4 .each switch is limited to one capacitor voltage through clamping diodes. If we increase the number of levels that will decrease harmonic distortion and efficiency of the inverter increases because of the reduced switching losses.
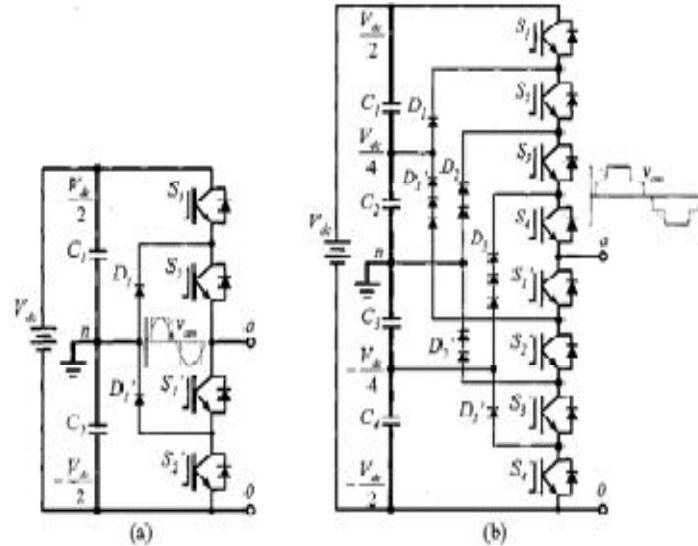

Fig. 1: Diode-Clamped Multilevel Inverter Circuit Topologies.
(a) Three-Level.(b) Five-Level.

5. Multilevel Converter Modulation Techniques

A detail explanation of the most common modulation method for multilevel inverters.

PWM Algorithms for Multilevel Converters:

Phase Shifted (PS-PWM): Phase-shifted PWM (PS-PWM) is a natural extension of traditional PWM techniques, specially conceived for FC [3] and CHB [4] converters.. Each cell can be modulated using the same reference signal. A phase shift is introduced between the carrier signals of contiguous cells, and producing a phase-shifted switching pattern between them.

Level Shifted (LS-PWM): Level shifted PWM (LS-PWM) is the bipolar PWM for multilevel inverters. Bipolar PWM uses carrier signal that is compared to the reference and the positive and negative bus bars of a VSI. a multilevel inverter, m-1 carriers are needed. They are arranged in vertical shift instead of the phase-shift used in PS-PWM.

6. Selective Harmonic Elimination-PWM

Selective Harmonic Elimination (SHE) is non carrier based PWM technique. In this method the basic square-wave output is "chopped" a number of times, which are obtained by proper off-line calculations.

A generalized quarter-wave symmetric stepped voltage waveform synthesized by a (2m+1) -level inverter, where m is the number of switching angles. By applying Fourier series analysis,

the amplitude of any odd n^{th} harmonic of the stepped waveform can be expressed as (4), whereas the amplitudes of all even harmonics are zero.

Where V_k is the Kth level of dc voltage, n is an odd harmonic order, m is the number of switching angles, and a_k is the th switching angle. According to Fig.5 a_1 to a_m must satisfy,

$$a_1 < a_2 < a_3 < .... < a_{m-1} < a_m < \pi/2$$
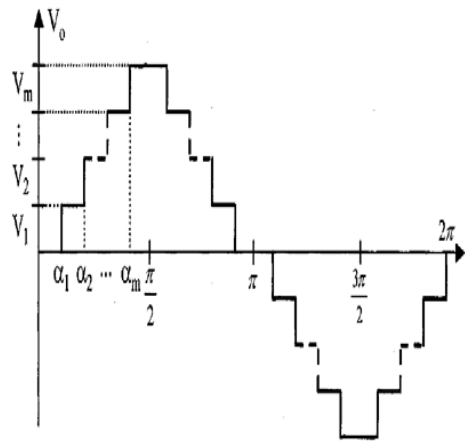

Fig. 2: Generalized Stepped-Voltage Waveform
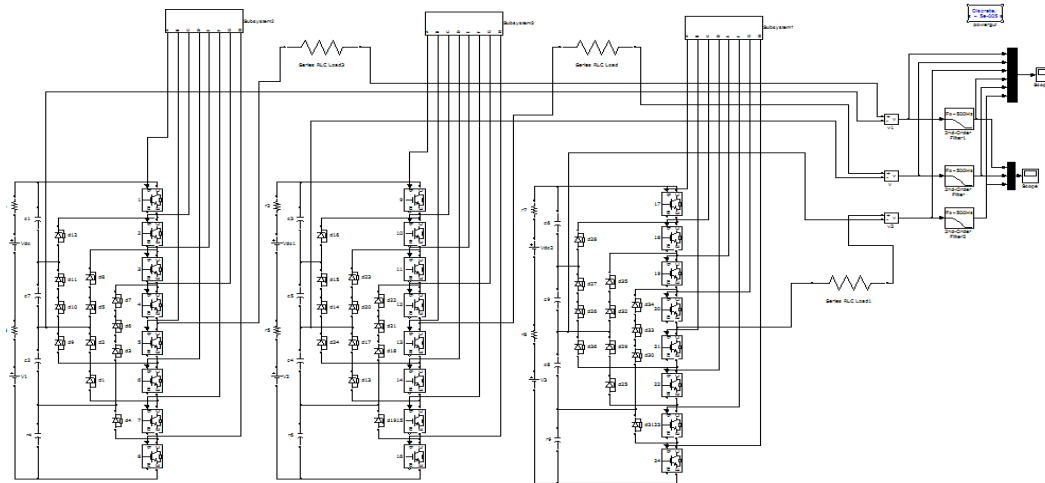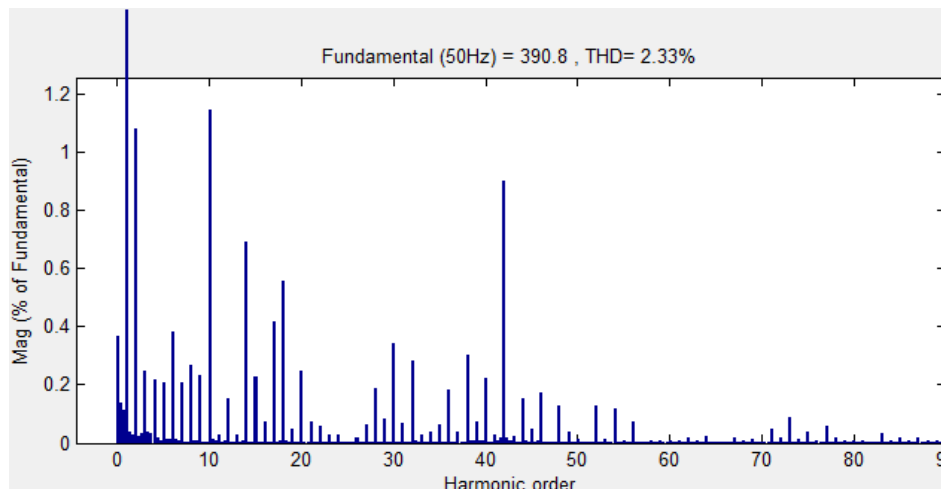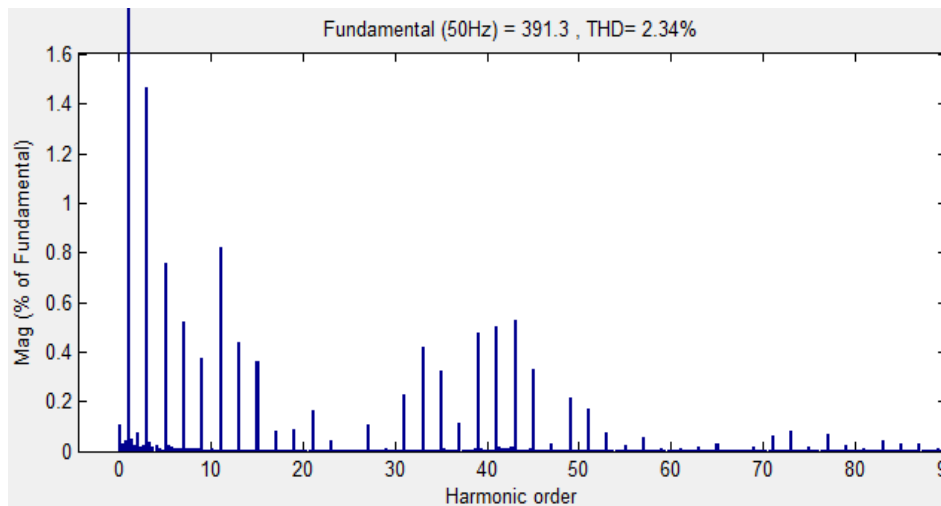
7. Simulation Result

Fig-4 5-LEVEL NPC SIMULATED MODAL

Fig. 5: %THD of POD with R-load

Fig. 4: % THD of PD with R-load.

Comparative Analysis of Simulated Result of 5-Level Neutral Point Claconverter Using Ls-PWM And SHEPWM Techniques

Table2: %THD for Different PWM

LOAD	SPWM			
	PD	**POD**	**APOD**	**SHEPWM**
R	2.33%	2.35%	1.94%	0.32%
RL	2.34%	2.36%	1.96%	0.39%
RLC	2.36%	2.38%	1.97%	0.44%
MOTOR	7.82%	7.80%	7.69%	6.80%

The 5- Level Neutral Point Clamped converter is simulated in rnatlab / sirnulink environment. The various method of the carrier based disposition analysis and gets the output waveform in the 5-level Neutral Point Clamped Inverter.

8. Conclusion

This paper has been addressed a survey of several technical literature concerned with Multilevel Inverter Topologies and their Modulation Technique. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references as well as the previous work done in the field of multilevel inverter topologies and their modulation technique.

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