

## **Programmable Frequency Divider Design for Multi – Ghz Phase Locked Loop (PLL) System**

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### **Abstract**

The objective of this project is to develop a Programmable Frequency divider design for multi GHz PLL System implementation on FPGA using VHDL (hardware description language). The frequency divider architecture features 6 parallel divider chains, each one of them implementing a single division ratio. The desired frequency division ratio is then selected using the four control bits of an output 16 to 1 multiplexer. To the extent of maximizing the frequency of operation, each frequency divider block has been realized using dynamic precharge-evaluation logic. The design of an improved dynamic logic DFF is presented. FPGA implementation of Frequency divider has been proposed in this project. This project involves two phases-simulation and synthesis of the VHDL codes using Modelsim SE 6. 1a and Xilinx Synthesis Technology (XST) of Xilinx ISE design suite 10. 1 tool. A VHDL specification can be executed in order to achieve high level satisfaction in its correctness before commencing design. Model sim is verification and simulation tool for VHDL, Verilog, System Verilog and it also supports mixed-signal language. It can simulate behavioral, RTL, and gate-level code separately or simultaneously. Model Sim also supports all ASIC and FPGA libraries, ensuring accurate timing simulations. Model Sim is known for delivering high performance, ease of use, and outstanding product support. The module for the Programmable frequency divider comprises basic digital components, such as frequency divide by 2, 3, 5, 7, 8, 13 and multiplexer.

**Keywords-**Phase locked loop (PLL), Voltage controlled oscillator (vco), frequency synthesizer, FPGA, VHDL.

### **1. Introduction**

On one side, the improvement of the microelectronics processes, especially for

complementary metal oxide semiconductor (CMOS) technology, allowed a drastic reduction of the power consumption, and an increase of the maximum operating frequency at which active devices can operate. This two combined factors allowed the integration on a single silicon die of both digital signal processing at base-band, and radio frequency signal conditioning, filtering and amplification at frequencies up to several gigahertz. The possibility of integrating all the functionalities of a full wireless transceiver on a single chip, allowed a consistent cost scaling and a reduction of the silicon die area compared to compound semiconductors technologies. Nonetheless, the newest wireless applications (like high-quality video streaming) are extremely demanding in terms of bandwidth. To face this problem, the allocation of new frequency bands has been necessary, and the frequency spectrum in the multi gigahertz range has been allocated. Inside this category of new frequency bands, the 7 GHz wide spectrum around 60 GHz (IEEE 802. 15 WPAN standard) is one of the newest and more promising. The recent scaling of CMOS processes down to 90-65-45 nm, allowed the operation of standard Si-CMOS processes at frequencies above 60 GHz In the overall transceiver system architecture, the frequency synthesis from a fixed reference frequency is an essential building block. Because of its better noise performances compared to other solutions and channel selection availability through the loop division ratio modulation, the phase lock loop (PLL) frequency synthesis is the natural choice for such an application. Specifically, the design of a programmable frequency divider chain for a PLL frequency synthesizer is taken into consideration. The purpose of the presented programmable divider is to enable frequency-channel selection capability in a PLL frequency synthesizer system [4].

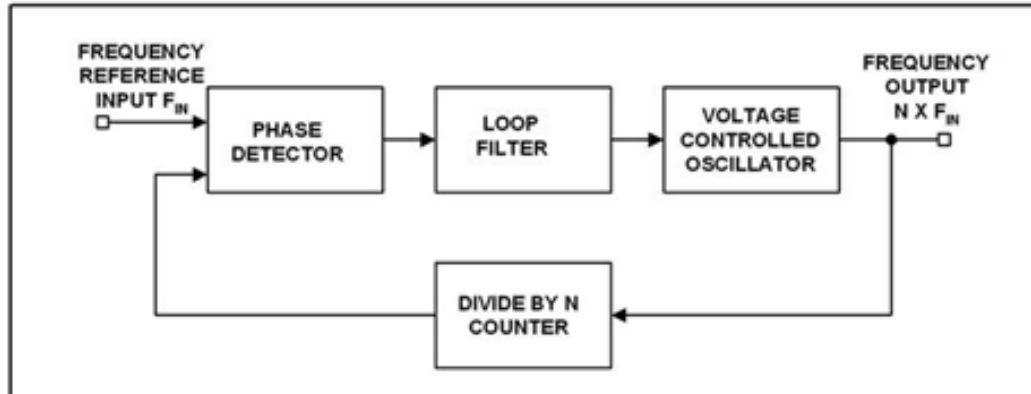
## **2. Phase-locked loop (PLL)**

A phase-locked loop (PLL) is a feedback control system that generates a signal that has a fixed relation to the phase of a reference signal. It responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase [1].

## **3. PLL Components and Basic Operation**

A PLL consists of five main blocks:

- Phase Detector or Phase Frequency Detector (PD or PFD)
- Charge Pump (CP)
- Low Pass Filter (LPF)
- Voltage Controlled Oscillator (VCO)
- Divide by N Counter



**Fig. 1** Block diagram of PLL

**3. 1 Phase frequency detector:**

The difference in phase between the reference and feedback signal is measured by the phase frequency detector, PFD. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/ low pass filter. If the error signal is an up signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage  $V_{ctrl}$ . And when the error signal from the PFD is a down signal, the charge pump removes charge from the LPF capacitor, which decreases  $V_{ctrl}$ . The control voltage  $V_{ctrl}$  is the input to the VCO[4], [3].

**3. 2 Charge pump:**

A charge pump is a three position electronic switch which is controlled by the three states of Phase-frequency detector. When the switch is in the UP or DOWN position, it delivers a pump voltage to the loop filter. When both UP and DOWN of Phase-frequency detector are off, that is, N position, the switch is open, thus the loop filter is isolated from the charge pump and phase-frequency detector[2].

**3. 3 Loop filter:**

The loop filter is the heart of PLL. The PFD/CP/LPF combination contains a pole at the origin and VCO also contains a pole at the origin. As the loop gain has two poles at the origin the instability arises. In order to stabilize the system, we must modify the phase characteristics by adding a resistor in series with the capacitor [2].

**3. 4 Voltage controlled oscillator:**

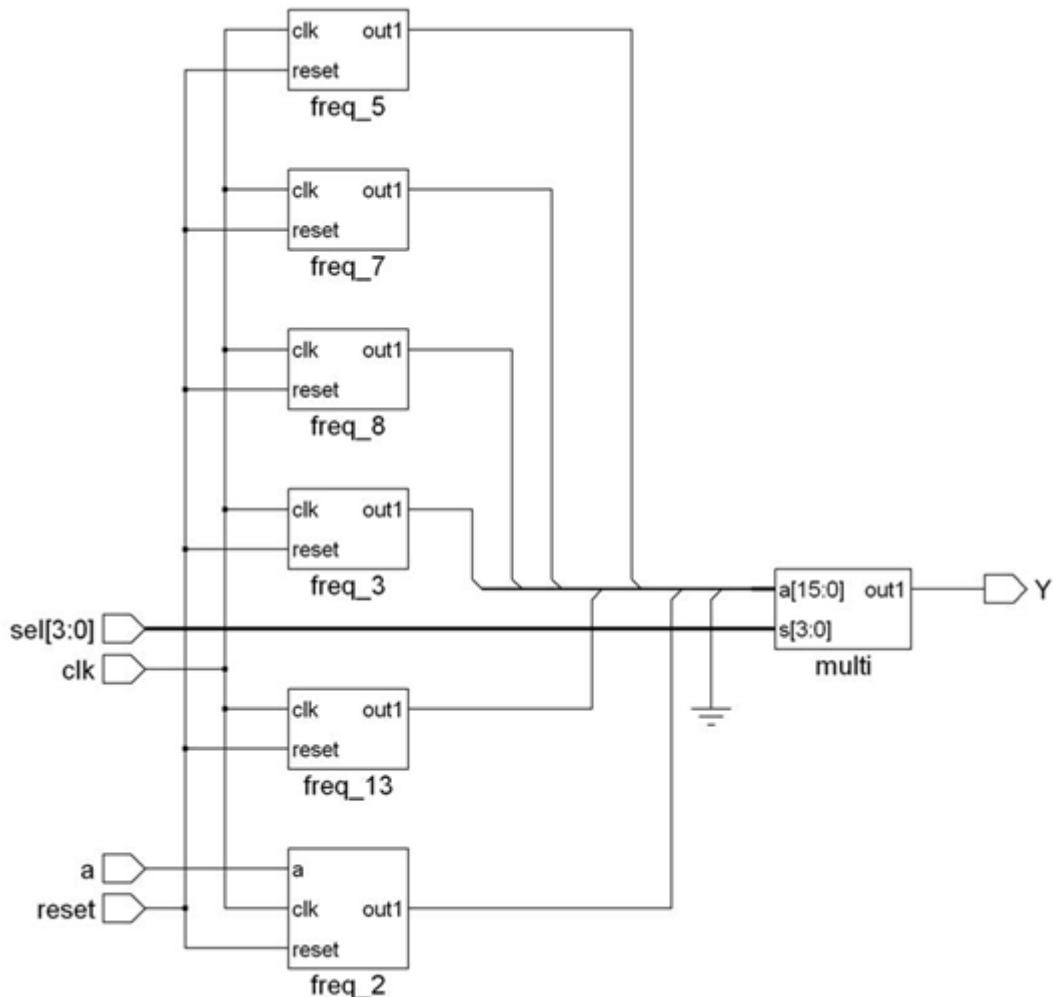
An oscillator is an independent system that generates a periodic output without any input signal. A voltage-controlled oscillator is an electronic oscillator designed such that its oscillation frequency is controlled by a voltage input. The frequency of oscillation is controlled by the applied DC voltage, while modulating signals may also be fed into the VCO to cause frequency modulation or phase modulation. The frequency of oscillation must be tunable for the phase of a PLL to be adjustable [4].

### 3.5 Frequency divider:

For clock generation, mostly reference frequencies are limited by the maximum frequency decided by a crystal frequency reference. The divider's purpose is to scale down the frequency from the output of the voltage controlled oscillator so that the system can operate at a higher frequency than the reference signal. Thus the VCO has to be designed such that the output of VCO is = N times the reference frequency. So the output of the VCO is passed through a divide by N-counter and feedback to the input. The D flip flop based divider has been chosen for this particular application because of practical reasons [2].

## 4. Implementation Results:

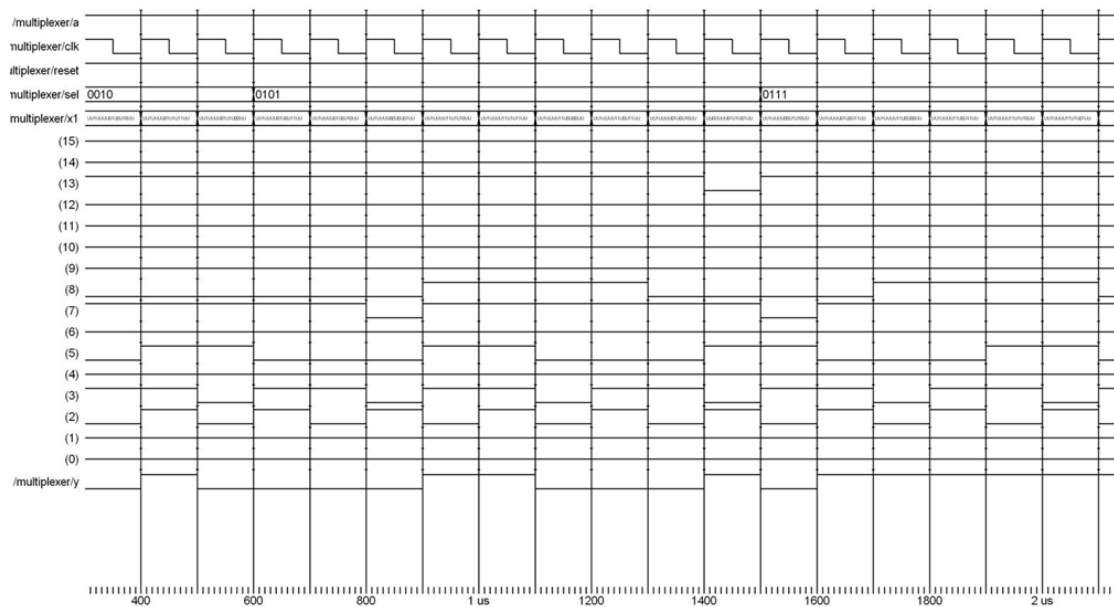
### 4.1 RTL Schematic:



**4. 2 Calculated duty cycle for dividers:**

Name of divider	calculation	Duty cycle [%]
Frequency divide by 3	$(24/48) * 100\%$	50%
Frequency divide by 3	$(68/90) * 100\%$	75. 5%
Frequency divide by 5	$(200/500) * 100\%$	40%
Frequency divide by 7	$(600/700) * 100\%$	85%
Frequency divide by 8	$(400/800) * 100\%$	50%
Frequency divide by 13	$(1200/1300) * 100\%$	92. 3%

**4. 3 Simulated waveform:**



**5. Conclusion:**

In this work, a programmable frequency divider suitable for millimeter wave phase-lock loops has been presented. In the following, a list of claims, innovations, and possible improvements for the presented design, is reported: 1) The addition of a fast reset implementation in the evaluation stage of the dynamic D-FF allowed higher speed reset in the divide-by-13 divider compared with traditional static D-FF designs; 2) The implemented architecture is modular, and therefore easily expandable: addition of new frequency division ratios and/or output channels can be done just adding the required divider chains and setting the needed number of control bits to the output multiplexer; 3) Since the presented programmable frequency divider is suited for PLL applications, not 50% output frequency duty-cycle does not represent an issue thanks to the edge-triggered logic implemented in the most phase-frequency detectors (PFDs): this fact allows the simplification of the divider architecture thus allowing

higher maximum operating frequencies; 4) Power consumption can be further reduced without any maximum speed degradation, switching off the unused divider chains when the desired one is selected by the output multiplexer.

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