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# 1-Bit Full-Adder cell with Optimized Delay for Energy- Efficient Arithmetic Applications

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**Abstract**

A high speed, low power full-adder cell is proposed using multiplexer logic that has resulted in reduced power-delay product in comparison with other full adder logic styles. The analysis for various full-adder cell designs for propagation delays at 0.06 µm 0.08µm, 0.12µm, 0.18µm, 0.25 µm technologies is carried out. The simulation results depict that the proposed design leads to efficient full-adder cell in terms of propagation delay irrespective of the technology used.

**Keywords:** Full-adder, full-adder with multiplexer, low delay, low power.

## INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where delay and power dissipation has become as important a consideration as performance and area. Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for many applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells.

To meet the growing demand, a new low power 1-bit adder cell with an alternative logic structure which uses multiplexers and an inverter is proposed. The resultant full adder cell demonstrates improvement in the propagation delay.

The rest of the paper is organized as follows: In sections II and III existing designs are described. Section IV introduces the proposed logic. In section V simulation results are given and compared, followed by conclusions in section VI.

# PREVIOUS WORK

## GENERALIZED FULL ADDER

The internal logic structure shown in the figure 1 has been adopted as the standard configuration in most of the 1-bit full-adder enhancement developed modules, which include block-1( to obtain XOR/XNOR) , block-2 and block-3 (multiplexers) to obtain sum and carry.

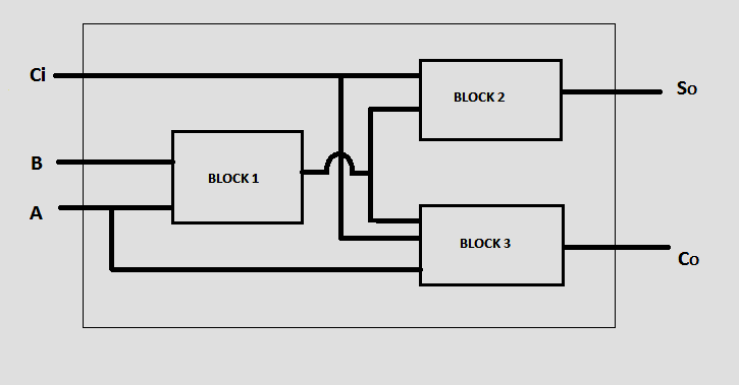


Figure 1: Full-adder cell formed by three main logical blocks

The major problem regarding the propagation delay for the logic structure of the above shown full adder was presented after a comparative study in [2] and an important conclusion was pointed out that it is necessary to obtain an intermediate (A XOR B) signal and its compliment, which are used to drive the blocks 2 and 3 to generate the final outputs. Thus, the power consumption and the overall propagation delay depend on the delay and voltage swings of the intermediate signal and its compliment generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of the intermediate signal to control the selection or transmission of other signals located on the critical path.

## ALTERNATIVE LOGIC STRUCTURE FOR A FULL- adder

The full-adder cell shown in the figure 2 was proposed using DPL and SR-CPL logic styles by Mariano Aguirre-Harnandez and Monico Linares-Aranda in [3]. This is a good design which is flexible for digital circuits [4].

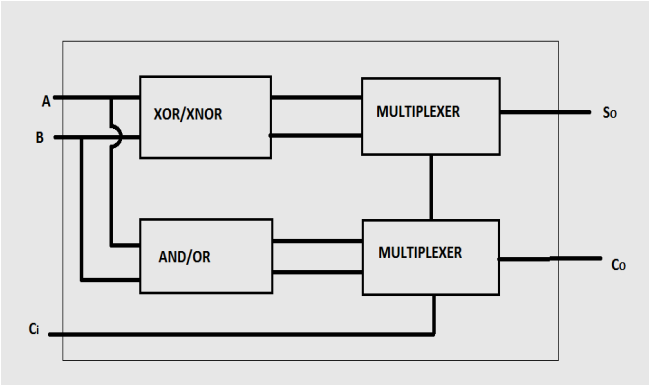


**Figure 2:** Alternative logic structure for designing full-adder cell

The advantage of the above structure is that it does not generate any intermediate signal, reduces the transistor count. But the delay is not reduced to the satisfactory level. There is still scope to reduce the propagation delay. In order to overcome the above mentioned problems of the existing designs, a low power and very fast adder circuit design is proposed.

**PROPOSED FULL-ADDER**

Considering the power dissipation as a critical design parameter, a design that does not generate the intermediate signal for minimizing the delay component has been presented.

**Truth Table**

| C | B | A | SUM(S) | CARRY(C0) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

From the truth table of the full-adder it can be seen that, when CB=00, SUM=A, CARRY= 0. When CB=01, SUM=$\bar{A}$, CARRY=A. When CB=10, SUM= $\bar{A}$, CARRY=A. When CB=11, SUM=A, CARRY=1[5].

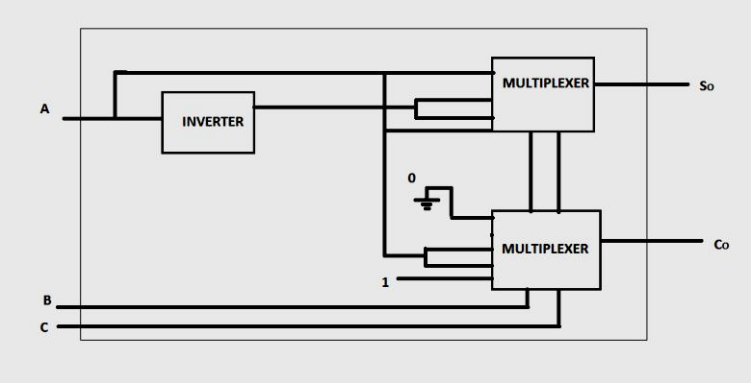


**Figure 3:** Logic structure for proposed full-adder cell

Thus multiplexers can be used to obtain the outputs sum and carry taking values of inputs CB as select lines. Hence an alternative logic scheme to design a full-adder can be formed by two multiplexers to obtain outputs sum and carry and an inverter at the input. The circuit diagram is given in the following figure 4.

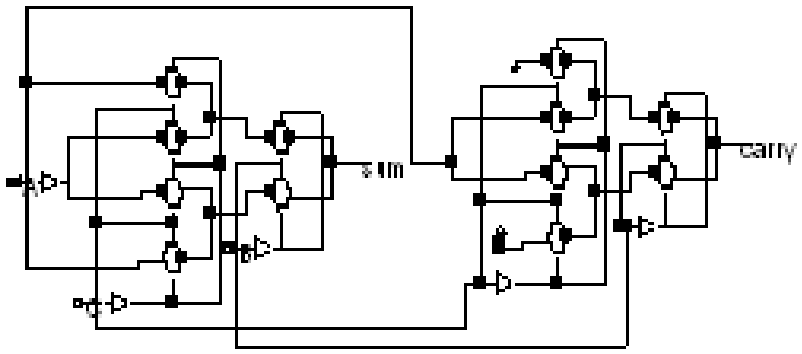


**Figure 4:** Full-adder designed with the proposed logic structure

The core part in this full-adder is the multiplexer logic. Two highly effective multiplexers are shown in this design (figure 4), the basic topology of which is to implement the logic functions of the full-adder in few steps. The efficiency comes from the two facts,(i)No intermediate signals are generated (ii) The capacitive load of the input has been reduced as it is connected to less number of transistors. Thus the overall propagation delay is reduced.

It is found that overall Power-Delay Product can be reduced by up to 36% than DPL logic and 14% than the PDP in SR-CPL logic. Also the delay is reduced by 42% than DPL logic and 35% than the delay in SR-CPL logic.

## FURTHER WORK ON PROPOSED FULL-ADDER BY SCALING DOWN THE TECHNOLOGY

The size of the transistor is usually defined in terms of its channel length L. As the channel length is scaled down, the edge of the depletion region around the source comes closer to that around drain. In order to prevent punch-through and maintain transistor action, the depletion region widths must also be scaled down such that the channel length L must be at least 2d. Therefore, L is in turn determined by the substrate concentration (N) and supply voltage (Vdd). N is increased to reduce d, Vdd is also scaled down. But this will increase the threshold voltage (Vt) which is against the required trends of scaling down. However, the deep channel implantation technology increases N only near the source and drain to substrate junctions. Due to scaling down Vdd, the time taken to develop the channel increases, resulting in increased propagation delay [6].

The performance of the proposed logic design is analyzed by scaling down the technology and compared with the other logic designs.

Although they all perform the same function, their styles of generating the intermediate nodes and the outputs are different, the loads on the inputs and intermediate nodes are different, and the transistor count varies significantly.

## SIMULATION RESULTS AND COMPARISON

In this section the performance of the proposed design is analyzed and compared. The simulations are performed using Micro wind2 simulation tool and nominal temperature of 27°C to extract the worst delay. The analysis for various full-adder cell designs for propagation delays at 0.06 µm, 0.08µm, 0.12µm, 0.18µm, 0.25 µm technologies is carried out and is shown in table II. The PDP and delay are plotted for different designs and compared, shown in figures 5 and 6 respectively.

The minimum delay is given by the SR-CPL logic design compared to the DPL logic and the best is made of the proposed design which uses only multiplexers and gives the least delay among the different technologies that are compared. The simulation results depict that the proposed design leads to efficient full-adder cell in terms of critical path delay irrespective of the technology used.

TABLE I -SIMULATION RESULTS OF FULL ADDERS COMPARED (POWER IN µW, DELAY IN nS, PDP IN µW.nS, )

| DESIGN | DELAY (ns) | POWER (µW) | PDP |
|---|---|---|---|
| DPL | 1.42 | 24.66 | 35.017 |
| SR-CPL | 1.28 | 20.23 | 25.894 |
| PROPOSED (MUX) | 0.83 | 26.88 | 22.310 |

TABLE II -SIMULATION RESULTS OF FULL ADDERS COMPARED FOR PROPAGATION DELAY using DIFFERENT TECHNOLOGIES

| DESIGN | Technology µm | DELAY (ns) |
|---|---|---|
| DPL | 0.06 | 3.5 |
| | 0.08 | 3.5 |
| | 0.12 | 1.42 |
| | 0.18 | 1.9 |
| | 0.25 | 1.9 |
| SR-CPL | 0.06 | 3.1 |
| | 0.08 | 3.1 |
| | 0.12 | 1.28 |
| | 0.18 | 1.8 |
| | 0.25 | 1.8 |
| PROPOSED (MUX) | 0.06 | 2.0 |
| | 0.08 | 2.0 |
| | 0.12 | 0.83 |
| | 0.18 | 1.1 |
| | 0.25 | 1.1 |

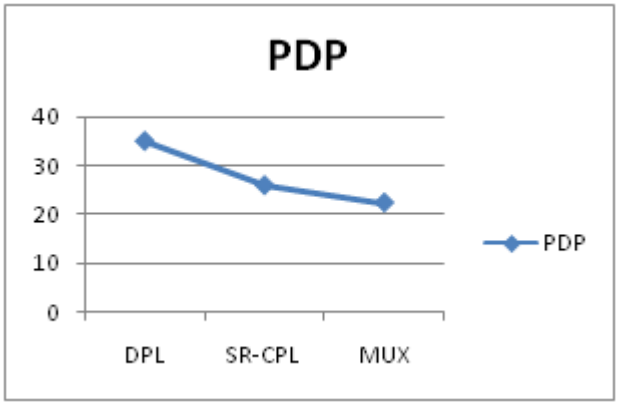


**Figure 5:** Power-delay product(PDP) comparison

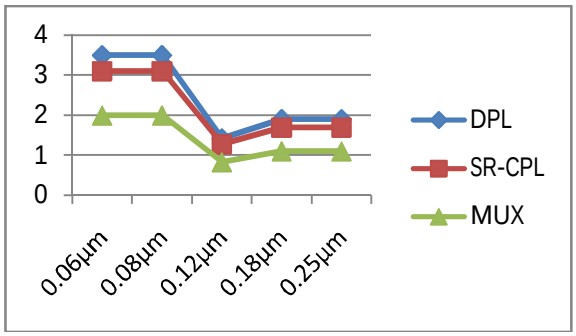


**Figure 6:** Comparison of delay for full-adder cell using different logic designs.

## CONCLUSIONS

Various designs for low delay full-adder are analyzed and their performance evaluated. It is found that propagation delay for the proposed logic can be reduced by up to 58.5% for technologies upto 0.12µm and 24.5% than the technologies beyond 0.12 µm.

The performance of the proposed full-adder design has been shown to outperform the other two designs.

Applying the explanation, results and comparison from the previous sections, it is estimated that the minimum possible channel length to be 0.12µm.

Thus a satisfactory level propagation delay can be achieved. Consequently, the proposed design is suitable for the application in the high performance arithmetic and VLSI circuits in the future.

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