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VLSI Design and Implementation of Binary Number Multiplier based on Urdhva Tiryagbhyam Sutra with reduced Delay and Area

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Abstract

This paper proposed the design of high speed and area efficient Binary Number Multiplier often called Binary Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics ie Urdhva Tiryagbhyam Sutra. Urdhva Tiryagbhyam Sutra is the Vedic method for multiplication which strikes a difference in the actual process of multiplication itself, giving minimum delay for multiplication of all types of numbers, either small or large. The work has proved the efficiency of Binary Number Multiplier designed using Urdhva Tiryagbhyam Sutra where multiplication process enables parallel generation of intermediate products and eliminates unwanted multiplication steps. Further, the Verilog HDL coding of Urdhva Tiryagbhyam Sutra for 23x23 bits multiplication and their implementation in Xilinx Synthesis Tool on Spartan 3E kit have been done. The propagation time for the proposed architecture is 26.559 ns. The results shows that the implemented Binary Number multiplier is efficient in terms of area and speed compared to its implementation using Array multiplier architectures.

Keywords— Arithmetic and Logical Unit, Array Multiplier, Binary Vedic Multiplier, Urdhva Tiryagbhyam Sutra.

1. Introduction

Multipliers are essential component of all the computer systems, cellular phones and most digital audios / videos etc. The important functions implementing multiplier are

Inverse Discrete Cosine (IDCT), Fast Fourier Transforms (FFT), and Multiply Accumulate (MAC)[1].The known method of conventional multiplication in a math coprocessors are array multiplication, booth multiplication each with its own limitations. The array multiplier does parallel multiplication. The array multiplier performs the parallel multiplication. The parallel multiplication process is based on the fact that in multiplication partial products can be independently computed in parallel. Array multiplier is a fast way of multiplying two numbers since the delay it takes, is the time for the signals to propagate through the gates that form the multiplication array but large number of logic gates are required to design array multiplier due to which of the area of multiplier architecture increases. So, there is a need for an improved multiplier architecture that has the simple design advantages, but which does not suffer the excessive delays associated with conventional multiplier structures[2, 3].

Many attempts have been reported in literature about improvement in multipliers that have the least number of gate delays and consume the least amount of chip area. Based on the comparison, Binary Vedic multiplier based on Urdhva Tiryagbhyam Sutra(Vertical and Crosswise algorithm) is one of the fast and area efficient multiplier.

The proposed Binary Vedic multiplier is based on the Vedic Sutras(formula) called Urdhva Tiryagbhyam Sutra. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics[4, 5].

2. Vedic Multiplication Scheme

Vedic Mathematics was written by Jagadguru Swami Sri Bharati Krsna Tirthaji Maharaja (1884-1960)(Sankaracharya of Govardhana Matha, Puri, Orissa, India). He comprised all his work together and gave the 16 sutras (aphorisms or formulae) and their corollaries [4]. The list of these main 16 sutras and of their sub-sutras or corollaries is prefixed in the beginning of the text and the style of language also points to their discovery by Sri Swamiji himself.

It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Application of the Sutras saves a lot of time and effort in solving the problems, compared to the formal methods presently in vogue. Though the solutions appear like magic, the application of the Sutras is perfectly logical and rational. The computation made on the computers follows, in a way, the principles underlying the Sutras. The Sutras provide not only methods of calculation, but also ways of thinking for their application.

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc[4]. The 16 Sutras and their Sub sutras or Corollaries are listed below

SI. No	Sutras	Sub sutras or Corollaries
1.	Ekādhikena Pūrvena (also a corollary)	Ānurūpyena
2.	Nikhilam Navataścaramam Daśatah	Śisyate Śesamjnah
3.	Ūrdhva - tiryagbhyām	Ādyamādyenantyamantyena
4.	Parāvartya Yojayet	Kevalaih Saptakam Gunỹat
5.	Sūnyam Samyasamuccaye	Vestanam
6.	(Ānurūpye) Śūnyamanyat	Yāvadūnam Tāvadūnam
7.	Sankalana - vyavakalanābhyām	Yāvadūnam Tāvadūnīkrtya Vargaňca Yojayet
8.	Puranāpuranābhyām	Antyayordasake' pi
9.	Calanā kalanābhyām	Antyayoreva
10.	Yāvadūnam	Samuccayagunitah
11.	Vyastisamastih	Lopanasthāpanabhyām
12.	Śesānyankena Caramena	Vilokanam
13.	Sopantyadvayamantyam	Gunitasamuccayah Samuccayagunitah
14.	Ekanyūnena Pūrvena	
15.	Gunitasamuccayah	
16.	Gunakasamuccayah	

The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing [1, 4].

3. Urdhva-Tiryagbhyam Sutra

"Urdhva" and "Tiryagbhyam" words are derived from Sanskrit literature. Urdhva means "Vertically" and Tiryagbhyam means "crosswise" [7]. It is based on a novel concept, where the generation of all partial products can be done with the concurrent addition of partial products. Anyone can easily realize that this Vedic method probably makes difference for mental calculations [12, 14]. For mental calculations it can be proved more convenient, as we can easily visualize Vedic multiplication line diagram shown in Figure 1. If someone tries to do multiplication mentally, in a conventional method, one would have to remember first row, then second row and likewise; then add all of them. In some cases it might be difficult to remember these

many numbers at a time. But in this Vedic method, to visualize line diagram and keep adding two consecutive product terms is easier for manual calculations. One needs to memorize only few numbers. So, one may find Vedic multiplication faster or more convenient for manual calculations [4].

3.1. Urdhva-Tiryagbhyam Sutra for Decimal Numbers

Ūrdhva Tiryagbhyām sutra which is the General Formula applicable to all cases of multiplication and will also be found very useful later on in the division of a large number by another large number is used to multiply decimal numbers[4].

The formula itself is very short and terse, consisting of only one compound word and means “vertically and cross-wise.” The applications of this brief and terse sutra are manifold. A simple example as shown in Fig.1 will clarify the operation. Suppose we have to multiply 12 by 13.

i. We multiply the left hand most digit 1 of the multiplicand vertically by the left hand most digit 1 of the multiplier get their product 1 and set down as the left hand most part of the answer,
ii. We then multiply 1 and 3 and 1 and 2 crosswise add the two get 5 as the sum and set it down as the middle part of the answer; and
iii. We multiply 2 and 3 vertically get 6 as their product and put it down as the last the right hand most part of the answer.

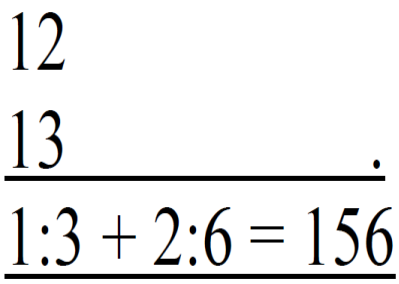

Fig.1 Decimal Multiplication Scheme using Urdhva Tiryagbhyam

3.2. Urdhva-Tiryagbhyam Sutra for Binary Numbers

In binary system only 0 and 1 are used hence multiplication in *Urdhva-tiryagbhyam* or vertically-crosswise formula is replaced by AND logic. AND logic is performed b/w two binary number for multiplication and addition is done according to binary logic[4, 5].

Vedic multiplication algorithm to binary number system with the preliminary knowledge that the multiplication of two bits a0 and b0 is just an AND operation and can be implemented using simple AND gate. To illustrate this multiplication scheme in binary number system, let us consider the multiplication of two binary numbers x3x2xlx0 and y3y2yly0. As the result of this multiplication would be more than 4 bits, we express it as... r3r2rlr0 and the carry are expressed as...c3c2c1c0. By mutilpliying two numbers using Urdhva Tiryagbhyam Sutra we get the following expressions:

r0 = x0y0+1'b0+1'b0+1'b0 (1)
clr1 = xly0+x0yl+1'b0+1'b0 (2)
c2r2 = cl+x2y0+xlyl+x0y2+1'b0 (3)
c3r3 = c2+x3y0 + x2yl + xly2 + x0y3 (4)
c4r4 = c3+x3yl+x2y2+xly3+1'b0 (5)
c5r5 = c4+x3y2+x2y3+1'b0+1'b0 (6)
c6r6 = c5+x3y3+1'b0+1'b0+1 'b0 (7)

With c6r6r5r4r3r2rlr0 being the final product. Partial products are calculated in parallel and hence the delay involved is just the time it takes for the signal to propagate through the gates.The multiplication scheme of two binary number is shown in Fig.2.

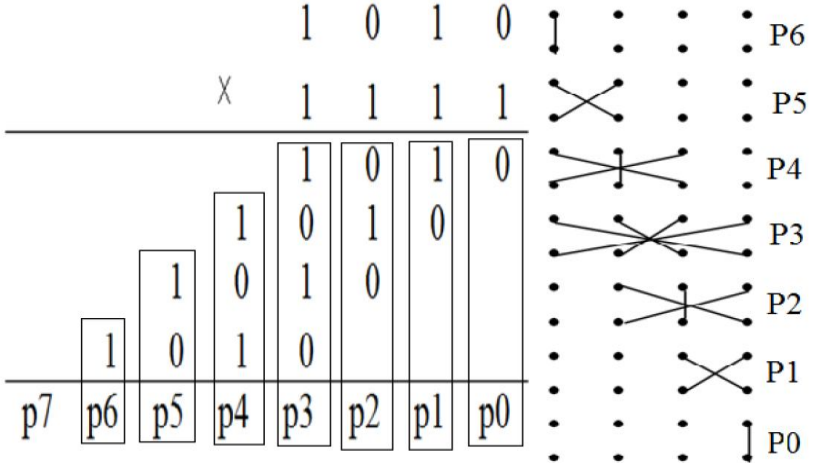

Fig.2 Binary Multiplication Scheme using Urdhva Tiryagbhyam Sutra

4. Implementation of Binary Number Multiplier

In binary system only 0 and 1 are used hence multiplication in *Urdhva-tiryagbhyam* or vertically-crosswise formula is replaced by AND logic. Each AND will be a bit wide and these bits are added together to generate cross-product. Rules for vertically-crosswise multiplication remains same as starting from MSBs – Most Significant Bit, of both multiplicands considered for first cross product. Then increasing one bit in each further calculation with cross product taken for bits of multiplicands till all bits are used. Further dropping bits from MSB process of cross-product is continued till only LSB is used for cross-product and combining of cross product is done further as shown in Fig 4.The proposed multiplier architecture is shown in Fig 3.

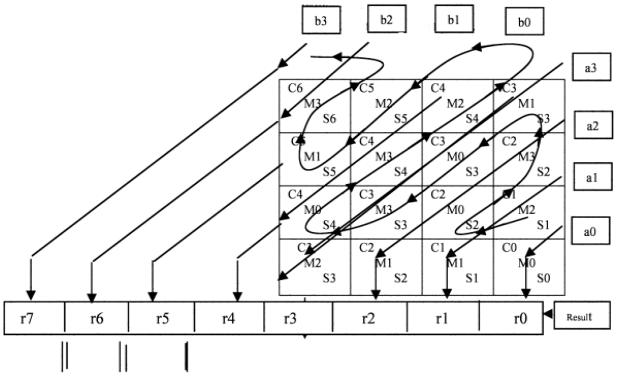

Fig.3 Proposed Binary Number Multiplier architecture for 4-bit multiplication.

In binary number system the maximum width of cross product depends on width of multiplicands. For example, in 8 bit multiplication maximum cross-product width will be $\log_2 8 + 1 = 4$. In 16 bit it will be 5 and in 23 bits it will be 5 again.

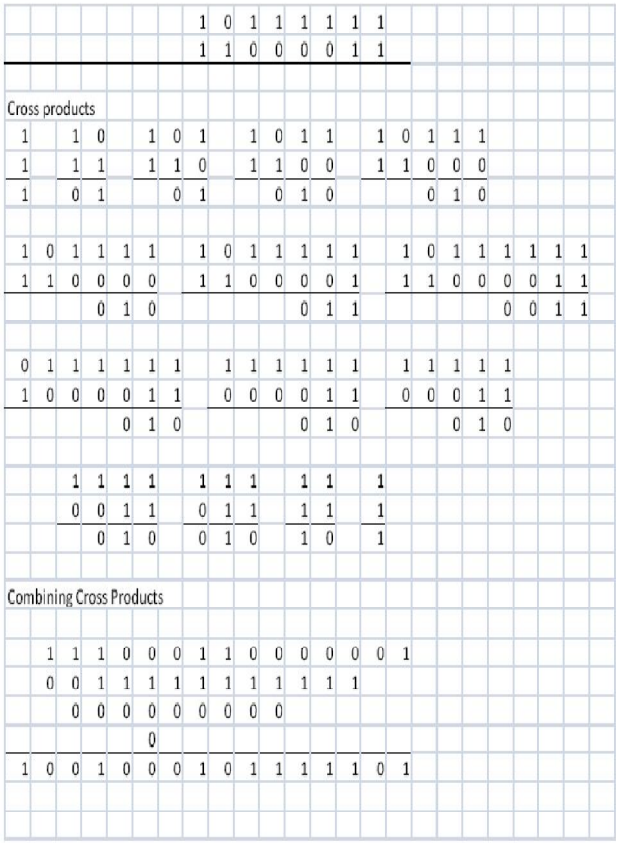

Fig.4 Proposed Binary Number Multiplication Scheme using Urdhva-tiryagbhyam Sutra

5. Results and comparison

The algorithm is designed for 23-bit binary input using Verilog-HDL. Simulation, Synthesis and Implementation is done using Xilinx Spartan-3E FPGA Board of device family xc3s400e-5pq208. The RTL, Technical Schematic and Simulation of 23-bit Binary Vedic multiplier is shown below in Fig5(a), 5(b), 5(c) respectively. The simulation and synthesis results for the 4-bit Binary Number Vedic and Array multipliers are respectively shown below in Fig 6, 7 and their comparison in terms of speed and area are respectively shown below in Fig 8, 9.

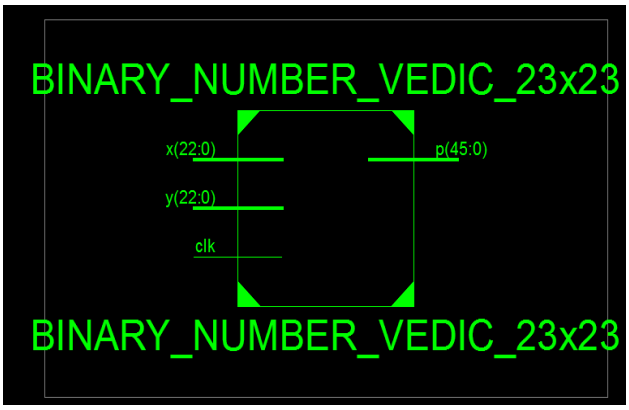

Fig. 5(a) RTL Schematic of 23-bit Binary Number Vedic Multiplier

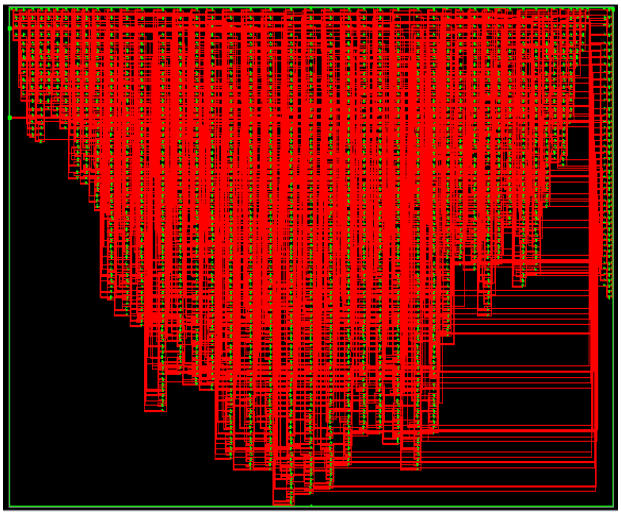

Fig. 5(b) Technology Schematic of 23-bit Binary Number Vedic Multiplier

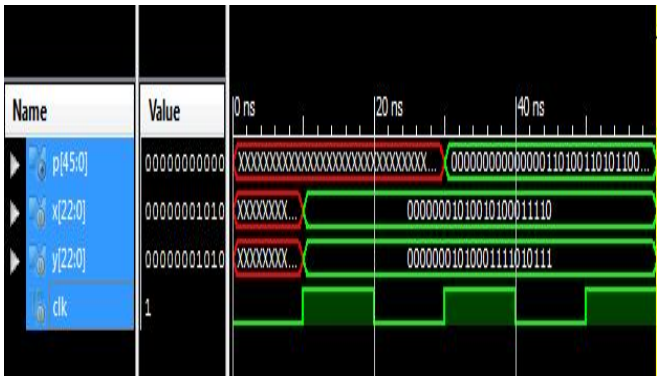

Fig. 5(c) Simulation Result for 23-bit Binary Number Vedic multiplier

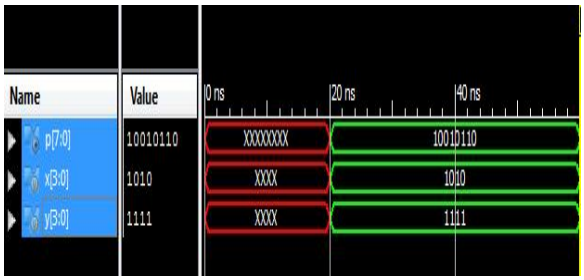

Fig. 6 Simulation Result for 4-bit Binary Number Vedic multiplier

Fig. 7 Simulation results for 4-bit Array Multiplier

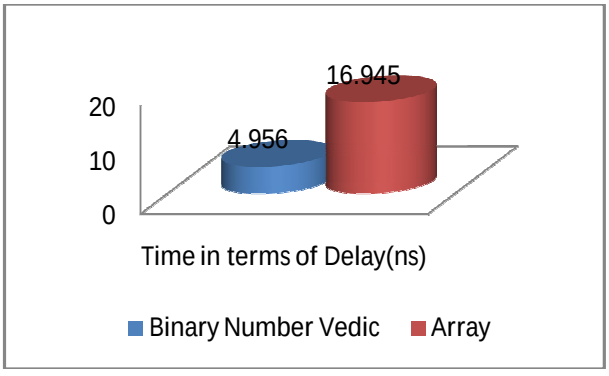

Fig. 8 Comparison of 4 bit Multipliers with respect to Delay

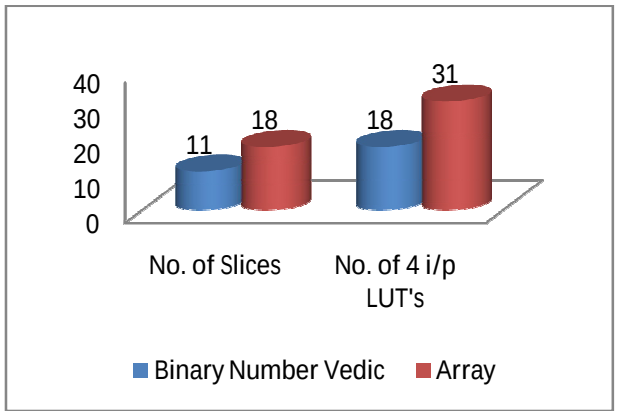

Fig. 9 Comparison of 4-bit Multipliers with respect to Area

6. Conclusion

The designs of 23-bits Binary Number Vedic multiplier have been implemented on Spartan XC3S400E-5PQ208. The design is based on Vedic multiplication scheme [4]. The worst case propagation delay in the 23-bit Binary Number Vedic multiplier is 26.559ns. The advantages of this proposed architecture is efficient in speed and area(1ess resources used, such as less number of multipliers and adders) and is Flexible in design.It is therefore seen that the Binary Number Vedic multipliers are much more faster than the conventional multipliers. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased.

In future, Urdhva-Tiryakbhyam Sutra is implemented along with Nikhilam and Anurupye sutras which can reduce the delay, power and hardware requirements for multiplication of several numbers.

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