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Development of Ge PIN Photodetectors on 300 mm Si wafers for Near-infrared Sensing

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Abstract

SiGe offers a low-cost alternative to conventional infrared (IR) sensor technologies such as InGaAs, InSb, and HgCdTe for developing near-infrared (NIR) photodetector devices that do not require cooling and can operate with high bandwidths and relatively low dark currents. As a result of the significant difference in thermal expansion coefficients between germanium (Ge) and silicon (Si), tensile strain incorporated into SiGe detector devices through specialized growth processes can extend their wavelength range of operation, i.e., to above 1600 nm. We have fabricated SiGe based detector devices on 300 mm diameter Si wafers in order to take advantage of high throughput, large-area complementary metal-oxide semiconductor (CMOS) technology. This device fabrication is facilitated by a two-step growth process involving epitaxial deposition of pure Ge designed to effectively reduce the density of defects and dislocations arising during deposition that form recombination centers which can result in higher dark current. Various techniques including scanning electron microscopy (SEM), Auger electron spectroscopy (AES), high-resolution X-ray diffraction (HRXRD), and secondary ion mass spectrometry (SIMS) have been employed to characterize the material and structural properties of the epitaxial growth and photodetector devices, and these results are presented and discussed in relation to their impact on detector performance.

Keywords: photodetectors, infrared detectors, germanium, thin films, wafers

1 Introduction

1.1 Conventional detector materials and devices

Detection of near-infrared (NIR) wavelengths (i.e., ~750-2000 nm) is critical for

optical fiber based communications and also can benefit certain defense applications such as hostile fire identification. Although silicon (Si) photodetectors are widely used to detect in the visible to lower NIR wavelength range, the relatively large Si band gap of 1.12 eV, which corresponds to an absorption cutoff wavelength of ~1100 nm, hinders the application of Si based photodetection at longer wavelengths, e.g., 1310 nm and 1550 nm commonly used for telecommunications.

For photodetection applications, group III-V compound semiconductor and HgCdTe based detectors possess advantages including high absorption efficiency, high carrier drift velocity, and mature design and fabrication technology. HgCdTe infrared (IR) photodetectors have been developed for 1-3, 3-5, and 8-14 µm applications,[1] InSb for 3-5 µm applications,[2] and InGaAs for ~1100-1700 nm applications[3] (see Fig. 1).[4] However, these devices typically require cooling for optimal performance, and incorporating them into complementary metal-oxide semiconductor (CMOS) processes generally entails increased complexity and higher costs, requires thick buffer layers due to lattice mismatch, and can potentially introduce doping contaminants into Si layers since III-V materials act as dopants for group IV materials.[5] In contrast to most III-V based detectors, SiGe photodetection devices can operate at room temperature and consequently do not require external cooling equipment, thus offering significantly reduced size, weight, and power (SWaP) as well as lower production costs.[6]

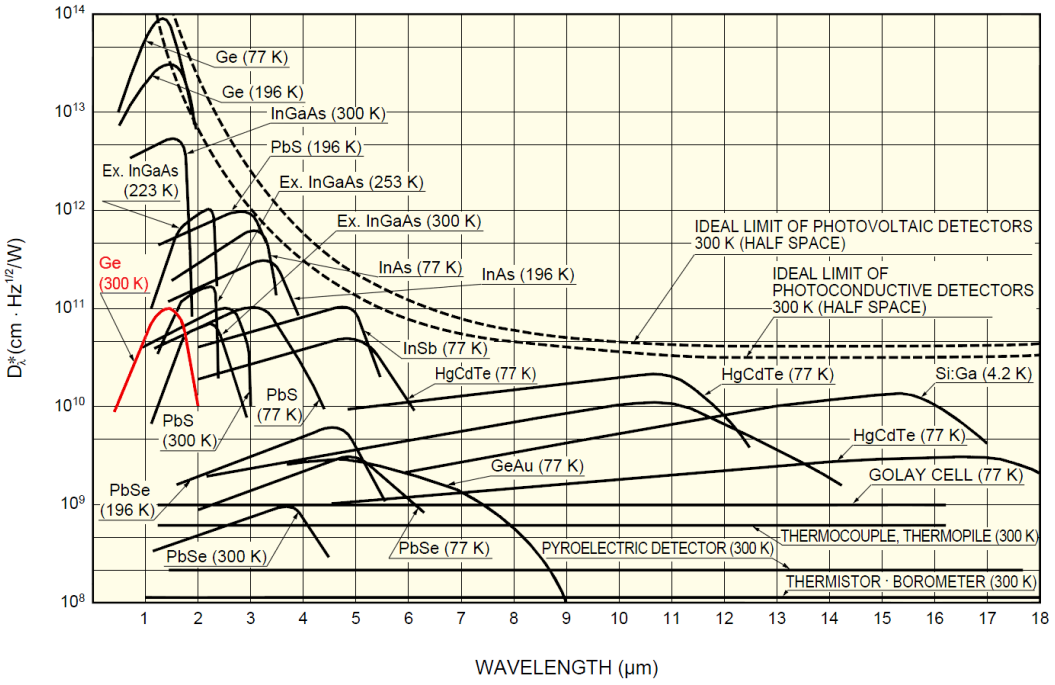

Fig. 1. Detectivity curves for various commercially available IR detectors plotted vs. wavelength. Calculated ideal detectivity limits are indicated by dashed lines.[4]

1.2 Advantages of SiGe based photodetector technology

Like Si, germanium (Ge) is a group IV material that is compatible with both front-

and back-end CMOS processes. Layers of Ge can be heterogeneously integrated with CMOS circuitry using manufacturing infrastructure that is already widely installed for the production of SiGe based CMOS and BiCMOS integrated circuits. This CMOS compatibility enables SiGe device fabrication on leading-edge, large-diameter (300 mm and 450 mm) Si wafers, providing a means of further reducing manufacturing costs and maximizing production output.

Although Ge like Si is an indirect band gap (E_g = 0.66 eV) material, its direct band gap of 0.80 eV is only 140 meV above its dominant indirect band gap. Consequently, Ge/SiGe can be made to behave more like a direct gap material by incorporating additional materials or through the introduction of strain in its crystalline atomic structure.[5,7] Incorporating a relatively low concentration (< 10%) of tin with Ge/SiGe can induce a significant redshift in the material band gap. However, this method is currently associated with high densities of defects and dislocations, and consequently relatively high dark currents have been reported for early GeSn based detector devices.[8] The fabrication method we are utilizing involves incorporating a small amount of tensile strain into deposited Ge layers, which will be discussed in more detail in Section 2.2. Detectors based on strained Ge absorption layers offer substantially higher optical absorption and enhanced transport properties over the 1300-1550 nm and longer wavelength range than Si devices can, making Ge based photodetectors promising candidates for numerous extended NIR sensing applications.

1.3 Potential SiGe detector applications

SiGe based photodetectors have demonstrated responsivities at 1310 nm and 1550 nm that are comparable to or in some cases exceed those of InGaAs based devices traditionally used in telecommunications networks.[9] Ge detectors are also used to realize low-cost and high performance optical interconnections that effectively bridge Si electronics with optics.[10] In addition, the availability of SiGe based NIR sensors can potentially benefit a variety of military applications. These include plume chemical spectra analysis, day-night vision for warfighters and ground vehicles, biochemical threat detection, and also detection of muzzle flash and hostile mortar fire, incendiary events that emit large amounts of energy in the NIR spectral region.[11]

2 Methodology

2.1 Fabrication of Ge based PIN photodetectors

We have fabricated Ge based PIN photodetector devices on 300 mm (12 inch) diameter Si wafers at the State University of New York Polytechnic Institute (SUNY Poly) located in Albany, NY. This facility offers industry-leading photolithography technologies and high-end CMOS fabrication capabilities in a fully-equipped 300 mm cleanroom with large-area Si/Ge tools to demonstrate cutting-edge SiGe technology with small feature sizes for micro-sensor applications.

Compared to metal-semiconductor-metal (MSM) photodetector devices based on SiGe, Ge/SiGe PIN detectors generally provide faster response times and significantly lower dark currents. Responsivities reported for some PIN devices are

as high as ~1 A/W, and even greater for certain waveguide integrated devices.[12,13] Reported dark currents of SiGe PIN photodetectors at room temperature are typically in the nanoamp range, with dark current densities down to the range of μA/cm^2.[14,15] In addition, bandwidths of Ge-on-Si PIN photodetectors have improved from several gigahertz to greater than 49 GHz (and 40 GHz at zero bias) in recent years, fast enough to accommodate future 40 Gb/s telecommunications applications with minimal power requirements.[12,16]

2.2 Incorporating strain to extend NIR response

Since the lattice constant of Ge exceeds of that of Si by 4.2%, very thin epitaxial Ge layers grown on Si substrates are usually compressively strained. The critical thickness for growth of Ge on Si with strain is typically less than 1 nm due to the significant 4.2% lattice mismatch between the materials, and thus a Ge layer grown significantly thicker than this on a Si substrate at temperatures above 600°C will nearly completely relax.[13,17] However, because Ge has a larger thermal expansion coefficient than Si, when the temperature of the deposited layer drops after growth and high temperature annealing, the consequent decrease in the lattice constant of the Ge material is suppressed by the relatively thick Si substrate, resulting in generation of tensile strain in the Ge layer typically in the range of 0.15-0.30%.[5,7]

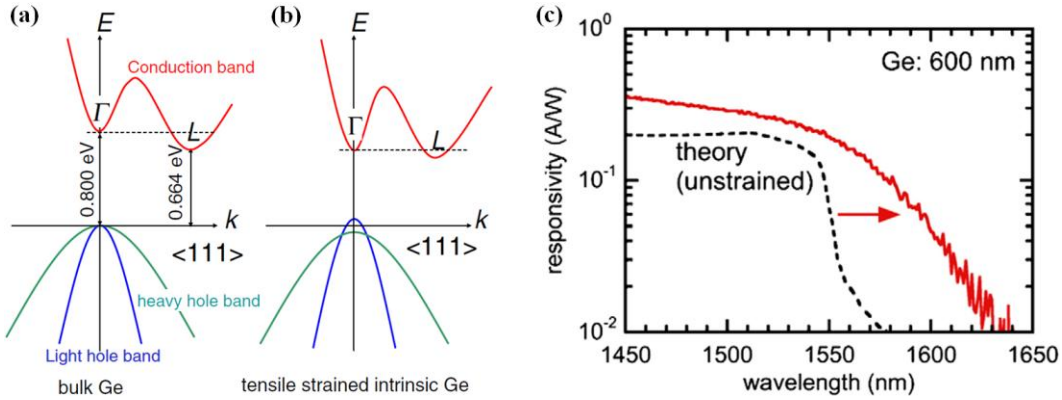

Fig. 2. (a) Schematic band structure of bulk Ge, showing 136 meV difference between direct and indirect band gaps; (b) shift of Ge from indirect gap toward direct gap material with application of tensile strain.[18] (c) Comparison of responsivity spectra for PIN photodetectors having unstrained and strained Ge layers.[19]

The presence of this biaxial tensile stress in Ge causes the valence subbands to split so that the top of the valence band subsequently comprises the light hole band, as can be seen by comparing Fig. 2(a) and 2(b).[18] As the light hole band energy increases both the direct and indirect gaps shrink, with the direct gap shrinking faster. Therefore, with the increase of tensile strain, Ge transitions from an indirect gap material towards a direct gap material. The direct band gap of tensile strained (0.2%) Ge is ~0.77 eV compared to 0.8 eV for unstrained Ge, corresponding to the cutoff

wavelength increasing from 1550 nm to around 1610 nm [Fig. 2(c)], thereby enabling greater sensitivity at longer NIR wavelengths.[19] Photodetectors with tensile strained Ge/SiGe layers can provide high optical absorption over the entire C band (1530-1565 nm) and most or all of the L band (1565-1625 nm) used in fiber based telecommunications.

2.3 Reducing dark current to enhance detector performance

At room temperature, leakage or dark current in PIN photodetectors is mainly due to generation of current through traps at recombination centers formed by defects and threading dislocations arising during the growth process. Since dark current can be particularly high in SiGe based photodetectors, a major focus in the detector design effort is to minimize it as much as is practical in order to enhance sensitivity and boost overall device performance. For high-speed detector operation, dark current levels of 1 μA or less are generally considered acceptable.[20] The reduction in band gap in Ge due to the presence of tensile strain lowers the density of states for holes, leading to a reduction in intrinsic carrier density that effectively reduces the dark current in SiGe devices. In addition, high quality passivation of the device surfaces (e.g., through depositing a top layer of oxide) is a key aspect of fabricating detectors with low dark current, and sidewall passivation is utilized to insulate mesa sidewalls from the signal contact.[21] For the fabrication of our detector devices, we have utilized a two-step growth process that can potentially reduce threading dislocations and resultant dark current by up to two orders of magnitude.[22]

3 Fabrication

3.1 Two-step growth process overview

The two-step growth process employed for deposition of Ge in the fabrication of normal incidence PIN detector devices involves initial low temperature growth of Ge to deposit a thin strain-relaxed seed layer and successive high temperature deposition to form a thicker absorption layer. Photolithographic etching of variously sized windows in an initial oxide layer may be performed to allow selective area growth, or subsequent deep etching utilized as an alternate means to form mesas and isolate the individual devices. The first step of this growth process is intended to reduce threading dislocations arising primarily from lattice mismatch between Si and Ge to enable higher quality Ge films with reduced surface roughness and dark current. All Ge depositions were performed using a 300 mm reduced-pressure chemical vapor deposition (RPCVD) system, utilizing germane as the precursor and hydrogen as the carrier gas with typical reactor pressures in the range of 5-100 Torr. This RPCVD method provides high control of layer and multi-layer thicknesses, making it well suited for future large wafer-scale fabrication.

3.2 Lower temperature seed layer deposition

The first low temperature growth step is crucial toward governing the film crystalline quality and the surface morphology (i.e., reducing islanding and associated surface roughness), enhancing the migration of threading dislocations (Fig. 3) to decrease

their proliferation, and facilitating the final strain state in the Ge films.[17] This process involved fully planar homoepitaxial growth of thin 45-90 nm Ge p^+ (boron) doped seed/buffer layers on p^+ 300 nm Si wafers, the latter of which were characterized by resistivities in the range of 0.005-0.02 Ω·cm.

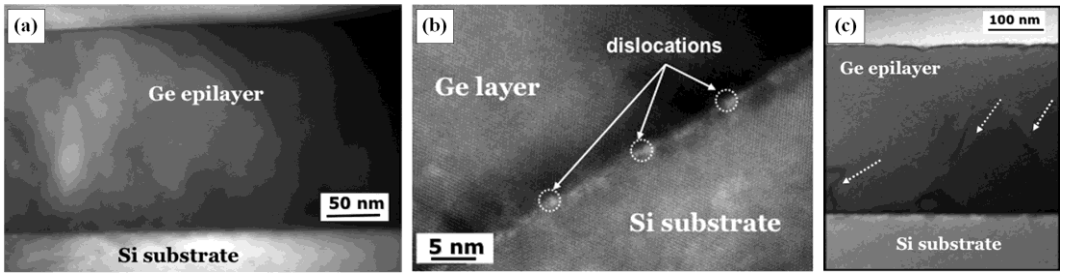

Fig. 3. (a) Cross-sectional transmission electron microscopy (TEM) image of Ge layer grown on Si; (b) enlargement of layer in (a) near the interface region, showing a high density of misfit dislocations; and (c) TEM image of the Ge layer grown following a two-step growth process, where threading dislocations are less evident.[17]

This deposited seed layer, a small portion of which was initially strained due to the lattice mismatch between it and the underlying Si substrate, is designed to prevent strain release from undesirable three-dimensional (3D) island growth. A sufficiently high doping level ($\geq 10^{19}$ cm^{-3}) is required to enhance the seed growth rate and lower the Ge/Si interfacial oxygen level.[23] At relatively low growth temperatures in the range of 350-400°C intended to promote planar growth, the low surface diffusivity of Ge kinetically suppresses undesired islanding that can otherwise result.[9] By contrast, seed layer deposition at temperatures below 320°C commonly leads to crystallographic defect formation, while that at temperatures above 400°C can produce surface roughening due to the increased surface mobility of Ge.[22]

3.3 Higher temperature intrinsic layer deposition

In the subsequent high temperature step of the growth process, a layer of intrinsic Ge serving as the absorption region was grown at 550-600°C. This temperature range was chosen to ensure satisfactory deposition rates for smooth high crystal quality Ge films with sufficient tensile strain.[9] The target thickness of this layer is 1-2 μm; increasing this thickness further generally provides higher detector responsivities but results in lower bandwidths. Rather than implementing a post-growth annealing step as is common following the two-step process, the devices were annealed *in situ* during the growth at temperatures up to 800°C. Upon cooling following the high temperature growth and annealing, tensile strain arises in the intrinsic layer due to the difference between the thermal expansion coefficients of the Ge layer material and the Si substrate as described above.

3.4 Remaining growth steps

Following the two-step growth, a layer of polycrystalline silicon *in situ* doped with

phosphorus was deposited above the intrinsic Ge layer, providing a conductive path to the opposite site of the detector. The RPCVD precursor and dopant source for deposition of the polysilicon were disilane and phosphine, respectively. This contact material was grown as an amorphous film at temperatures below 600°C and pressures of 10-200 Torr. This polysilicon layer was designed to be relatively thin (less than 200 nm) so as to limit potentially adverse effects of free-carrier absorption, which increase as the NIR wavelength increases. Spike-annealing at 800°C was then performed to activate the dopants, recrystallize the amorphous silicon, and drive the dopants into the Ge layer to form a thin n^+ Ge region.

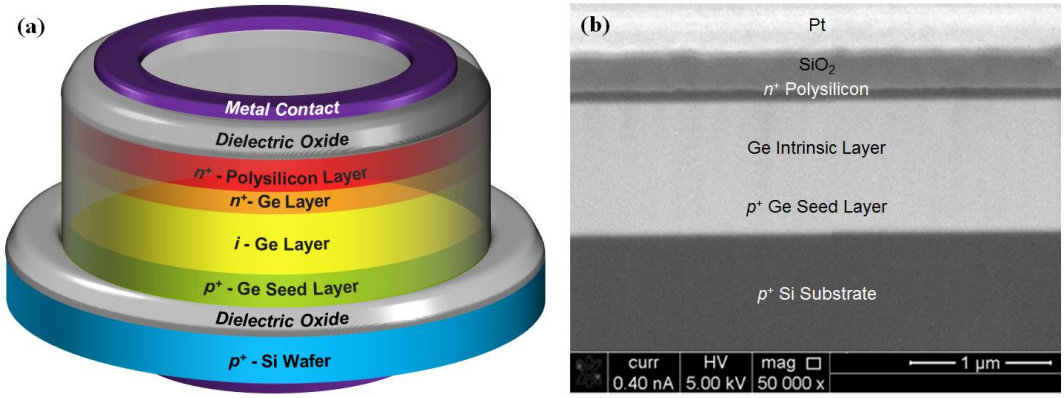

Fig. 4. (a) Schematic representation of final SiGe PIN photodetector device (not drawn to scale); (b) focused ion beam (FIB) cross-sectional image of fabricated SiGe photodetector device covered with a layer of platinum.

A layer of SiO_2 was then deposited on top of the polysilicon. This oxide layer was intended to isolate states at the layer interface from signal carrying layers to prevent communication between the interface states and the intrinsic Ge layer, and also to reduce traps that can contribute to leakage current.[24] Finally, windows in this oxide layer were patterned using a photolithographic process and copper top contacts deposited in these openings, with bottom contacts likewise deposited on the backside of the substrate. The final PIN photodetector device is schematically illustrated in Fig. 4(a), and Fig. 4(b) comprises a cross-sectional focused ion beam (FIB) image of a fabricated device showing the individual layers.

4 Characterization

Various characterization techniques were employed in order to determine material and structural related properties of the epitaxial layer growth and fabricated SiGe PIN photodetector devices. Auger electron spectroscopy (AES) analysis, performed to characterize the film composition [Fig. 5(a), *inset*], shows a sharp Ge peak evidencing an intrinsic layer composed essentially of 100% Ge as no significant peaks corresponding to Si or other constituent elements were observed. A detector intrinsic absorption region composed of pure Ge rather than $Si_{1-x}Ge_x$ further minimizes the band gap to enable extended detection in the NIR regime.

Optical microscopy demonstrates that the Ge epitaxial film topologies, which in earlier processed wafer samples had rough and pitted surfaces, when grown on seed layers 45-90 nm thick are very smooth and virtually defect-free as shown in Fig. 5(a). This is in contrast to Ge intrinsic layers grown on 22 nm thick seed layers, for which a surface defect density of approximately 2000/cm^2 was observed. Consequently the thicker seed layers were found to be most optimal, which may be attributed to a higher degree of relaxation present in their growth process.

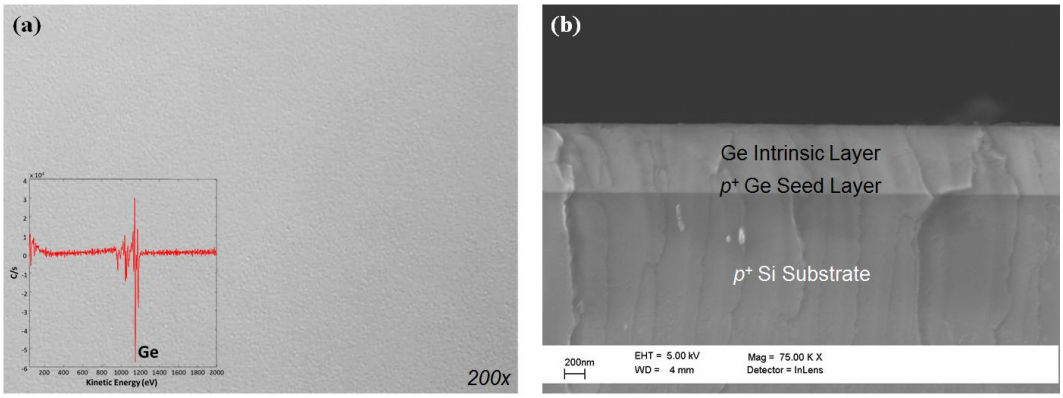

Fig. 5. (a) Optical microscopy image at 200X magnification of top of wafer following intrinsic Ge layer growth, showing a virtually defect-free surface with low RMS surface roughness; inset shows plotted Auger electron spectroscopy (AES) data evidencing near total Ge concentration in *i*-Ge layer. (b) Cross-sectional scanning electron microscopy (SEM) image of epitaxial Ge intrinsic and seed layers deposited on Si substrate (here it is difficult to differentiate between these two layers due to their nearly identical material composition).

Fig. 5(b) comprises a scanning electron microscopy (SEM) image of epitaxial Ge seed and intrinsic layer growth. The SEM and FIB characterization methods involved capturing cross-sectional images of the wafer with the deposited layers of material to gauge their thicknesses and also the quality of the layer growth and interfaces. As depicted in the SEM image [and verified by secondary ion mass spectrometry (SIMS)], the thickness of the intrinsic Ge layer is close to 1.1 μm, sufficient to provide adequate detector sensitivity in the NIR.

High-resolution X-ray diffraction (HRXRD) data, plotted in Fig. 6(a), shows a peak shift in the negative Q_z direction in reciprocal space confirming epitaxial layers composed entirely of Ge, as well as in the negative Q_x direction evidencing greater than 100% relaxation, i.e., tensile strain; we are looking to quantify the precise amount of this strain utilizing standard XRD measurements. The SIMS measurement results, plotted in Fig. 6(b), show the thicknesses of the intrinsic Ge, polysilicon, and oxide layers to be approximately 1100 nm, 150 nm, and 400 nm, respectively. Measured doping levels indicate boron doping of ~5×10^{19} cm^{-3} in the Ge seed layer, phosphorus doping of 10^{21} cm^{-3} in the polysilicon layer, and doping levels in the intrinsic layer at or below ~5×10^{16} cm^{-3}, the minimum detection limit of the

instrument. In addition, copper contacts have been deposited in oxide windows above the highly doped polysilicon to enable low contact resistance and thus facilitate high speed detector operation. These thicknesses and doping levels largely meet our PIN photodetector design objectives for a device capable of achieving the operational behavior and level of performance described in previous sections.

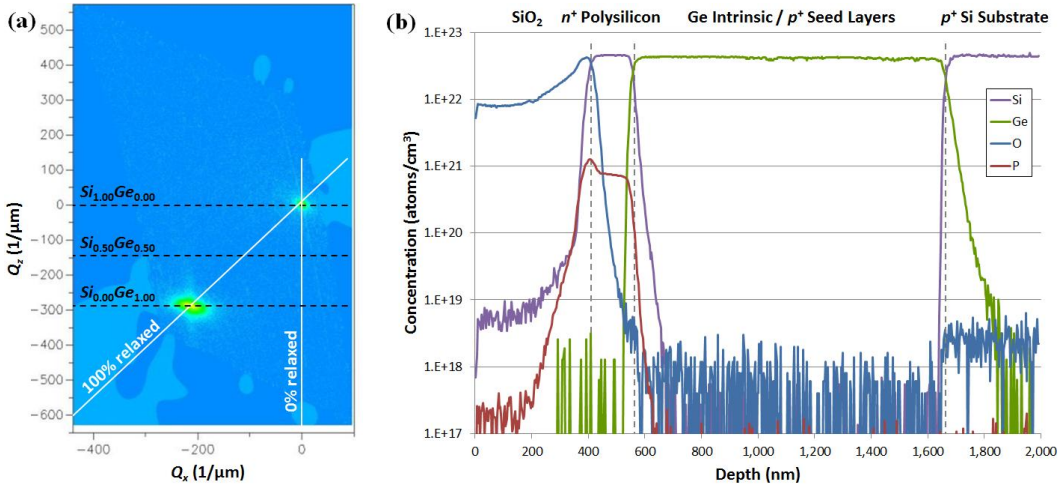

Fig. 6. (a) High-resolution X-ray diffraction (HRXRD) characterization of growth of Ge *i*-layer and p^+ seed layer on 300 mm Si wafer. (b) Plotted secondary mass ion spectroscopy (SIMS) results showing material concentrations and thicknesses of the layers comprising the fabricated PIN detector device. (Due to a variable amount of charging of the sample that occurs while profiling through the top SiO_2 layer, the oxygen profile is not stable within the SiO_2, leading to some uncertainty in its magnitude.)

5 Summary and Conclusions

Uncooled photodetectors fabricated using CMOS processes incorporating growth of epitaxial Ge layers on Si substrates offer a low-cost alternative for NIR detection potentially benefitting both commercial and military applications. Installed infrastructure and leading-edge 300 mm diameter silicon wafer CMOS processing technology are being leveraged to fabricate small feature size SiGe based PIN photodetector devices exhibiting optimal NIR detection properties. Reduction of dark current and incorporation of tensile strain are instrumental in optimizing detector performance and extending the operating wavelength, respectively. We have utilized a fabrication process involving two-step low/high temperature epitaxial growth of Ge on large-area Si wafers to reduce the threading dislocation density and thereby improve device quality and performance. Various methods of characterizing the material properties of fabricated detector devices have yielded results evidencing high quality epitaxial growth of pure Ge with desirable device surface features.

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