International Journal of Engineering Research and Technology.
ISSN 0974-3154 Volume 10, Number 1 (2017), pp. 81-103

http://www.irphouse.com

SiGe Focal Plane Array Detector Technology for Near-Infrared Imaging

Ashok K. Sood, John W. Zeller, and Yash R. Puri
Magnolia Optical Technologies, 52-B Cummings Park, Suite 314, Woburn, MA 01801

Caitlin Rouse, Pradeep Haldar, and Harry Efstathiadis
State University of New York Polytechnic Institute, Colleges of Nanoscale Science and Engineering, 257 Fuller Road, Albany, NY 12203

Nibir K. Dhar
U.S. Army Night Vision & Electronic Sensors Directorate, Fort Belvoir, VA 22060

Priyalal S. Wijewarnasuriya
U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, MD 20783

Abstract

Detection of near-infrared (NIR) wavelengths can benefit a variety of applications, but current NIR-capable sensors typically require cooling and can be difficult and expensive to manufacture. Due to the lower band gap, photodetectors based on Ge can detect NIR radiation of significantly longer wavelengths than possible with Si detectors while maintaining compatibility with complementary metal-oxide semiconductor (CMOS) fabrication processes. SiGe *pin* photodetectors, designed to function as elements in NIR imaging focal plane arrays (FPAs), have been fabricated on 300 mm Si substrates. A two-step low/high temperature growth process was utilized to minimize formation of threading dislocations and thus reduce dark current.

Bright-field scanning transmission electron microscopy (STEM) analysis of cross-sectional detector structures evidenced high quality Ge seed and intrinsic layers with minimal dislocations. The fabricated *pin* detectors characterized by various n^+ region doping levels demonstrated above two orders of magnitude enhancement in current under visible-NIR illumination in comparison to dark current. Front-side illuminated detector devices exhibited dark currents in the

range of nanoamps at -1 V. In addition, the measured zero-bias photocurrent was only marginally less than that at -1 V, potentially benefitting low power requirement NIR detection applications.

1.0 INTRODUCTION

Optical sensing technology plays a critical role for commercial and defense applications requiring infrared (IR) detection, particularly of near-infrared (NIR) wavelengths used for telecommunications. IR photodetectors and detector arrays have traditionally been based on materials including HgCdTe, InSb, InGaAs, and VOx [1]. Group III-V compound semiconductors possess advantages of high absorption efficiency, high carrier drift velocity, excellent noise characteristics, and mature design and fabrication technology [2]. InGaAs IR photovoltaic detectors have been developed for NIR (up to ~1700 nm) applications, InAs for 1-3 µm detection, and InSb for 1-5 µm operational requirements. In addition, HgCdTe, a common and versatile IR material system offering a wide range of spectral operability, has been used extensively for applications spanning 1-5 µm, 8-14 µm, and longer wavelengths [3]. However, III-V and HgCdTe-based detectors often require cooling (typically down to 77K), which increases their size, weight, and power (SWaP). Furthermore, incorporating III-V materials into the prevalent silicon-based fabrication process entails increased complexity and higher costs, and this also can potentially introduce doping contaminants into the silicon since III-V semiconductors act as dopants for group IV materials [4].

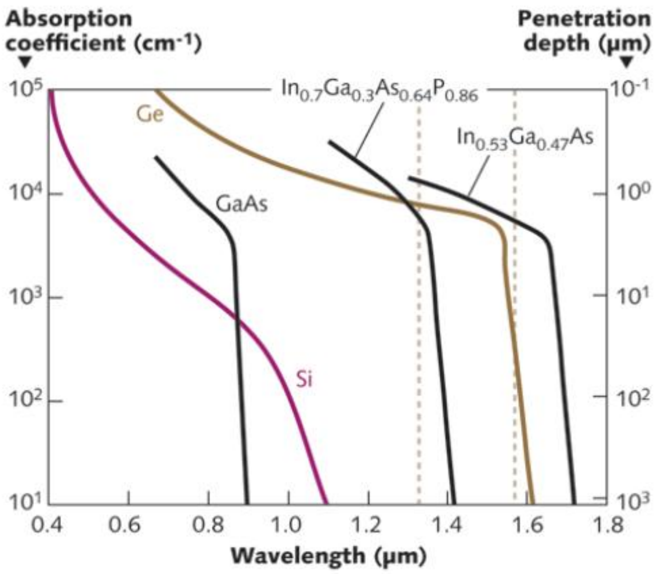

Figure 1. Absorption coefficients for various vis-NIR detector materials plotted vs. wavelength [5].

Given the widespread adoption of silicon in semiconductor manufacturing, Si is a preferable material for detection of visible to short-NIR wavelengths, particularly for applications where cost is a primary concern. However, Si has a relatively large band gap of 1.12 eV, corresponding to an absorption cutoff wavelength of ~1100 nm. This hinders the application of Si photodetectors for longer NIR wavelengths, including those over the 1260 nm to 1625 nm range used extensively for medium- and long-haul optical fiber communications.

Due in part to recent improvements in techniques for depositing epitaxial layers of pure Germanium, Ge now offers a low-cost alternative to III-V compound semiconductors such as InGaAs for developing sensors and detector arrays that do not require external cooling and operate over the visible to NIR spectrum [6]. Figure 1 shows the absorption coefficients of Si, Ge, and certain group III-V semiconductors, which correspond to the spectral responses of detectors based on these materials [5]. Because of their compatibility with Si growth methods using standard complementary metal oxide semiconductor (CMOS) process technology, photodetectors and likewise sensor arrays developed through selective epitaxial growth of Ge can now be heterogeneously integrated with CMOS circuitry. Ge epitaxial growth processes are compatible with both front- and back-end Si CMOS fabrication technologies, enabling very small feature sizes and compatibility with silicon CMOS readout circuits for signal processing.

2.0 BACKGROUND: GE SENSOR TECHNOLOGY

2.1 SiGe Infrared Focal Plane Arrays (IR-FPAs)

A *focal plane array* (FPA) comprises a two-dimensional (2D) assemblage of individual detector pixels located at the focal plane of an imaging system [7]. FPAs convert optical images into electrical signals that can be read out, processed, and eventually stored in digital format if desired. FPAs, also known as *staring arrays*, are scanned electronically typically using circuits integrated within the arrays. Their associated optics serve solely to focus a visual image onto the detectors in the array. The electrical output from the array can be either an analog or digital signal, which in the latter case requires the inclusion of analog-to-digital conversion electronics.

Unlike charge-coupled device (CCD) imagers that require specialized and comparatively complicated processing techniques, imagers based on CMOS technology can be built on fabrication lines designed for commercial microprocessors. This has enabled the resolution of CMOS imagers to continue to increase rapidly in accordance with Moore’s Law due to the ongoing transitions to finer lithographies. The result has been higher circuit density and levels of integration, better image quality, lower voltages, and lower overall system costs for CMOS devices in comparison with traditional CCD-based solutions [8].

Readout integrating circuits accumulate photocurrent from each pixel to provide parallel signal processing circuitry for readout, and are therefore needed for an FPA to be fully functional. CMOS-based silicon ROICs, the dominant technology for large-scale FPAs, are mature with respect to fabrication yield and attainment of near-theoretical sensitivity. ROICs can be processed in standard commercial foundries, and custom designed to feature any type of circuit that will practically fit within the unit cells. ROIC functions include pixel deselecting, antiblooming on each pixel, subframe imaging, and output preamplification [8].

ROICs may be monolithically integrated, where both detection of light and signal readout (multiplexing) is performed in the spacing between the pixels rather than in an external readout circuit [9]. Advantages of this approach include fewer processing steps, increased yield, and reduced costs. Another common architecture for IR-FPAs utilizes a hybrid-based approach where the individual pixels are directly connected with the readout electronics for multiplexing. In addition to allowing independent optimization of the detector material and multiplexer, hybrid-packaged ROICs/FPAs offer near-100% fill factors and increased signal processing area on the multiplexer chip [10].

ROICs comprise input cells or unit cells, which in the case of hybrid FPAs consist of the areas located directly under each pixel. These are connected to the FPA pixels through indium bumps or loophole interconnections which effectively join the aligned FPA and ROIC. Such procedures allow multiplexing the signals from thousands of pixels onto a few output lines. Figure 2 schematically depicts contrasting indium bump bonding and loophole interconnection techniques in a hybrid IR-FPA design [7,10].

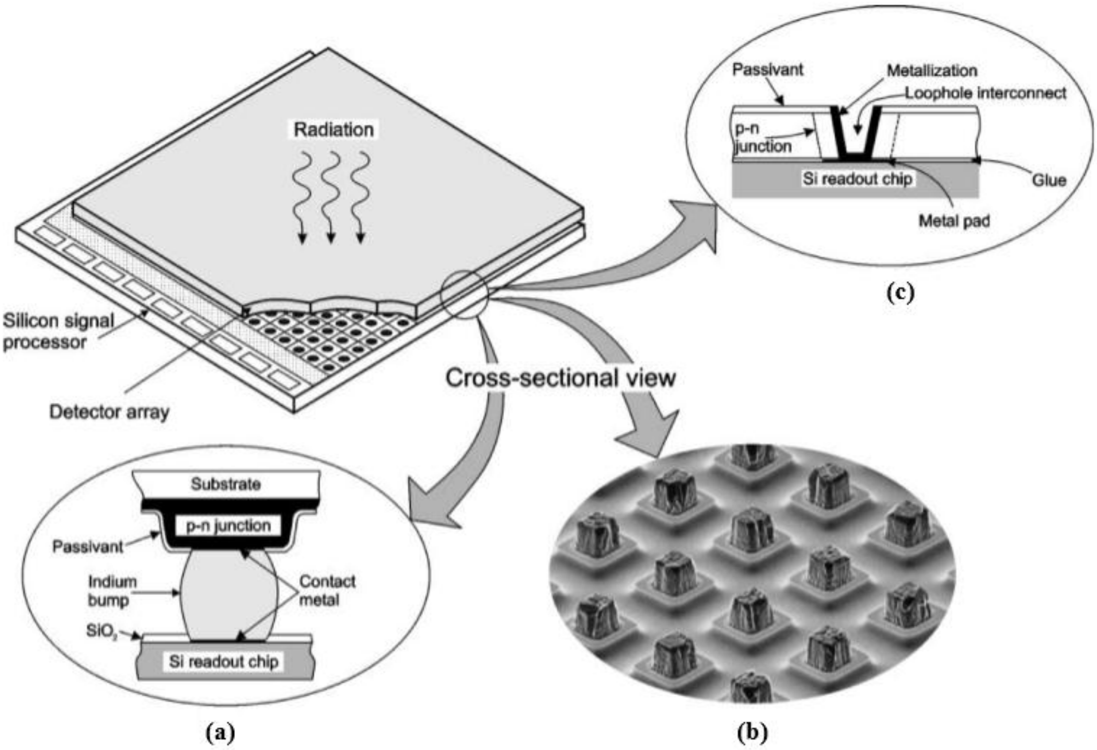

Figure 2. Hybrid IR-FPA with independently optimized signal detection and readout: (a) indium bump technique; (b) individual detector elements; and (c) loophole technique [10].

FPAs employ either front-side illumination, where light is incident on and passes through the ROIC, or backside illumination, where the photons pass through a transparent detector array substrate. The latter approach, though more technologically challenging, is most advantageous since ROICs typically have areas of metallization and other opaque regions that effectively reduce the optical area of the structure [7]. The high fill factors associated with backside illumination also eliminate the need for microlenses, used to concentrate incoming light into photosensitive regions to enhance sensitivity, above each pixel.

2.2 *pin* Detector Elements in FPAs

A photovoltaic photodiode, or photodetector, is basically a device that converts an optical signal (photons) into an electrical signal (electrons, i.e., electrical current), usually while biased. There exist three primary classes of semiconductor photodetectors: avalanche photodiodes (APDs), metal-semiconductor-metal (MSM) detectors, and *p-i-n* (*pin*) detectors. Detectors of each of these three classifications based on SiGe have been demonstrated [4-6]. For the vis-NIR detection applications in view, SiGe devices having *pin* layer structures are well suited.

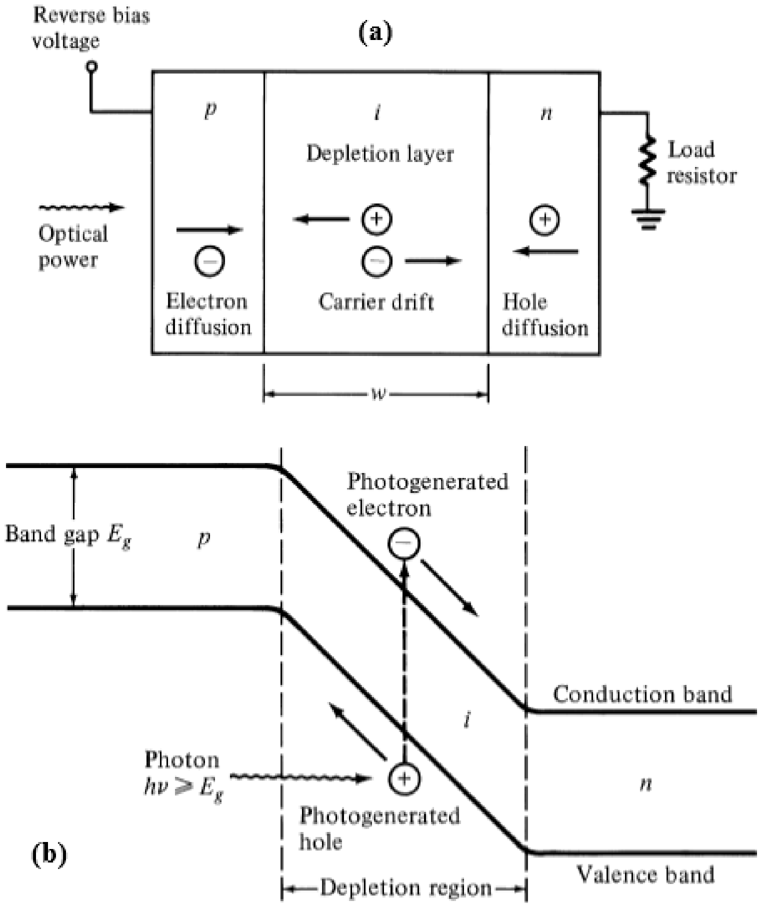

Figure 3. (a) Schematic diagram of a reverse biased *pin* junction and (b) corresponding energy band diagram, illustrating intrinsic photogeneration processes [11].

A typical *pin* structure electrical configuration and associated energy band diagram are given in Figure 3(a) and 3(b), respectively [11]. As the name suggests, *pin* photodetectors generally consist of an intrinsic (*i*) region sandwiched between heavily doped p^+ and n^+ semiconductor layers. The p^+ and n^+ regions may be formed by implantation, *in situ* doping, and/or consist of a highly doped monocrystalline Si substrate [12].

The depletion layer in which all absorption occurs is almost entirely defined by the thicker, highly resistive intrinsic region. The intrinsic/depletion region thickness, normally made substantially larger than that of the p^+ and n^+ regions, can be tailored to optimize detector performance [4]. Since there are relatively few charge carriers in the intrinsic region, the space charge region reaches completely from the *p*-type to the *n*-type layers. SiGe *pin* photodetector structures may exhibit significant built-in electric fields of several kV/cm inside the *i*-Ge/SiGe layers that overcome recombination processes at lattice defects, improving the detector quality and enabling smaller, lower power devices [13].

2.3 Applications of Ge Sensing Technology

Due to their useful performance features and capabilities, room temperature operating SiGe-based detectors and FPAs are potentially beneficial to various commercial and military applications. Unlike their Si counterparts, photodetectors incorporating tensile strained Ge layers can provide high optical absorption over the entire *C* band (1530-1565 nm) and most or all of the *L* band (1565-1625 nm) commonly utilized by optical fiber-based dense wavelength division multiplexing (DWDM) systems extensively employed in telecommunications networks. This feature of Ge detectors is very useful, as expanding the detection limit in the *L* band from 1605 nm to 1620 nm can enable 30 additional channels for long-haul optical telecommunications [14]. SiGe detectors can accommodate current state-of-the-art fiber optical requirements of 200 Gb/s transmission rates, 37.5 GHz bandwidth per wavelength channel with high sensitivity, a broad detection spectrum, and low power requirements [4,15].

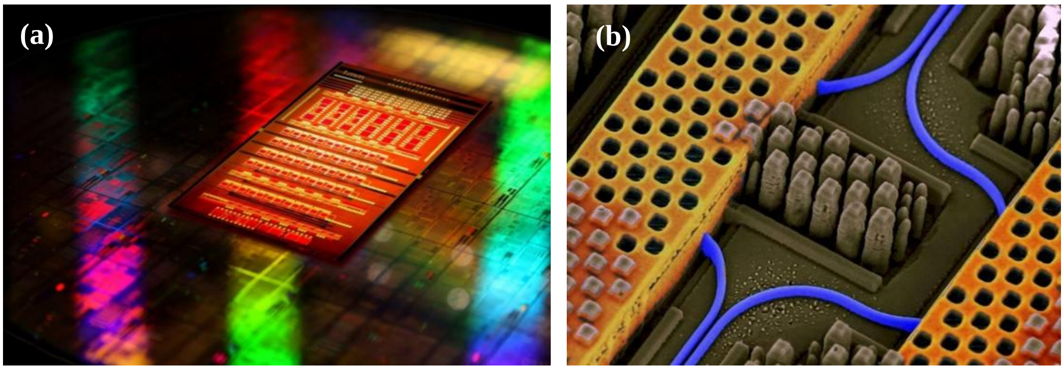

Figure 4. (a) Optoelectronic nanophotonics integrated circuit containing Ge detectors. (b) Magnified view of portion of device, showing integrated optical waveguides (blue) [16].

Ge is also a promising material to bridge low-cost electronics with optics through monolithic integration in next generation Si-based photonic integrated circuits (PICs). Conventional copper interconnects become bandwidth-limited above 10 GHz due to frequency-dependent losses (such as skin effects) and dielectric losses from printed circuit board substrate materials [17]. Photonic interconnection of SiGe photodetectors with optical modulators and passive waveguide components has proven an innovative method for enabling chip-scale data communication [18]. Recent years have seen rapid advancements in the adaption of optical interconnects transitioning from rack-to-rack to board-to board, chip-to-chip, and finally to on-chip applications. The latter two types of applications require high-speed, low cost photodetectors densely integrated with Si electronics. One example of on-chip implementation was demonstrated by the development of a CMOS-compatible nanophotonics chip, shown in Figure 4, containing optical modulators and high bandwidth Ge detectors [16].

Military/defense applications where detection of radiation at NIR wavelengths plays a role include plume chemical spectra analysis, enhanced day-night vision for warfighters and autonomous vehicles, and muzzle flash and hostile mortar fire detection. Muzzle flashes, which approximate a blackbody spectrum from 800K to 1200K, consist of an intermediate flash and (unless suppressed) a brighter secondary flash that produce large amounts of energy in the NIR spectral region [19,20]. The ability to image flashes from hostile fire events combined with target detection capability [e.g., by using spectral tags (chemical additives) for identification of friendly fire] can provide vital information in battlefield situations.

3.0 DESIGN OPTIMIZATION OF GE PHOTODETECTORS

3.1 Incorporating Strain to Extend NIR Detection

Strains and stresses normally arise during epitaxial growth of thin films on substrates having different compositions and/or crystalline structures. If the lattice mismatch between two materials is less than ~9%, the initial layers of film will grow pseudomorphically, straining elastically so as to maintain the same interatomic spacing [14]. As the film grows thicker, the increasing strain will create a series of misfit dislocations separated by regions of relatively good fit.

Since the lattice constant of Ge exceeds that of Si by 4.2%, very thin epitaxial Ge layers grown on Si substrates are usually compressively strained. If a layer of epitaxial Ge is grown thicker than the critical thickness of about 1 nm on a Si substrate at temperatures of approximately 600°C or greater, it will nearly completely relax [21]. However, because Ge has a larger thermal expansion coefficient than Si, when the temperature is reduced after growth the Ge will become suppressed by the thicker Si substrate. This results a reduction in the lattice constant of the Ge and associated tensile strain (typically 0.15-0.30%) arising in the Ge layer [22].

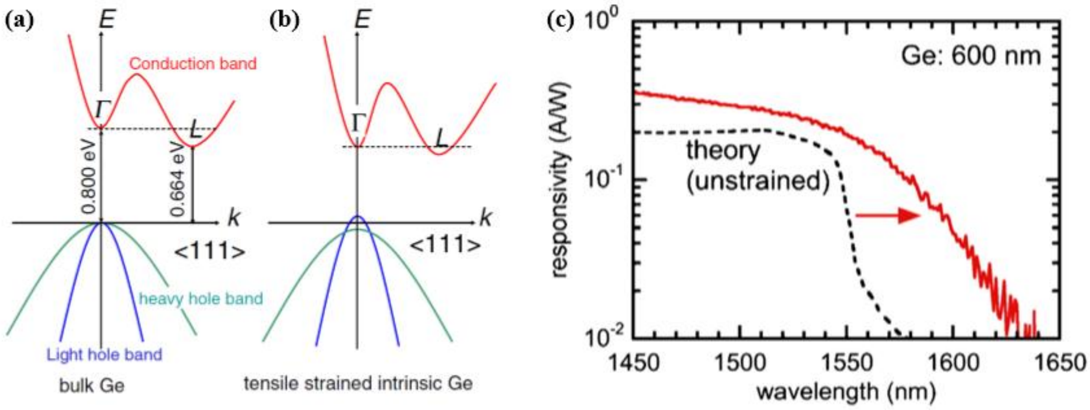

Figure 5. (a) Schematic band structure of bulk Ge, showing 136 meV difference between the direct gap and the indirect gap; and (b) difference between direct and indirect gaps can be reduced by tensile strain [22]. (c) Responsivity spectrum for strained Ge-on-Si photodetector compared to plotted theoretical data for unstrained material [23].

Ge has a direct band gap of 0.80 eV, which is only 136 meV above its dominant indirect band gap [Figure 5(a)]. The presence of biaxial tensile stress in Ge causes the valence subbands to split, at which point the top of the valence band effectively comprises the light hole band [Figure 5(b)]. As the light hole band energy increases, both the direct and indirect gaps shrink, with the direct gap shrinking faster. This causes the Ge to transition from an indirect gap material towards a direct gap material with the development of tensile strain. The ability to induce an extended absorption coefficient in Ge over this range offers greater sensitivity for sensor detection of wavelengths exceeding 1550 nm [Figure 5(c)] [23].

In order to determine the composition, origin, and density of defects arising in device layers, bright-field scanning transmission electron microscope (STEM) images were acquired at atomic resolutions and analyzed. The processed high magnification (5000kx) STEM image featured in Figure 6 shows the atomic structure of the Ge-Si substrate interface. The upper portion of the image depicts Ge composition and the lower part Si, where a conglomerate mixture of materials exists at and around the layer junction.

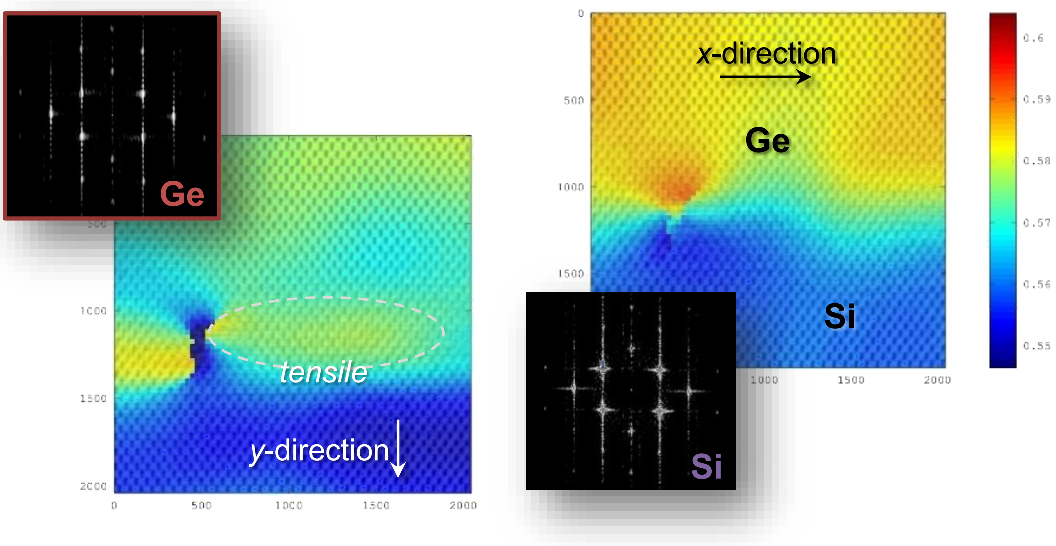

Figure 6. Plots of 2D spatial lattice variation for STEM atomic scale image, along with Ge and Si lattice diffraction patterns.

Due to the lattice mismatch between the Si and Ge, regions of strain will arise near the layer interface. The spatially-averaged magnitudes of the localized lattice constants computed in the *x*- and *y*-axis directions as functions of position over the image were processed using a 2D FFT-based algorithm to create color mappings providing information about the material composition and localized tensile strain in Si/Ge layer structures. [We used the TEM Lattice Calculator (Version 2.0.2; Teherani, 2014) for modeling the localized lattice constant variations.] Differences in lattice constant in the *x*-direction were utilized to distinguish the Ge (4.2% greater lattice constant) from Si, and also provide insight into the nature and configuration of material coalescence at the junction. Certain fluctuations in lattice constant in the *y*-direction verified the presence of tensile strain, such as that indicated in the figure localized in close proximity to the Si-Ge interface.

3.2 Minimizing Dark Current

Stranski-Krastanov growth of Ge on Si for film thicknesses below a critical thickness results in the formation of a 2D wetting layer, beyond which a transition to three-dimensional (3D) islanding growth mode occurs to relieve built-in strain in the Ge layers [24]. Defects and threading dislocations arising during Stranski-Krastanov growth, such as those found in the intrinsic layer of the *pin* detector device in Figure 7, typically form recombination centers [25]. At room temperature, leakage or dark current in *pin* photodetectors is mainly due to generation current passing through such traps. Higher levels of dark current result in increased power consumption that reduces detector performance, and shot noise associated with this leakage current can also lower NIR sensitivity [6,26].

Since dark current can be relatively high in SiGe photodetectors operating at room temperature, it is crucial when designing such devices to reduce it to acceptable levels generally considered to be 1 μA or less, above which the transimpedance amplifier noise may be exceeded and the SNR reduced [2,27]. Thermionic emission limits the dark current density in SiGe photodetectors to above ~10 μA/cm^2 at room temperature, which is around two orders of magnitude higher than that of standard InGaAs-based photodetectors [13].

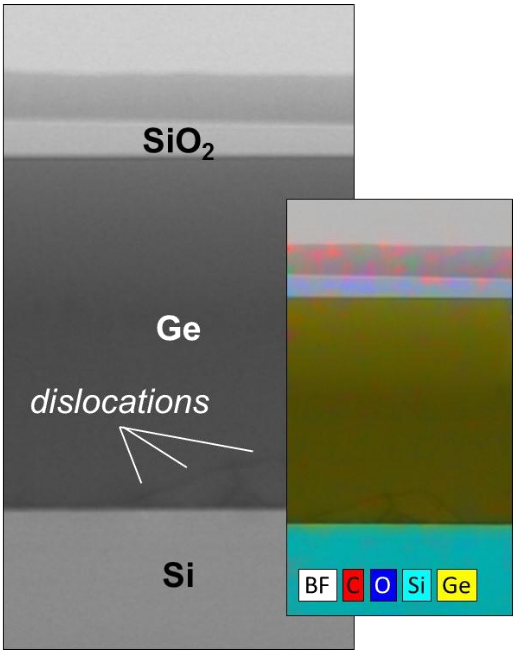

Figure 7. Cross-sectional STEM image, obtained in conjunction with energy-dispersive X-ray spectroscopy (EDS) mappings providing color mapping of materials. This detector sample comprising Ge layer grown on Si exhibits misfit dislocations near Si-Ge layer junction.

Various design approaches have been proposed and implemented to limit the dark current in SiGe detectors, including improving surface passivation and utilizing buried junctions [28]. Dark current generally scales with device area, so reducing the overall dimensions of SiGe detector devices is one means of limiting dark current (though not necessarily dark current density) for a given photodetector design. The splitting of the valence bands in Ge due to the presence of tensile strain also lowers the density of states for holes, leading to reduction of intrinsic carrier density that can likewise limit the dark current at reverse biases [29].

4.0 GROWTH AND FABRICATION OF GE PHOTODETECTORS

4.1 Two-step Growth Process Overview

Epitaxial growth of Ge using gas precursors has been utilized over the past three decades [13]. An early method for growing Ge on Si with reduced threading dislocation density involved using graded SiGe buffer layers, but this technique necessitated films at least 6 µm thick, making it prohibitive for many applications [30]. A more recent and useful method to deposit Ge layers to form functional *pin* detector devices involves a two-step growth process in which the growth temperature is ramped up between the growth steps [25,31]. While growth of Ge on silicon-on-insulator (SOI) surfaces has been thus demonstrated, this method is likewise applied to epitaxial deposition of Ge on pure Si substrates [14].

For development of the normal-incidence *pin* Ge photodetectors, deposition of Ge was accomplished through such a two-step growth process involving initial low temperature epitaxial deposition to form a thin strain-relaxed seed layer, and successive high temperature growth to deposit a thicker absorbing film [6]. This growth method was designed to produce high quality Ge films with limited threading dislocations arising from the lattice mismatch between the Si and Ge [32]. A 300 mm reduced-pressure chemical vapor deposition (RPCVD) system was employed that provided high control of the layer thicknesses. Germane was utilized as the precursor and hydrogen as the carrier gas, with reactor pressures in the 5-100 mTorr range. Figure 8 depicts early growth of a Ge layer on Si.

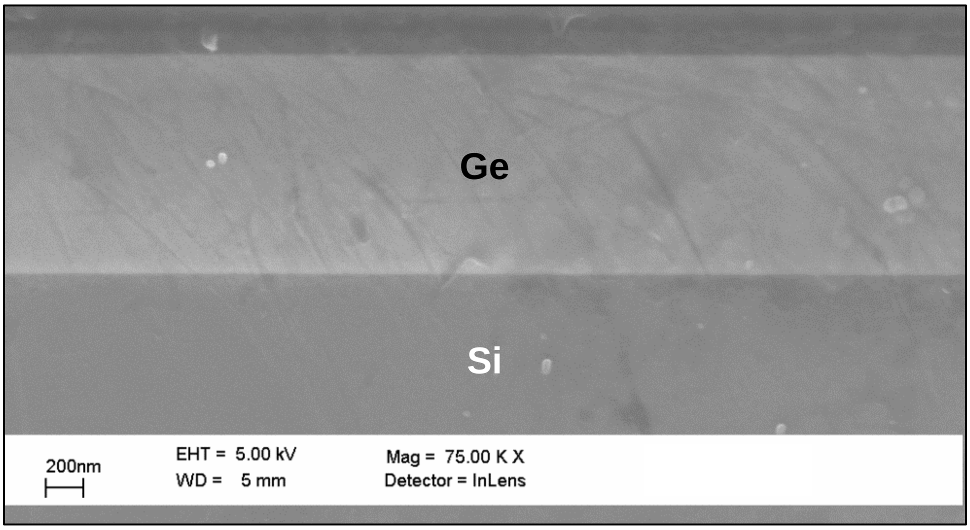

Figure 8. Scanning electron microscopy (SEM) image showing epitaxial deposition of Ge layer on Si substrate.

4.2 Low Temperature Growth

The first low temperature (325-425°C) growth step involved fully planar homoepitaxial deposition of a thin ~100 nm Ge p^+ (boron) doped seed/buffer layer on 300 mm <001> oriented Si wafers (resistivity: 9-18 Ω·cm). This process was critical in governing the film crystalline quality and surface morphology (i.e., reducing Stranski-Krastanov islanding and associated surface roughness), enhancing the migration of threading dislocations to limit their proliferation, and facilitating the final strain state in the Ge films [24]. Over this range of growth temperatures, the low surface diffusivity of Ge kinetically suppresses undesired 3D islanding that can otherwise result from strain release to promote planar growth [13]. By contrast, seed layer deposition at temperatures below 320°C commonly leads to crystallographic defect formation, while using growth temperatures significantly above this range can result in surface roughening due to increased surface mobility in the Ge [21].

In situ p^+ doping of this layer with boron was performed to enhance the seed growth rate, which was found to scale linearly with doping concentration, as well as lower the Ge/Si interfacial oxygen level [33]. Increasing the seed layer doping level to up to at least 10^{19} cm^{-3} has been determined to lower series resistance under forward bias and reduce the dark current under reverse bias [34].

4.3 High Temperature Growth

In the subsequent high temperature step of the growth process, a layer of intrinsic Ge serving as the absorption region was grown at ~550°C above the relaxed buffer/seed layer. This approximate temperature was chosen to ensure satisfactory deposition rates that enable smooth, high crystal quality tensile strained Ge films [14]. The intrinsic Ge epitaxial film topologies when grown on seed layers ~100 nm thick we found to be very smooth and have relatively few defects, in contrast to Ge intrinsic layers grown on 22 nm thick seed layers which exhibited surface defect density of approximately 2000/cm^2 [35]. Generally, as the *i*-Ge layer is made thicker, the transit time increases which reduces the device bandwidth, but the responsivity rises due to higher absorption and reduced junction capacitance [36]. However, topological and defect density concerns limit the *i*-layer thickness for practical *pin* devices to below 2 µm [1]. The doping level of the intrinsic Ge layer in our devices was ~10^{15} cm^{-3}, 4-5 orders of magnitude lower than those of the highly-doped n^+ and p^+ layers in the *pin* detectors [37].

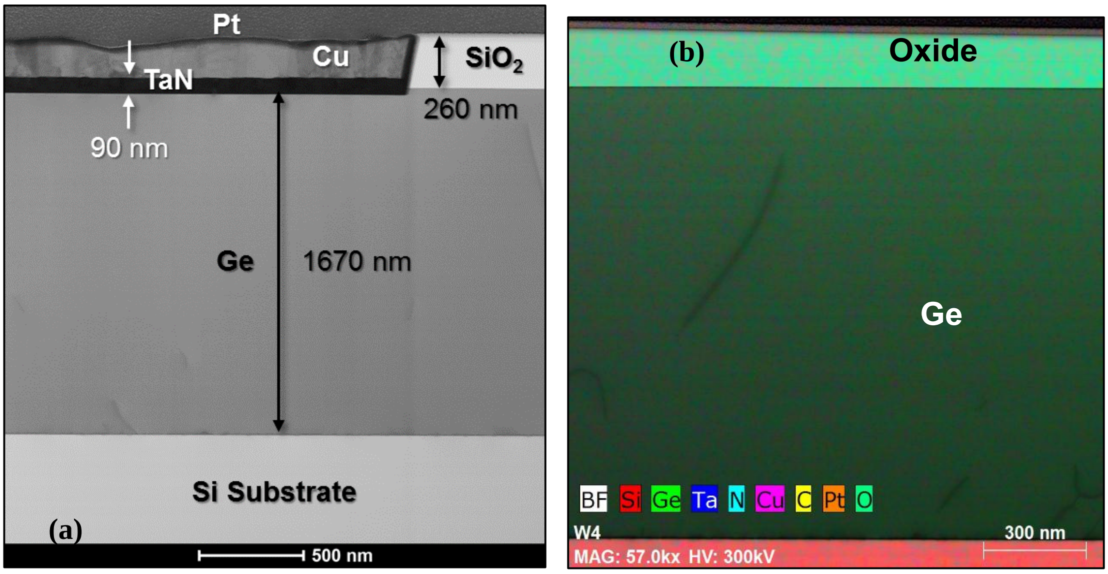

Figure 9. (a) Cross-sectional STEM image of detector device layers showing portion of Cu contact [38]. (b) Comparable STEM image of a different detector device, providing material compositions (identified by color) and layer structure down to Si substrate [39,40].

Following the high temperature growth steps, *in situ* annealing at 600°C was performed for 30 s. The cyclic annealing process was aimed to reduce the threading dislocation density by transforming sessile threading dislocations to glissile ones (which effectively annihilate the dislocations due to thermal stress glide), and enhance the strain in the *i*-Ge layer [22,41,42]. Figure 9(a) and 9(b) show cross-sectional on-contact and off-contact STEM analyses, respectively, of the layer structure of *pin* detector devices [38-40].

4.4 Subsequent Fabrication Steps

After completion of the two-step growth process, n^+ regions were formed by ion implantation of phosphorus. (This replaced n^+ polysilicon layers utilized for earlier detector devices.) Four different n^+ doping levels were implemented through the implantation process, ranging from 5×10^{18} cm^{-3} to 10^{20} cm^{-3}. A layer of oxide (SiO_2) was then deposited over the detector surfaces. This oxide was intended to isolate states at the layer interface from the signal carrying layers to prevent communication between the interface states and the intrinsic Ge layer, as well as further reduce traps contributing to leakage current [1,13].

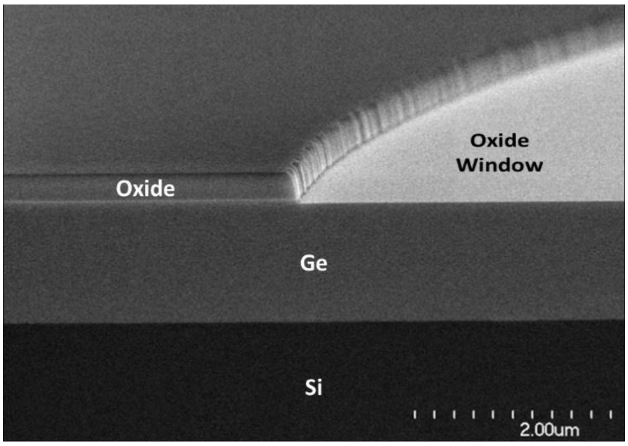

Figure 10. SEM image showing window in oxide for top Cu contact on detector device [39].

Windows in the oxide layer, like the one partially shown in Figure 10, were opened to facilitate the deposition of low resistance copper top contacts [39]. Reactive ion etching (RIE) was utilized for this step to minimize faceting and enhance trench filling. Before formation of the Cu contacts, TaN barrier layers were deposited above the n^+ Ge to limit diffusion of the Cu and thus improve the electrical characteristics of the detector devices. TaN was determined to be an optimal material for this purpose due to its inherent thermodynamic stability with respect to copper and relatively low electrical resistance. The Cu contacts were then deposited in the oxide windows above the TaN, followed by chemical-mechanical polishing (CMP) to planarize the wafer/device surfaces. Figure 11 presents a flowchart and pictorial overview of the wafer device fabrication process [43].

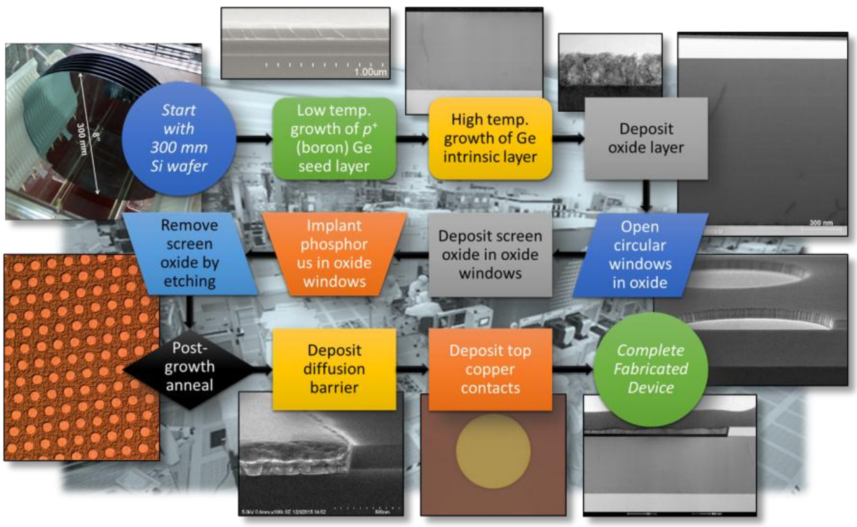

Figure 11. Sequential flowchart summarizing photodetector device fabrication process [43].

5.0 DETECTOR PERFORMANCE

5.1 Testing Configuration

Current-voltage (I-V) measurements of the dark current and photocurrent behavior of room temperature operation SiGe *pin* photodetectors representing individual pixels in a NIR FPA were acquired. The testing was performed using a laboratory probe station setup with source-measurement unit (Keithley 2400 Source Meter). A broadband fiber-coupled tungsten-halogen vis-NIR source (Thorlabs SLS201) provided relatively high intensity over the approximate 1000-1700 nm wavelength range of interest. The optical power output from the light source delivered to the detectors by a single-mode, 400 µm diameter optical fiber was 10 mW, corresponding to an optical power density of 8 W/cm^2. Dark current and photoresponse characteristics were measured for devices utilizing both front-side illuminated and backside illuminated configurations as functions of applied bias and time.

5.2 Backside Illumination

In the backside illuminated test configuration, light was incident through the Si substrate of the device, and the current measured over a range of applied forward and reverse biases. The maximum photocurrent under backside illuminated conditions was found to occur when the fiber-delivered NIR radiation was angularly incident as schematically depicted in Figure 12(a). Detector devices under backside illuminated conditions, plotted in Figure 12(b), demonstrated dark current and photocurrent of 2.5 μA and 112 μA, respectively, corresponding to over 40X enhancement after NIR illumination. The zero-bias photocurrent was marginally lower than that measured at -1 V, and from -4 V to 0 V bias it decreased by only 20%. This behavior is attributed to high carrier collection efficiency (carriers being quickly collected before recombining at defect centers) resulting from a significant built-in electric field in the depletion region [44]. The shunt resistance, used for the determination of zero-bias noise current, was ~1.5 MΩ.

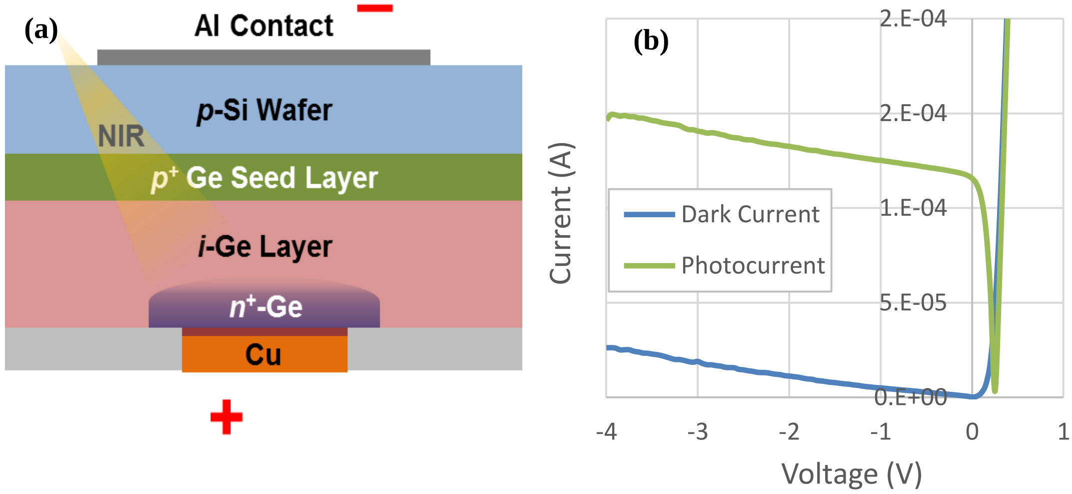

Figure 12. (a) Backside illuminated detector testing configuration (device dimensions not to scale); and (b) I-V characteristics of detector device.

5.3 Front-side Illumination

I-V photoresponse measurements for the *pin* detectors were likewise acquired using more conventional front-side illumination. The dark current and photocurrent I-V curves for a detector with n^+ region phosphorus doping level of 5×10^{19} cm^{-3} are plotted in Figure 13(a), and the time-dependent photoresponse at 0 V bias plotted in Figure 13(b) [43]. The measured dark current at -1 V was approximately 0.6 nA; it remained fairly constant even as the magnitude of the reverse bias was increased, rising slightly to 0.7 nA and 1.1 nA at -2 V and -4 V, respectively. The photocurrent at -1 V for this device was 168 nA, greater than the dark current by a factor of over 250. The zero-bias photocurrent (138 nA) was above 80% the value of that measured at -1 V, and the detectors demonstrated short rise-fall times in relation to the time intervals utilized.

This front-side illuminated detector device likewise exhibited decent diode rectifying behavior, with a forward to reverse current ratio of ~5×10^4 at ±1 V. The average shunt resistance for detectors was on the order of 100 MΩ, reflective of the comparatively low leakage currents. Compared to the backside illuminated case, for front-side illumination the dark current was lower and the enhancement in photocurrent greater, which is attributed in part to a higher percentage of photons from the source reaching and being absorbed in the intrinsic regions of the detectors.

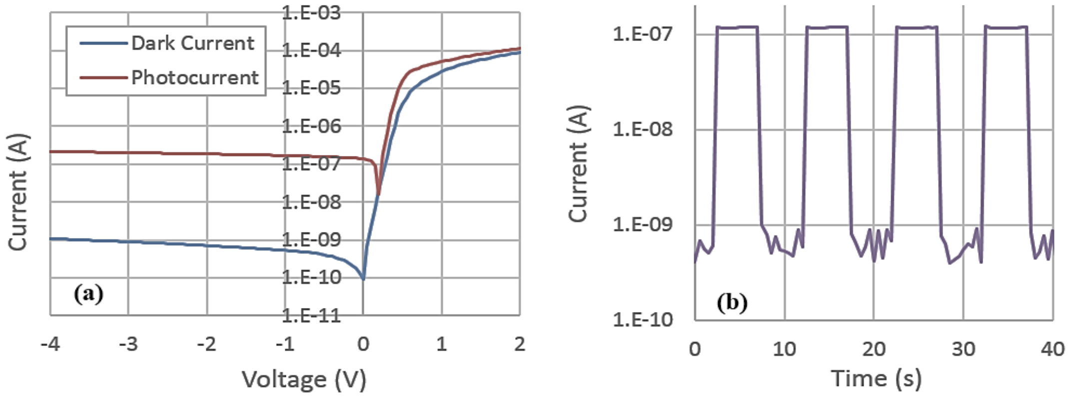

Figure 13. (a) Dark current and photocurrent I-V curves for front-side illuminated detector (dark current curve partially extrapolated to adjust for measurement uncertainty). (b) Time-dependent photoresponse at zero-bias measured while modulating incident NIR radiation on and off [43].

I-V photoresponse front-side illuminated measurements were likewise acquired for devices representing four different doping concentrations ranging from 5×10^{18} cm^{-3} to 10^{20} cm^{-3}. The corresponding device I-V results based on *n*-doping level are plotted in Figure 14. It can be seen that the detector device with the highest doping concentration (~10^{20} cm^{-3}) had the lowest measured dark current, and the device with next highest *n*-doping level of 5×10^{19} cm^{-3} exhibited the greatest photocurrent with a dark current to photocurrent ratio at -1 V approaching 300. Table 1 presents the measured I-V data and calculated results obtained from the fabricated photodetectors characterized by the different n^+ region doping concentrations [43].

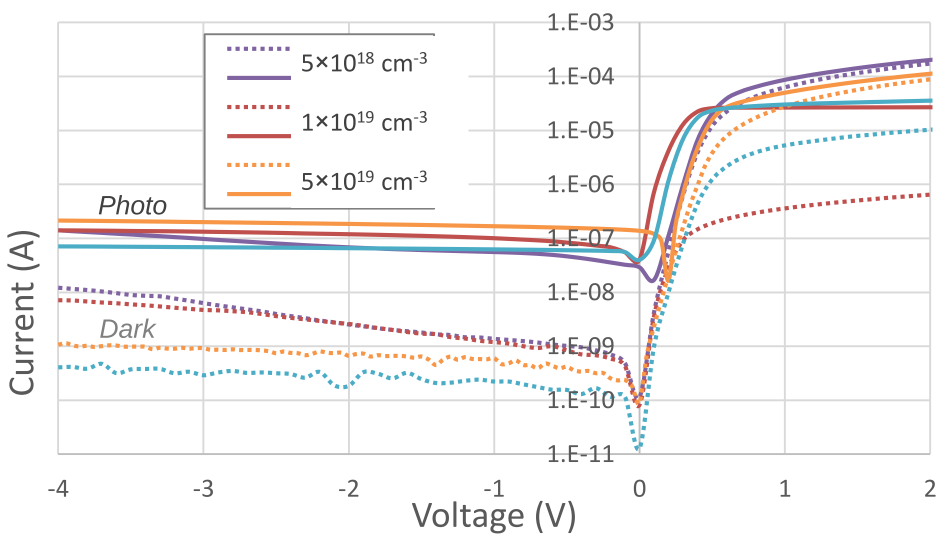

Figure 14. Dark current and photocurrent I-V curves for detectors having to various *n*-region doping concentrations.

Table 1. Comparison of I-V results for four SiGe detectors having different n^+ region (P) doping concentrations [43].

n^+ *Region Doping Level*	5×10^{18} cm^{-3}	1×10^{19} cm^{-3}	5×10^{19} cm^{-3}	1×10^{20} cm^{-3}
Dark Current @ -1 V (nA)	1.38	1.20	0.57	0.23
Photocurrent @ -1 V (nA)	56	100	168	63
I_D : I_P Ratio @ -1 V	41	84	288	282
Photocurrent @ 0 V (nA)	29	40	138	40
I_F : I_R (Dark) Ratio @ ±1 V	4.6×10^4	3.0×10^2	4.8×10^4	2.4×10^4

6.0 SUMMARY AND CONCLUSIONS

SiGe provides an alternative material system enabling uncooled, lower cost photodetectors operating at NIR wavelengths using CMOS-based fabrication processes. Ge *pin* photodetectors have been developed on 300 mm Si substrates utilizing a two-step low/high temperature fabrication process for incorporation of tensile stain and reduction of dark current. These fabricated detectors, designed to function as elements in an NIR imager focal plane array (FPA), demonstrated up to three orders of magnitude enhancement in current under NIR illumination compared to the dark current. In addition, under front-side illumination the detectors exhibited measured dark currents well under the 1 μA limit at -1 V bias.

From an applications standpoint, low power operation and performance (typically involving bias voltages below 1.5 V) is desirable in IR photodetectors, and by the same token in IR-FPAs comprising arrays of detector elements [45]. Consequently, there has been increasing research interest in detectors capable of providing sufficient performance (e.g., responsivity) at low applied bias, and even at zero-bias. In this regard, a potentially useful feature of these *pin* detectors is sustained photoresponse at zero-bias, enabled by a built-in electric field in the intrinsic Ge region. Typically, the photocurrent at 0 V bias was comparable to that measured at -1 V, and only marginally lower than that at -4 V bias. These performance qualities, coupled with low dark currents demonstrated by the *pin* devices, hold promise towards practically benefitting low power sensor and IR-FPA applications.

ACKNOWLEDGEMENTS

The authors thank Dr. Jay Lewis of DARPA / MTO for technical discussions and guidance, as well as Ms. Susan Nicholas and Mr. Oscar Cerna of DARPA for their on-going support. This research was developed with funding from the Defense Advanced

Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

REFERENCES

[1] N. K. Dhar, R. Dat, and A. K. Sood. "Advances in infrared array detector technology." Chapter in *Optoelectronics: Advanced Materials and Devices*, edited by S. L. Pyshkin and J. M. Ballato, Intech Publications, 2015.

[2] DiLello, Nicole Ann. "Fabrication and characterization of germanium-on-silicon photodiodes." Ph.D. dissertation, Massachusetts Institute of Technology, 2012.

[3] A. K. Sood, R. A. Richwine, Y. R. Puri, N. DiLello, J. L. Hoyt, T. I. Akinwande, N. Dhar, S. Horn, R. S. Balcerak, and T. G. Bramhall, "Development of low dark current SiGe-detector arrays for visible-NIR imaging sensor," *Proc. SPIE* 7660, 76600L (2010).

[4] K. W. Ang and G. Q. Lo Patrick, "Avalanche photodiodes: Si charge avalanche enhances APD sensitivity beyond 100 GHz," *Laser Focus World* 46.8 (2010).

[5] J. Wang and S. Lee, "Ge-photodetectors for Si-based optoelectronic integration," *Sensors* 11, 696-718 (2011).

[6] A. K. Sood, J. W. Zeller, R. A. Richwine, Y. R. Puri, H. Efstathiadis, P. Haldar, N. K. Dhar, and D. L. Polla. "SiGe based visible-NIR photodetector technology for optoelectronic applications." Chapter in *Advances in Optical Fiber Technology: Fundamental Optical Phenomena and Applications*, edited by Moh Yasin, Hamzah Arof, and Sulaiman Wadi Harun, Intech Publications, 2015.

[7] A. Rogalski, "Progress in focal plane array technologies," *Prog. Quant. Electron.* 36, 342-473 (2012).

[8] A. Rogalski, "Infrared detectors: status and trends," *Prog. Quant. Electron*. 27, 59-210 (2003).

[9] V. A. Vu, D. E. Ioannou, R. Kamocsai, S. L. Hyland, A. Pomerene, and D. Carothers, "PIN germanium photodetector fabrication issues and manufacturability," *IEEE Trans. Semi. Manufact.* 23, 411-418 (2010).

[10] A. Rogalski, "Infrared detectors: an overview," *Infrared Phys. & Tech.* 43.3, 187-210 (2002).

[11] Rajagopal, K. *Textbook of Engineering Physics*. PHI Learning Pvt. Ltd., 2012.

[12] M. Jutzi, M. Berroth, G. Wohl, M. Oehme, and E. Kasper, "Ge-on-Si vertical

incidence photodiodes with 39-GHz bandwidth," *IEEE Photon. Tech. Lett*. 17, 1510-1512 (2005).

[13] J. Michel, J. Liu, and J. C. Kimerling, "High-performance Ge-on-Si photodetectors," *Nature Photon*. 4, 527-534 (2010).

[14] J. Liu, D. D. Cannon, K. Wada, Y. Ishikawa, S. Jongthammanurak, D. T. Danielson, J. Michel, and L. C. Kimerling, "Silicidation-induced band gap shrinkage in Ge epitaxial films on Si," *Appl. Phys. Lett.* 84, 660-662 (2004).

[15] E. Agrell, M. Karlsson, A. R. Chraplyvy, D. J. Richardson, P. M. Krummrich, P. Winzer, K. Roberts, J. K. Fischer, S. J. Savory, B. J. Eggleton, and M. Secondini, "Roadmap of optical communications," *J. Optics* 18, 063002 (2016).

[16] *Image credit*: IBM (http://researcher.ibm.com).

[17] B. Jalali, M. Paniccia, and G. Reed, "Silicon photonics," *IEEE Microwave Mag*. 7, 58-68 (2006).

[18] P. Chaisakul, D. Marris-Morini, J. Frigerio, D. Chrastina, M. S. Rouifed, S. Cecchi, P. Crozat, G. Isella, and L. Vivien, "Integrated germanium optical interconnects on silicon substrates," *Nature Photon.* 8, 482-488 (2014).

[19] D. B. Law, E. M. Carapezza, C. J. Csanadi, G. D. Edwards, T. M. Hintz, and R. M. Tong, "Multi-spectral signature analysis measurements of selected sniper rifles and small arms," *Proc. SPIE* 2938, 288-298 (1997).

[20] C. Callan, J. Goodman, M. Cornwall, N. Fortson, R. Henderson, J. Katz, D. Long, R. Muller, M. Ruderman, and J. Vesecky, "Sensors to support the soldier." No. JSR-04-210. Mitre Corp., McLean, VA, 2005.

[21] Olubuyide, O. Oluwagbemiga. "Low pressure epitaxial growth, fabrication and characterization of Ge-on-Si photodiodes." Ph.D. dissertation, Massachusetts Institute of Technology, 2007.

[22] J. Liu, R. Camacho-Aguilera, J. T. Bessette, X. Sun, X. Wang, Y. Cai, L. C. Kimerling, and J. F. Michel, "Ge-on-Si optoelectronics," *Thin Sol. Films* 520, 3354-3360 (2012).

[23] Y. Ishikawa and K. Wada, "Germanium for silicon photonics," *Thin Sol. Films* 518, S83-S87 (2010).

[24] T. K. P. Luong, M. T. Dau, M. A. Zrir, M. Stoffel, V. Le Thanh, M. Petit, A. Ghrib, M. El Kurdi, P. Boucaud, H. Rinnert, and J. Murota, "Control of tensile strain and interdiffusion in Ge/Si(001) epilayers grown by molecular-beam epitaxy," *J. Appl. Phys.* 114, 083504 (2013).

[25] Z. Huang, J. Oh, S. K. Banerjee, and J. C. Campbell, "Effectiveness of SiGe buffer layers in reducing dark currents of Ge-on-Si photodetectors," *IEEE J.*

Quantum. Electron. 43, 238-242 (2007).

[26] A. K. Sood, R. A. Richwine, Y. R. Puri, O. O. Olubuyide, N. DiLello, J. L. Hoyt, T. I. Akinwande, R. S. Balcerak, S. Horn, T. G. Bramhall, and D. J. Radack, "Design considerations for SiGe-based near-infrared imaging sensor," *Proc. SPIE* 6940, 69400M (2008).

[27] D. Ahn, C. Hong, J. Liu, W. Giziewicz, M. Beals, L. Kimerling, J. Michel, J. Chen, and F. X. Kartner, "High performance, waveguide integrated Ge photodetectors," *Opt. Express* 15, 3916-3921 (2007).

[28] V. T. Bublik, S. S. Gorelik, A. A. Zaitsev, and A. Y. Polyakov, "Calculation on the binding energy of Ge-Si solid solution," *Phys. Status Solidi* 65, 79-84 (1974).

[29] Y. Ishikawa, K. Wada, D. D. Cannon, J. Liu, H. C. Luan, and L. C. Kimerling, "Strain-induced band gap shrinkage in Ge grown on Si substrate," *Appl. Phys. Lett*. 82, 2044-2046 (2003).

[30] S. Luryi, A. Kastalsky, and J. Bean, "New infrared detector on a silicon chip," *IEEE Trans. Electron. Dev.* ED-31, 1135-1139 (1984).

[31] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, "Metal-semiconductor-metal near-infrared light detector based on epitaxial Ge/Si," *Appl. Phys. Lett.* 72, 3175-3178 (1998).

[32] H. C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, "High-quality Ge epilayers on Si with low threading-dislocation densities," *Appl. Phys. Lett*. 75, 2909-2911 (1999).

[33] O. Olubuyide, D. Danielson, L. Kimerling, and J. Hoyt, "Impact of seed layer on material quality of epitaxial germanium on silicon deposited by low pressure chemical vapor deposition," *Thin Sol. Films* 508, 14-19 (2006).

[34] A. K. Sood, R. A. Richwine, Y. R. Puri, N. DiLello, J. L. Hoyt, N. Dhar, R. S. Balcerak, and T. G. Bramhall, "Development of SiGe arrays for visible-near IR imaging applications," *Proc. SPIE* 7780, 77800F (2010).

[35] J. W. Zeller, H. Efstathiadis, G. Bhowmik, P. Haldar, N. K. Dhar, J. Lewis, P. Wijewarnasuriya, Y. R. Puri, and A. K. Sood, "Development of Ge PIN photodetectors on 300 mm Si wafers for near-infrared sensing," *Int. J. Engr. Res. Tech.* 8, 23-33 (2015).

[36] J. Liu, J. Michel, W. Giziewicz, D. Pan, K. Wada, D. D. Cannon, S. Jongthammanurak, D. T. Danielson, L. C. Kimerling, J. Chen, F. O. Ilday, F. X. Kartner, and J. Yasaitis, "High-performance, tensile-strained Ge p-i-n photodetectors on a Si platform," *Appl. Phys. Lett*. 87, 103501 (2005).

[37] M. Oehme, J. Werner, O. Kirfel, and E. Kasper, "MBE growth of SiGe with high Ge content for optical applications," *Appl. Surf. Sci*. 254, 6238-6241 (2008).

[38] J. W. Zeller, C. Rouse, H. Efstathiadis, P. Haldar, N. K. Dhar, J. S. Lewis, P. Wijewarnasuriya, Y. R. Puri, and A. K. Sood, "Design and development of wafer-level near-infrared micro-camera," *Proc. SPIE* 9609, 96090O (2015).

[39] J. W. Zeller, C. Rouse, H. Efstathiadis, P. Haldar, J. S. Lewis, N. K. Dhar, P. Wijewarnasuriya, Y. R. Puri, and A. K. Sood, "Development of silicon-germanium visible-near infrared arrays," *Proc. SPIE* 9854, 985408 (2016).

[40] J. W. Zeller, A. K. Sood, C. Rouse, H. Efstathiadis, P. Haldar, N. K. Dhar, and P. Wijewarnasuriya, "Development of low dark current SiGe near-infrared PIN photodetectors on 300 mm silicon wafers," *Proc. SPIE* 9974, 997401 (2016).

[41] H. C. Luan and L. C. Kimerling. "Cyclic thermal anneal for dislocation reduction," U.S. Patent No. 6635110, 21 Oct. 2003.

[42] L. Colace, M. Balbi, G. Masini, G. Assanto, H. C. Luan, and L. C. Kimerling, "Ge on Si *p-i-n* photodiodes operating at 10 Gbit/s," *Appl. Phys. Lett*. 88, 101111 (2006).

[43] J. W. Zeller, C. Rouse, H. Efstathiadis, P. Haldar, J. S. Lewis, N. K. Dhar, P. Wijewarnasuriya, Y. R. Puri, and A. K. Sood, "Development of low dark current SiGe near-infrared PIN photodetectors on 300 mm silicon wafers," *Opt. Photon. J.* 6, 61-68 (2016)

[44] J. Liu, "Monolithically integrated Ge-on-Si active photonics," *Photonics* 1, 162-197 (2014).

[45] L. Pavesi and D. Lockwood. *Silicon Photonics, Topics in Applied Physics, Vol. 94*. Springer-Verlag, Berlin, Germany, 2004.