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Low-Power Near-Explicit 5:2 Compressor for Superior Performance Multipliers

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Abstract

Arithmetic modules are crucial components in numerous superior performance processors and in Digital Phase Locked Loop circuits. In many complex executions, multipliers have been demanding, and imperative elements in governing the complete circuit efficacy when power estimation and speed are to be examined. Compressors are the substantial supplements of the multiplier circuit, which is convenient in the compression of partial products and in increasing the speed of the complete circuit. This article demonstrates various structures of 5:2 compressors by arranging them as, exclusive 3:2 compressors, XOR-XNOR and multiplexers, employing 4:2 and 3:2 compressors one each, and is simulated to estimate their achievement in power dissipation and speed at different supply voltages. Out of all the above circuits, the proposed one is based on approximate 5:2 compressor which is implemented employing only two 3:2 compressors instead of three 3:2 and simulations are carried out in 45nm technology node using cadence spectre simulator. Experimental results show that the proposed 5:2 compressor with two 3:2 modules scales down power and escalates speed.

Keywords: Approximate, CMOS, Compressors, Multipliers, XOR-XNOR

I. INTRODUCTION

Digitization has remarkable effect in electronics industry as the growth is steadily extending from mainframe computers to laptops [1]. Filtering operation is one of the vital activities in digital signal processing units and in most of the applications employing arithmetic logic units and floating point units, multipliers and adders are the demanding peripherals in determining the performance of the complete circuit in terms of power consumption and computation speed. Multiplication operation is basically a three step process consisting of partial product generation, partial product reduction and final addition of all the partial products, out of which the second step consumes more silicon area, power and delay. Various approaches like modified booth encoding technique [2], ripple carry adders and carry save adders were used to cut down partial product generation and to reduce the circuitry for partial product reduction. The above specified designs were eliminated with the initiation of compressor circuits [3] where the carry propagation is confined.

A compressor is a logic circuit that takes all the bits of same significance and generates a Sum bit and several Carry bits as the output. The primary variation between compressor and adder is that, the former one adds multiple bits of same significance and the latter adds two operands of multiple numbers of different significant. Example of a 5:2 compressor operation is disclosed in Fig. 1 below.

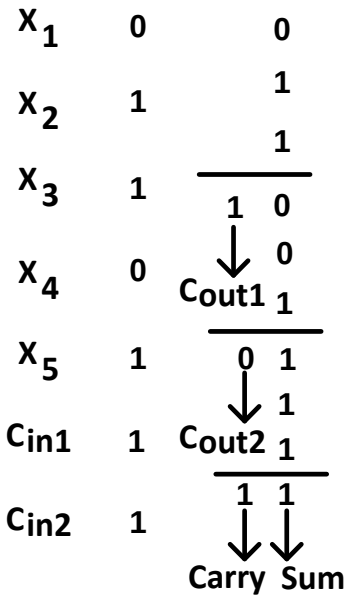

Fig 1: 5:2 Compressor Example

This 5:2 compressor addition is performed with three Full Adders. The first Full Adder (FA1) adds X_1, X_2 and X_3 which gives Carry1 and Sum1, where the Carry1 is taken as C_{out1}. The second Full Adder (FA2) adds Sum1, X_4 and X_5 bits to give C_{out2}

and Sum2. To this Sum2 of FA2, C_{in1} and C_{in2} are added to give Carry and Sum of 5:2 compressor. With the expanding need for low power structures, inexact circuits [4-6] are acquiring rising concentration with an accord in correctness of output for energy/power, delay and area. The increasing demand for these inexact circuits is due to the fact that the three parameters are substantially improving. Heretofore, approximations to the original circuit were being done by scaling the supply voltage vdd from which error can be tolerated but had convincing drawbacks that the hardware of the overall circuit is increasing in the form of level shifters for supply voltage fine tuning.

To prevent these disadvantages, equivalent architecture level approaches with zero hardware were proposed namely probabilistic pruning [7] and probabilistic logic minimization [8].The former one deletes the extra non-significant hardware during the design of a circuit and in the latter, bits are flipped in the minterms of Boolean functions through which the three dimensions energy/power, delay and area improves with a little adjustment in accuracy. Inexact Multipliers were designed by employing approximate compressors in [9-12]. Paper [13] discloses decimal compressors to handle decimal multipliers. The principal objective of the arrangement is to concentrate on compressors which are one of the fundamental elements of multiplier circuits that are being extensively used in high speed systems. A new 5:2 compressor with 58 transistors is discussed in [14]. In this paper, new design approaches have been investigated for low power 5-2 compressor circuits that acquire adequate drivability at ultra low voltages based on the progressive CMOS process technology.

The subsequent sections of this paper are arranged as follows. In Section II, existing structures of 5:2 compressors are articulated. Section III presents proposed structure of 5:2 compressor and multipliers utilizing these compressors in terms of approximate 4:2 compressor and exact 3:2 compressor. Sections IV and V gives experimental results in terms of power, delay and conclusions respectively.

II. EXISTING 5:2 COMPRESSOR MODEL

Compressors are essential sections used for acquiring partial products during the multiplication process. The primary concept in any compressor is that the number of operands present gets added column wise leaving a sum and carry, i.e. all the columns of partial product are added in parallel without relying on previous carry. The earliest compressor is the full adder circuit and is generally indicated as 3:2 compressors. The next advanced compressor is the 4:2 compressors [15] which shrink four partial products into two and hence high compression ratio is obtained when compared with 3:2. A tertiary compressor subsequent to 4:2 is the 5:2 compressor. The basic structure of it is shown in Fig. 2

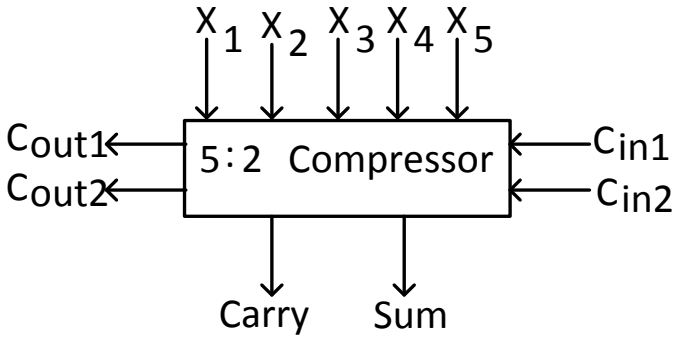

Fig 2: Basic 5:2 Compressor structure [17]

Out of the seven inputs, five are direct inputs X_1, X_2, X_3, X_4 and X_5 and two are carry inputs C_{in1}, C_{in2} from a previous stage. Similarly, there are four outputs of which two are carry-out bits (C_{out1}, C_{out2}) to the next stage and the other two are Sum and Carry bits. The conventional way of representing 5:2 is using three cascaded full adders as depicted in Fig. 3.

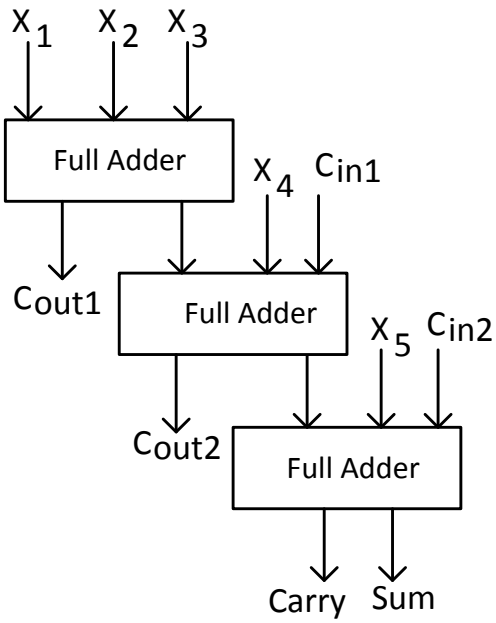

Fig. 3: 5:2 with Full Adders [17]

The operation of Fig.3 can be explained with respect to Fig. 1. The regular implementation of 5:2 is with XOR-XNOR blocks and the sum and carry expressions are given by the following equations [17].

$$\text{Sum} = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_5 \oplus C_{in1} \oplus C_{in2} \tag{1}$$

$$\text{Sum} = \left\{ \begin{array}{l} \left[\left(X_1 \oplus X_2 \right) X_3' + X_3 \left(X_1 \oplus X_2 \right)' \right] \oplus \\ \left[\left(X_4 \oplus X_5 \right)' C_{in1} + C_{in1}' \left(X_4 \oplus X_5 \right) \right] \end{array} \right\} C_{in2}' + C_{in2} \left\{ \begin{array}{l} \left[\left(X_1 \oplus X_2 \right) X_3' + X_3 \left(X_1 \oplus X_2 \right)' \right] \oplus \\ \left[\left(X_4 \oplus X_5 \right)' C_{in1} + C_{in1}' \left(X_4 \oplus X_5 \right) \right] \end{array} \right\}' \tag{2}$$

$$\text{Carry} = \left[\left(X_1 \oplus X_2 \oplus X_3 \right) \oplus \left(X_4 \oplus X_5 \oplus C_{in1} \right) \right] C_{in2} + \left(X_1 \oplus X_2 \oplus X_3 \right) \left[\left(X_1 \oplus X_2 \oplus X_3 \right) \oplus \left(X_4 \oplus X_5 \oplus C_{in1} \right) \right]' \tag{3}$$

$$C_{out1} = X_1 X_2 + X_2 X_3 + X_1 X_3$$
$$C_{out2} = \left(X_1 \oplus X_2 \oplus X_3 \oplus X_4 \right) C_{in1} + \left(X_1 \oplus X_2 \oplus X_3 \oplus X_4 \right)' X_4 \tag{4}$$

The block diagram of 5:2 compressor in terms of XOR-XNOR and MUX blocks with respect to the above equations are depicted in Fig. 4.

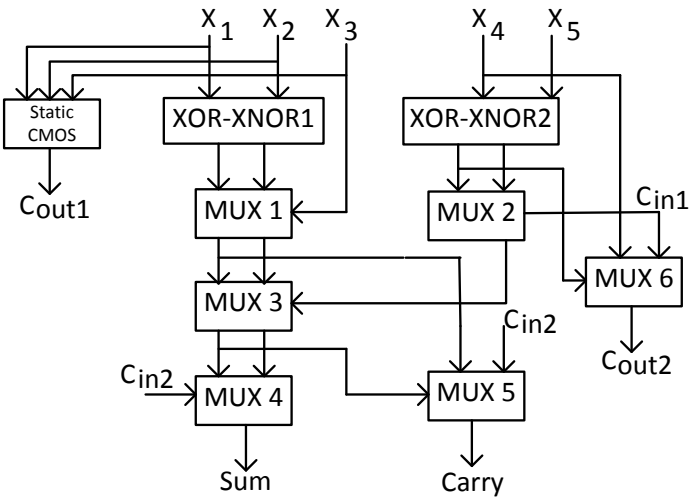

Fig 4: 5:2 in terms of XOR-XNOR and MUX [3]

The XOR-XNOR and MUX circuits with different number of transistors were used in the literature [17], but in this paper, pass transistor logic based 6T XOR-XNOR has been employed with transmission gate (TGL) and pass transistor logic (PTL) based two input multiplexers.

III. PROPOSED STRUCTURES

III.I. Proposed 5:2 Compressor

In this section, the proposed 5:2 compressor design with an imprecise 4:2 and an exact 3:2 compressor is presented. In the literature various 5:2 compressors with full adders, XOR-XNOR and MUX gates were designed. A 5:2 compressor can be implemented using an exact 4:2 and 3:2 compressors whose representation is displayed below in Fig. 5.

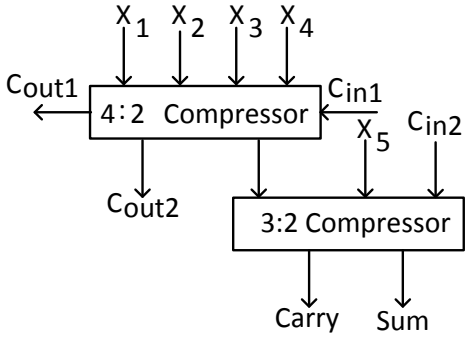

Fig 5: 5:2 with exact 4:2 and 3:2

The construction of the above figure is, X_1, X_2, X_3, X_4 and C_{in1} are used as inputs of 4:2 compressor, the SUM of it is one of the input and X_5,C_{in2} are other two inputs of 3:2 compressor, the outputs C_{out} , Carry of 4:2 acts as carry outputs C_{out1}, C_{out2} of 5:2 respectively and the Sum, Carry outputs of 3:2 are final outputs of 5:2.

In this paper, a 5:2 compressor has been approximated and designed with two 3:2 compressors which have five inputs X_1, X_2, X_3, X_4, X_5 and three outputs C_{out1}, Carry, Sum instead of seven inputs X_1, X_2, X_3, X_4, X_5, C_{in1}, C_{in2} and 4 outputs C_{out1}, C_{out2}, Carry, Sum. The proposed 5:2 compressor is implemented by approximating the 4:2 compressor and using exact 3:2 compressor which turn out to be a 4:2 compressor. Approximations are applied by considering truth table and Boolean equations of 4:2 compressor. The proposed approximate 4:2 compressor is designed by equating X_4, C_{in1}inputs since the lowest and highest order bits of both are same such that the Sum and Carry expressions of exact 4:2 compressor turns in to eq.(5) to eq.(12).

$$\text{Sum} = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in} \tag{5}$$

Equating X_4 and C_{in1}

$$\text{Sum} = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_4 \tag{6}$$

$$\text{Sum} = X_1 \oplus X_2 \oplus X_3 \tag{7}$$

As X_4 part of Sum expression is zero, i.e, if $X_4 = 0$,

$$\text{Carry} = X_4 \left(X_1 \oplus X_2 \oplus X_3 \oplus X_4 \right)' + C_{in} \left(X_1 \oplus X_2 \oplus X_3 \oplus X_4 \right) \tag{8}$$

$$\text{Carry} = 0 \tag{9}$$

There is no change in C_{out1} of 4:2 as there are no X_4 and C_{in1} terms in it. Thus, Sum, Carry and C_{out} expressions of approximate 4:2 compressor is given as follows.

$$\text{Sum} = X_1 \oplus X_2 \oplus X_3 \tag{10}$$

$$\text{Carry} = 0 \tag{11}$$

$$C_{out1} = X_1X_2 + X_2X_3 + X_1X_3 \tag{12}$$

No approximations are being done to 3:2 compressor as it has only three inputs and two outputs. With the approximations applied to exact 4:2 compressor, it has been reduced to 3:2 compressor. Therefore, the 5:2 compressor has altered to a 4:2 compressor. The 5:2 compressor with two 3:2 compressors is portrayed in Fig. 6.

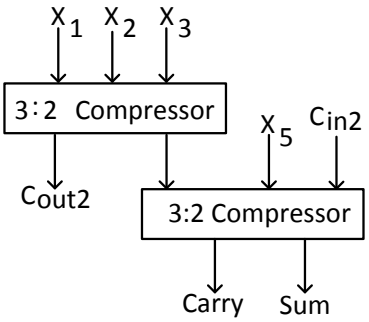

Fig 6: Proposed 5:2 Compressor

The two input multiplexers with Transmission gate logic (TGL) and pass transistor logic (PTL) employed in 5:2 compressors in all the above circuits are displayed in Fig.7.

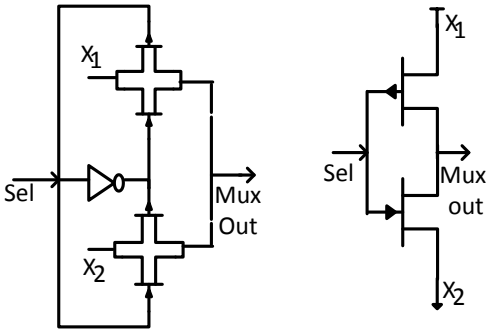

Fig 7: (a) TG MUX [3], (b) 2T MUX

The 3:2 compressors employed in approximate 5:2 compressor is displayed in Fig. 8.

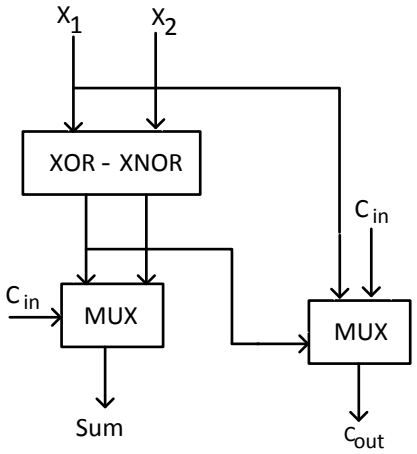

Fig 8: Approximate 4:2 compressor=3:2 compressor

III.II Dadda Multipliers using 5:2 Compressors

This part of section III describes eight Dadda multipliers where in the first six are the existing multipliers as they employs different existing 5:2 compressors and the last two are the proposed multipliers which includes proposed 5:2 compressors. All the eight multipliers implemented are utilizing transmission gate and pass transistor logics multiplexers. Fig. 9 displays the existing multipliers which include three Half Adders, nine Full Adders and ten existing 5:2 compressors. Half Adders and Full Adders are remained same in all the multipliers but 5:2 compressors have been changed according to the type of structure employed.

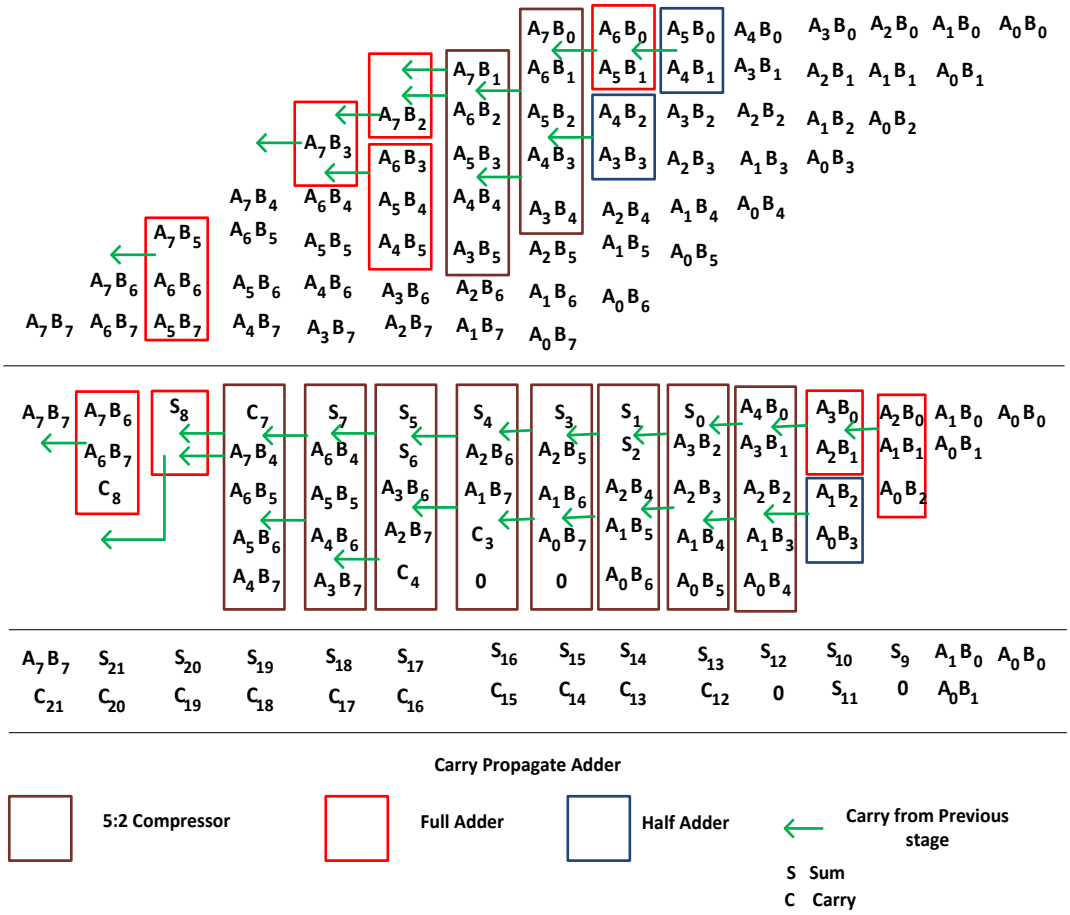

Fig 9: Multiplier using exact 5:2 compressors

Fig. 10 shown is the proposed multiplier employing all 4:2 compressors with 3 Full Adders, 3 Half Adders and 18 4:2 compressors. The 4:2 compressors have been utilized since the proposed compressor has turned into 4:2 compressor as described in proposed compressors part of this section.

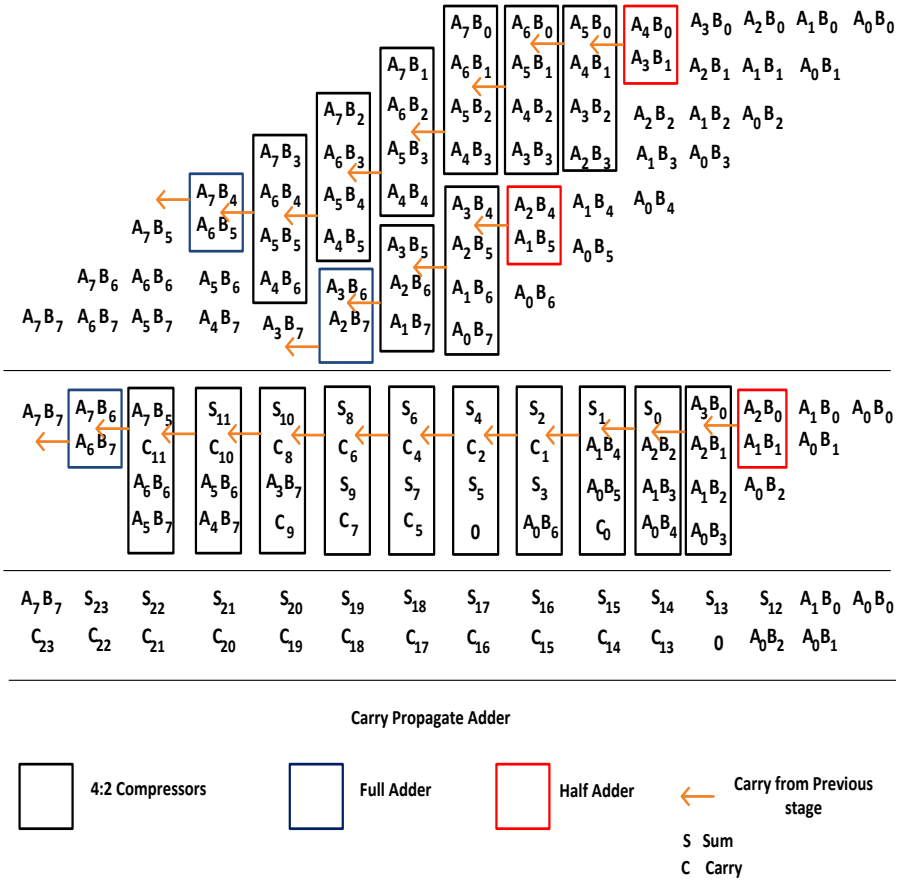

Fig 10: Proposed Multiplier using exact 4:2 compressors

IV. EXPERIMENTAL RESULTS

IV.I. Precise and Imprecise 5:2 Compressors

To demonstrate the effectiveness of the proposed 5:2 compressor, all the architectures, particularly 5:2 with exact 4:2 and 3:2, with three full adders, with six transistor XOR-XNOR and MUX gates, and the proposed one is with approximated 4:2 and exact 3:2 compressors have been implemented utilizing cadence spectre simulator in 45nm CMOS technology node and comparisons have been done among all the above implemented compressors and found that all the dimensions are lower for proposed 5:2 compressor.

The results are tabulated in Tables (I-II). Table I exhibits various 5:2 compressors [15-17] and the proposed compressor is in terms of average power dissipation and propagation delay at different supply voltages by depositing Pass transistor and transmission gate [17] logic based multiplexers.

Table I: Average Power Consumption of 5:2 Compressors

5:2 with	Power (nW)									
	Transmission Gate Logic based MUX					Pass Transistor Logic based MUX				
	0.9V	1.2V	1.8V	2.5V	3.3V	0.9V	1.2V	1.8V	2.5V	3.3V
6T XOR-XNOR	0.593	45.77	198.9	472.6	660.2	1.532	17.06	165.8	301	463.6
Exact 4:2 and 3:2	0.494	36.93	194.6	429	597.5	0.276	1.925	134.1	186.9	255.7
Full Adders	0.448	28.54	192.6	427	596.2	0.185	1.631	122.6	170.4	231.3
Proposed	0.078	11.99	164.2	290.5	399.1	0.045	0.4585	62.95	88.52	122.5

Fig. 11 and Fig. 12 displays the average power consumption of existing and proposed 5:2 compressors employing TGL and PTL two input multiplexers respectively. As predicted, according to the number of transistors employed, the average power consumption of each 5:2 compressor either exact or proposed are increasing with increase in the supply voltages. The minimum power consumed is for the proposed 5:2 compressor which when using TGL and PTL based multiplexers.

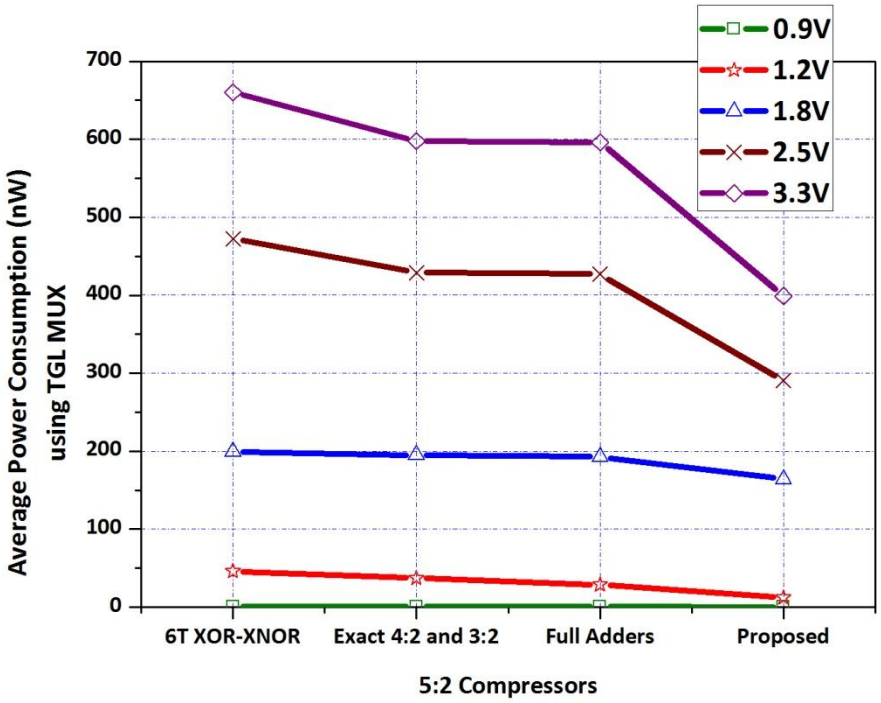

Fig 11: Average Power of 5:2 compressors using TGL

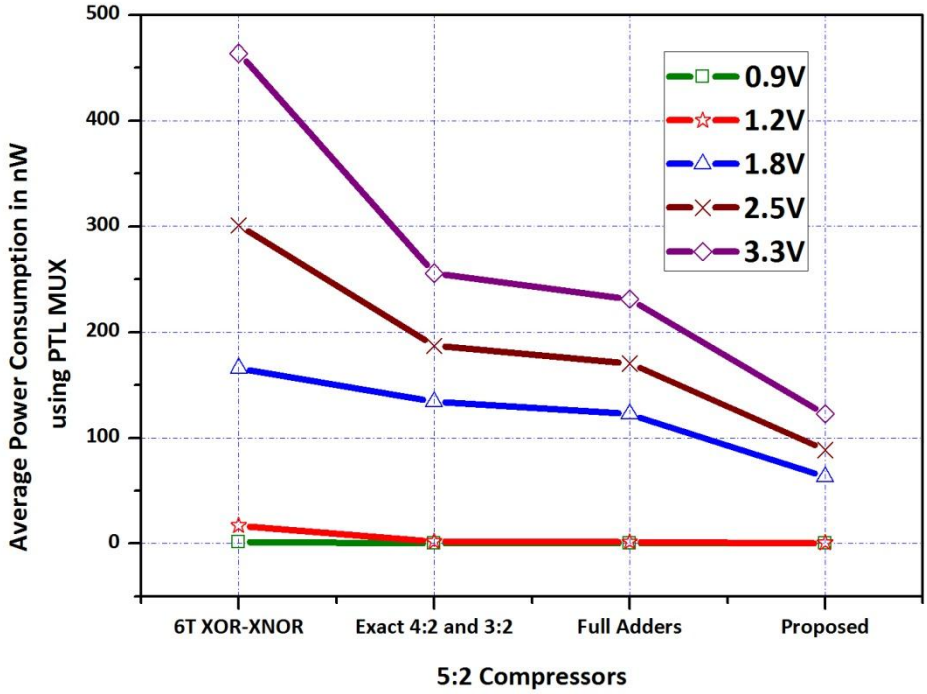

Fig 12: Average Power of 5:2 compressors using PTL

The propagation delays of all the above compressors in Table II are varying with different supply voltages but the least delay is for the proposed compressor at all the voltages under two conditions.

Table II: Propagation Delay of 5:2 Compressors

5:2 with	Propagation Delay (ns)									
	Transmission Gate Logic based MUX					Pass Transistor Logic based MUX				
	0.9V	1.2V	1.8V	2.5V	3.3V	0.9V	1.2V	1.8V	2.5V	3.3V
6T XOR-XNOR	4.64	4.831	10.139	10.085	10.085	5.197	5.205	10.173	7.199	11.194
Exact 4:2 and 3:2	5.299	5.304	0.252	5.441	5.692	0.099	0.102	0.134	0.24	0.491
Full Adders	3.568	4.997	5.043	5.094	5.099	3.703	5.239	5.268	5.364	5.606
Proposed	0.277	0.629	5.025	5.103	5.103	0.054	0.062	0.104	0.217	4.63

Fig. 13 and Fig. 14 exhibits the propagation delay in ns for all the 5:2 compressors employing TGL and PTL two input multiplexers respectively.

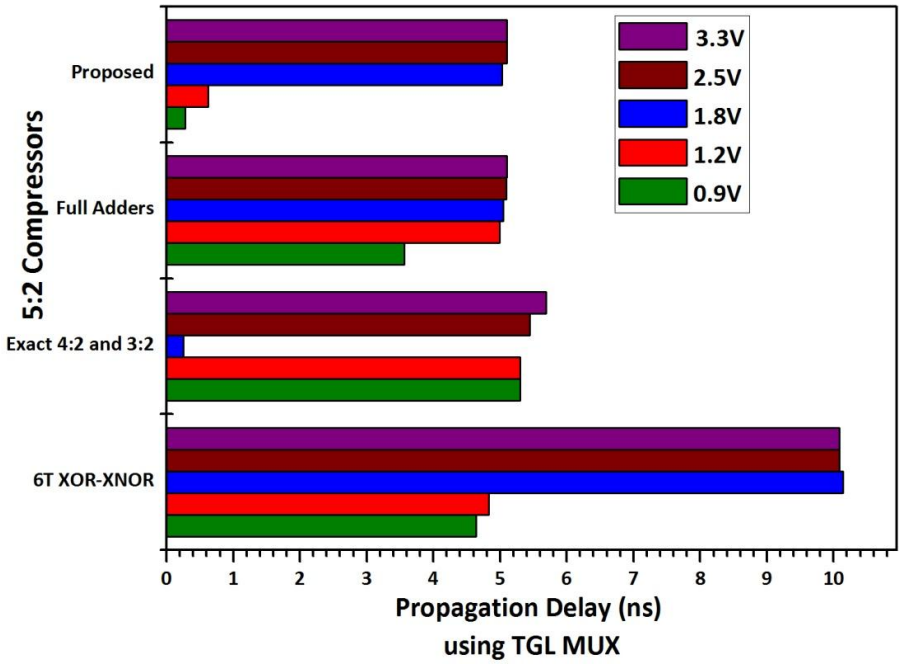

Fig 13: Propagation Delay of 5:2 compressors using TGL

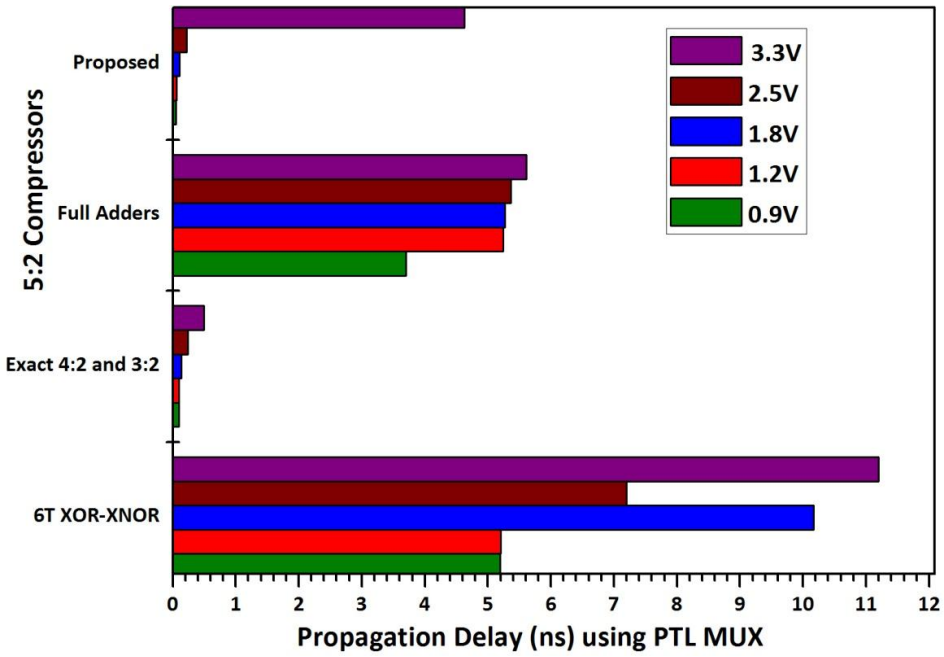

Fig 14: Propagation Delay of 5:2 compressors using PTL

IV.II. Multipliers using 5:2 Compressors

The multipliers discussed in section III are simulated employing cadence spectre simulator in 45nm technology node and found average power consumption and delay. These parameters are observed to be low for the proposed multiplier using pass transistor logic. Tables (III-IV) display the acronyms and average power and propagation delay of all the multipliers.

Table III : Multipliers with Acronyms

Multipliers	**Acronym**
Multiplier1 with existing 5:2 compressor using 6T XOR-XNOR and TGL MUX	M152E6TTGL
Multiplier2 with existing 5:2 compressor using exact 4:2, 3:2 and TGL MUX	M252E4232TGL
Multiplier3 with existing 5:2 compressor using Full Adders and TGL MUX	M352EFASTGL
Multiplier4 with existing 5:2 compressor using 6T XOR-XNOR and PTL MUX	M452E6TPTL
Multiplier5 with existing 5:2 compressor using exact 4:2, 3:2 and PTL MUX	M552E4232PTL
Multiplier6 with existing 5:2 compressor using Full Adders and PTL MUX	M652EFAsPTL
Multiplier7 with Proposed 5:2 compressor using exact 4:2, 3:2 and TGL MUX	M752P4232TGL
Multiplier8 with Proposed 5:2 compressor using exact 4:2, 3:2 and PTL MUX	M852P4232PTL

Table IV: Average Power and Delay of Multipliers

Multipliers	**Average Power(uW)**	**Propagation Delay(ns)**
M152E6TTGL	12.92	90.25
M252E4232TGL	11.85	82.35
M352EFASTGL	11.21	76.44
M452E6TPTL	8.598	71.29
M552E4232PTL	8.129	67.56
M652EFAsPTL	7.918	59.77
M752P4232TGL	8.541	51.9
M852P4232PTL	5.428	32.43

Fig. 15 shows the corresponding graph for both average power consumption in uW and propagation delay in ns of all the multipliers employing the above 5:2 compressors.

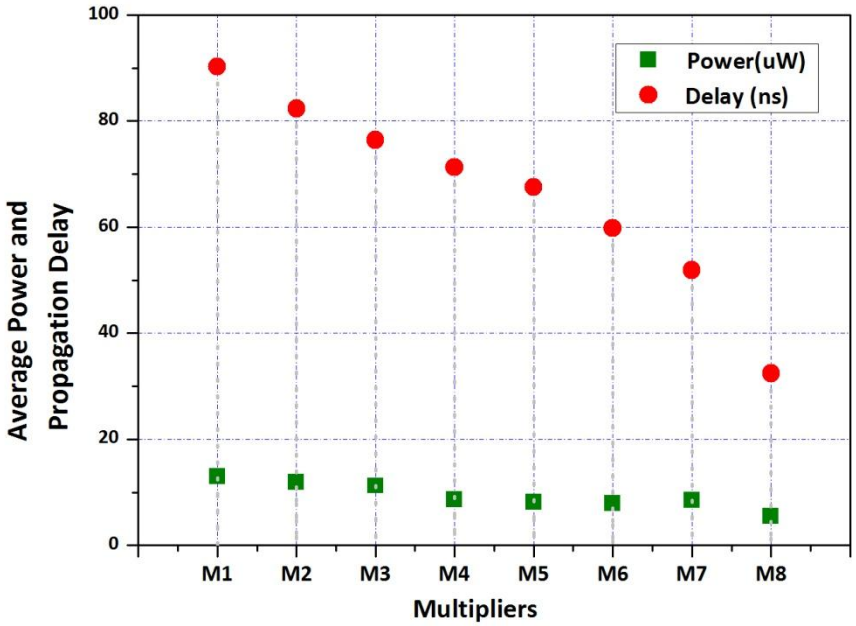

Fig 15: Average Power and Propagation Delay of multipliers

IV.III. Error Analysis of proposed Architectures

Since the proposed 5:2 compressor is a precise 4:2 compressor with two 3:2 compressors or Full Adders, the error distance (absolute difference between exact and approximate outputs), Mean Error Distance (MED), Normalized mean error distance (NMED) [18] are zero's. Thus, for this proposed compressor Sum, Carry and C_{out} bits are identical to 4:2 compressor. As the multipliers are using these compressors, existing being 5:2 and proposed being 4:2 compressors, the error distance, MED and NMED's are 0's.

V. CONCLUSION

In this paper, different 5:2 compressors have been simulated and the proposed compressor is in terms of approximate 4:2 and exact 3:2 compressors by depositing six transistor XOR-XNOR gates, TGL and PTL based multiplexers. The proposed 5:2 compressor has become exact 4:2 compressor after applying approximations which has been employed in the Dadda structure and found that the average power consumption and propagation delay of the proposed design is less for the compressor and multiplier architectures when analyzed with the other arrangements.

VI. ACKNOWLEDGMENTS

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