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Fault Identification Method Applied to Full-Bridge Submodule of MMC

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Abstract

This paper considers MMC submodule fault identification method valid for both open circuit and short circuit cases. The article is mainly focused on DC-link capacitor abnormal operation. Proposed protection method is based on comparison of measured and calculated DC-link capacitor voltages. The protection algorithm is tested by means of computer modeling for the particular design of modular multilevel converter based active power conditioner with uninterruptible power supply capability. It is shown that proposed method provides fault detection over the time interval of order of PWM period that is sufficient for the safe operation of Submodule.

Keywords: Capacitor, Fault, IGBT, MMC, Observer, Protection, Submodule.

I. INTRODUCTION

Modular multilevel converter (MMC) is rapidly developing during the last decade and more than 10 HVDC transmissions, HVDC B2B and STATCOM equipment based on MMC scheme are commissioned at present [1]. Modular scheme allows to implement medium and high voltage transistor valves without direct connection of IGBT-modules in series that cancels simultaneous commutation control of all transistors and does not require active drivers. Furthermore MMC scheme provides low current harmonics emission of converter while keeping switching frequency of individual semiconductor devices in range of 50-1200 Hz [2]. The listed features make MMC technology attractive for both HVDC transmissions and active power conditioners.

Modular multilevel converters defers in functions, rated parameters, converters topologies or submodules schemes but all of them have at least one common property, e.g. all submodules in the phase (or arm) are connected in series. As a rule all MMC

devices are designed with a number of extra submodules in each phase that provides it to operate normally even when some modules get broken. For stopples operation it is necessary to detect faulty submodule and to bypass it automatically. A number of works investigates this problem [3-5], but none of them considers full-bridge scheme of submodule.

This paper is organized as follows. Basic MMC design parameters developed in project and submodule scheme are presented in Section 2. Submodule fault types analyzes are summarised in section 3. Faults detection method is given in Section 4. Electrical models as well as protection algorithm are described in Section 5 and some conclusions are given in Section 6.

II. CONVERTER DESIGN

Converter scheme shown in Fig.1a was developed for modular multilevel converter based active power conditioner with uninterruptible power supply capability [6]. Main converter parameters are indicated in Table 1. Discussed device contains voltage source converter and supercapacitor based energy storage. The converter includes six arms grouped into three phases. Each arm includes reactor and a number of identical submodules connected in series.

Table 1. Power Conditioner Specifications

Parameter	Value
Rated AC Voltage	6.0 kV
Rated power	6.0 MVA
Number of submodules in arm	10
Rated SM voltage	1200 V
Rated energy storage capacity	9.0 MJ
Rated DC voltage of energy storage	9.6 kV
Peak active power	3.0 MW
PWM switching frequency	1000 Hz
Arm reactor inductance	5.0 mH

Most of the time described power conditioner acts as active filter compensating imaginary power of load connected in parallel with it. Power conditioner starts to supply active power to sensitive load during deep voltage sag, momentary or instantaneous interruption after islanding them from the main grid.

Simplified scheme of full FB-SM power circuit is shown in Fig.1b, where «A1»-«A4» are Semikron SKM400GB17E4 IGBT-modules, «C» – DC-link capacitors assembly of 4 ElectronicON capacitors E50.S34-205NT0 (2 mF), «S» are IGBTs and «D» are

freewheeling diodes respectively. Modules «A1» and «A2» are connected in parallel as «A3» and «A4» so transistors «S_j» and «S_j'» operates simultaneously (j=1,2,3,4). Post-fault mechanical bypass is denoted by «QS».

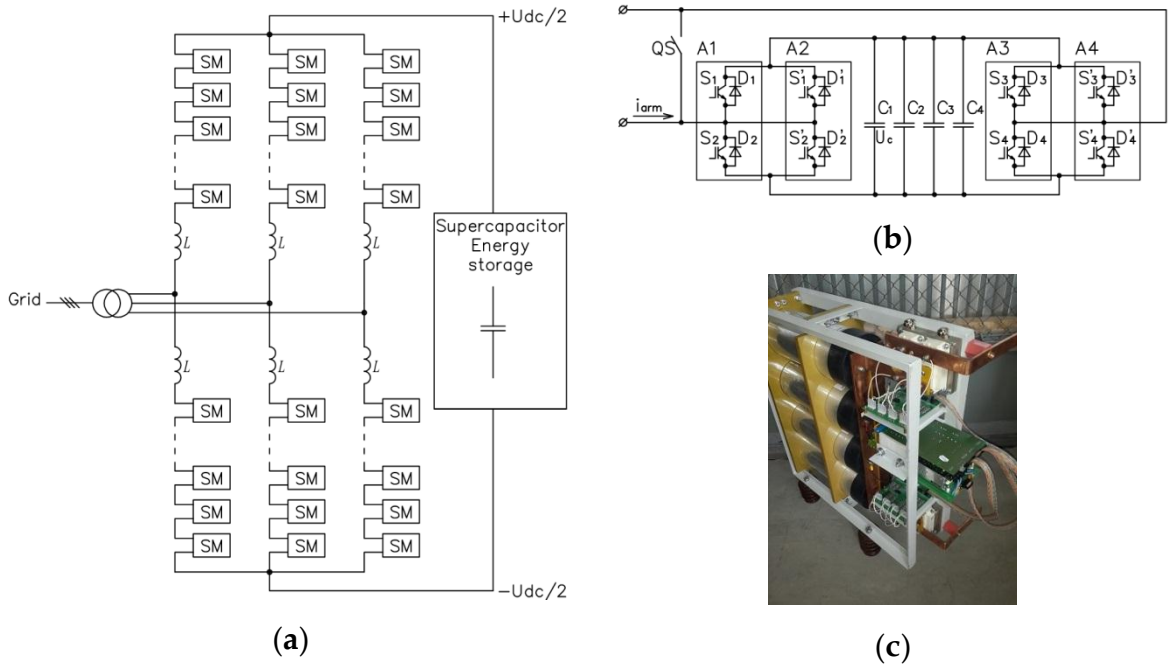


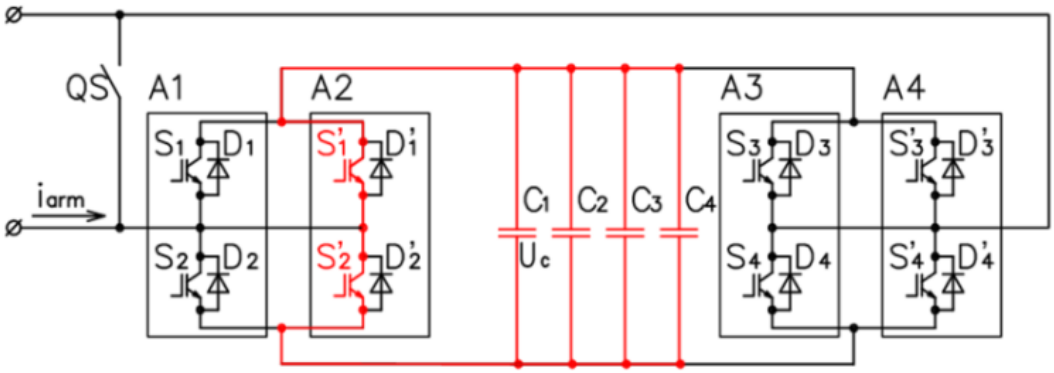
Figure 1. (a) converter scheme; (b) submodule scheme; (c) submodule design

III. SUBMODULE FAULT TYPES ANALYZES

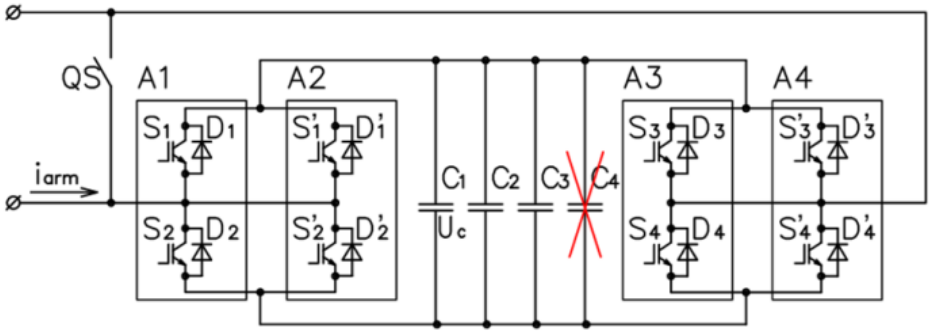
Two types of submodule faults are considered in [3], namely open circuit of IGBT-module and it's short circuit. The former is supposed to be a consequence of overheating of IGBT-module and bonding wires lifting. The latter is supposed to be due to wrong gating signals of supplementary transistors in half-bridge submodule or semiconductor breakdown caused by overvoltage. Main failure rate in submodule is related to semiconductor elements break-down followed by DC-link short circuit according to [7]. It is noted that such fault can procced in two ways. Short circuit of the broken device becomes a stable state if press-pack IGBT are used and on the contrary the faulty IGBT-module eventually may lead to an open circuit if common industrial IGBT-modules are used. Papers [4-5] considers only open-circuit types of IGBT faults while [8] gives more broad abnormal modes classification witch shows that DC-link capacitor fault is the second most frequent problem in submodules of cascaded converters while [9] specifies that film capacitors tend to fall into open-circuit mode of operation if it is faulty.

Open-circuit mode of IGBT fault is not considered in this work because a number of reasons. Firstly each leg of the bridge consists of two IGBT-model connected in parallel that reduces the probability such type of the fault. Second, IGBT driver is

capable to detect transistor misoperation by means of collector-emitter voltage monitoring [10]. So on the base of reasons described above the following fault types are considered: pole-to-pole (Fig. 2a) short circuit and open circuit of one of the DC-link capacitors (Fig. 2b).



(**a**)



(**b**)

Figure 2. Submodule faults scheme: (a) IGBT fault; (b) Capacitor fault.

IV. FAULTS DETECTION METHOD

In this paper a normal mode of submodule operation supposes output voltage of it is defined as $gs \times U_c$, where U_c is the instantaneous DC-link capacitor voltage and gs is defined according to Table 2. So there is no faults in normal mode of submodule operation and it is not operating as diode rectifier. Under these conditioned arm current I_{arm} and capacitor voltage U_c are related as follows:

$$C_s \cdot \frac{dU_c}{dt} = gs \cdot I_{arm} \tag{1}$$

where «C_s» is equivalent DC-link capacitance and «gs» is gating signal state defined by Table 2. It should be noted that the Table does not include states corresponding to diode mode of operation of the bridge and any abnormal states.

Table 2. Submodule IGBT states under normal operation.

gs	S1 & S1'	S2 & S2'	S3 & S3'	S4 & S4'	Zero state type (ZT)
-1	OFF	ON	ON	OFF	-
0	ON	OFF	ON	OFF	0
0	OFF	ON	OFF	ON	1
1	ON	OFF	OFF	ON	-

Submodule fault identification method is based on deviation signal Err calculation as follows:

$$E_{rr}(t) = \left| \int_{t-T}^{t} (U_c(\tau) - gs(\tau) \cdot I_{arm}(\tau)/C_s) d\tau \right| \quad (2)$$

where averaging interval is denoted by «T». Under normal conditions Err is of an order of voltage measurement tolerance.

Once fault occurs, equation (1) is violated so Err begin to increase. Protection counter Cnt starts to rise while Err exceeds the predefined limit K1 otherwise it falls until it reaches zero. If the counter Cnt exceeds predefined setpoint K2 the protection rises it's flag signaling that fault is detected and forcing bypass switch QS shown in Fig.1b to close.

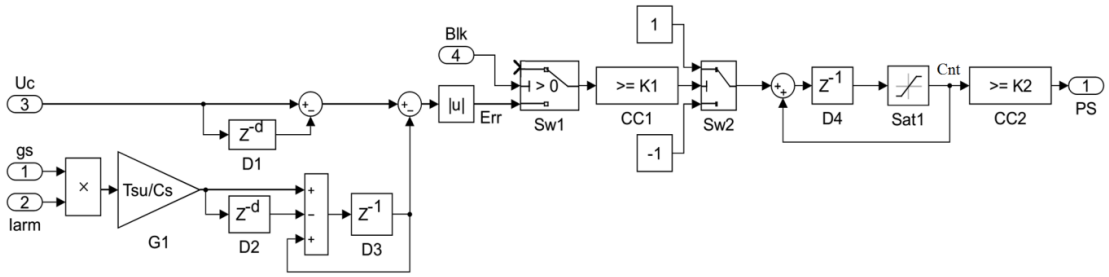


Figure 3. Proposed protection SM scheme in Simulink.

V. PROTECTION TESTING BY MEANS OF COMPUTER MODELING

Electrical modes of submodule operation are calculated by means of Matlab Simulink SimPowerSystems. Submodule scheme shown in Fig. 1b is assembled of standard SimPowerSystems library blocks. Submodule current is provided by controlled current source connected to it's AC terminals.

Described in section IV fault detection method is modeled by means of Simulink blocks as it is shown in Fig. 3, where step time is denoted by «Tsu» and is equal to 10 μs; «D1» and «D2» are 1 ms delay blocks; one step delay block are denoted as «D3» and «D4»; «Sat1» is saturation block that set lower limit at 0 level and upper limit at K2 level; «Blk» is a special signal that blocks protection during the converter start-up when submodule bridge operated as uncontrolled rectifier. Parameters K1 and K2 are set equal to 5 and 10 respectively. The delay of blocks D1 and D2 are of the same order as PWM period. It should be noted that the designed converter exploits phase-

shifted PWM with switching frequency of 1 kHz.

Pole-to-pole short circuit shown in Fig.2a was tested both under idle and rated current conditions. Time interval between considered faults instant and flag rise is less than 100 µs. Another series of experiments tested protection functions in case when one of four capacitors shown in Fig. 2b came into open circuit mode of operation. Reduced to 75% of rated value of arm current was used corresponding to rated current flowing through each of three capacitors in submodule after one of four goes into open circuit mode. The dependencies of arm current, DC-link capacitors voltage, deviation signal Err and counter signal Cnt on time are shown in Fig. 4 respectively, where the fault occurs at instant of 60 ms. Time interval between considered fault instant and flag rise does not exceed PWM period that is equal to 1 ms in this work. Conducted tests proofed the ability of proposed algorithm to detect considered faults under 5% tolerance of both DC-link voltage sensor and arm current transformer. Supplementary test of IGBT-module faults similar to [3-5] show the applicability of described algorithm for detecting IGBT-open circuit faults.

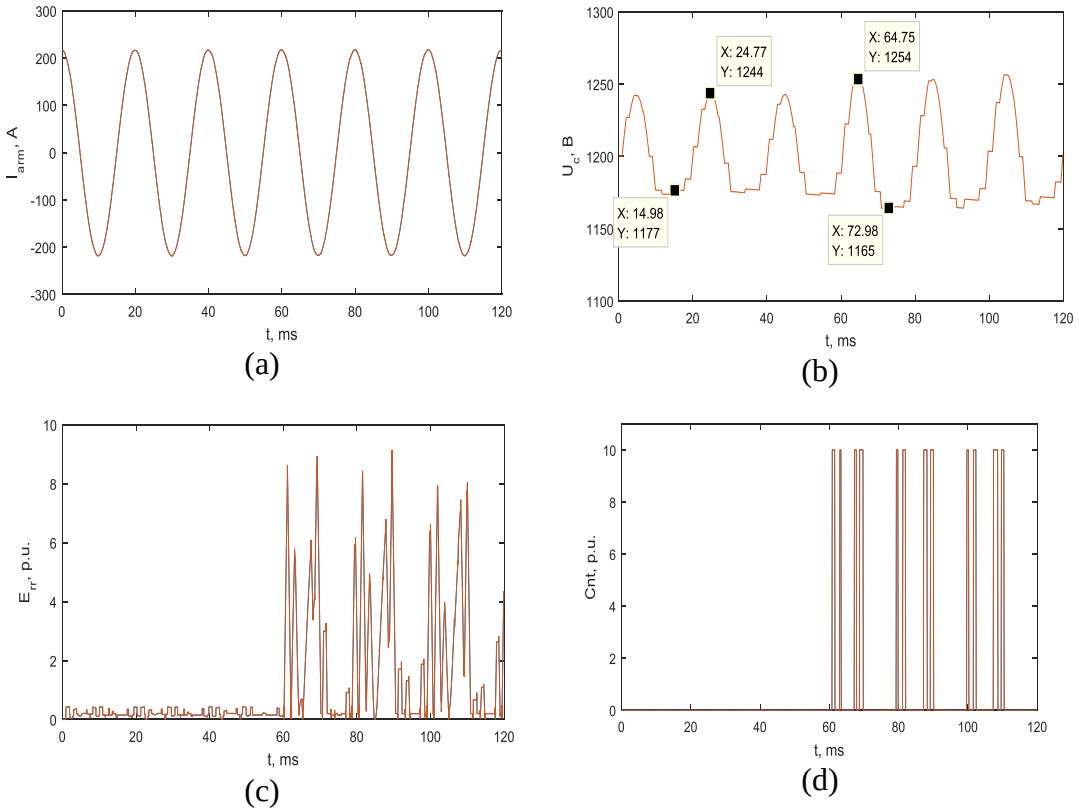


Figure 4. Test results: (a) Arm current during capacitor open circuit fault; (b) DC-link voltage during capacitor open circuit fault; (c) Err signal during capacitor open circuit fault; (d) Cnt signal during capacitor open circuit fault.

VI. CONCLUSION

Method of submodule abnormal operation detection is proposed and tested. Both short circuit of IGBT-module and DC-link capacitor open circuit types of faults can be detected. In former case the proposed method can be used as backup protection for driver ones. In latter case proposed method can be used as main protection of DC-link capacitors assembly. The protection showed robustness against current and voltage measurement errors inherent in 5% tolerance.

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